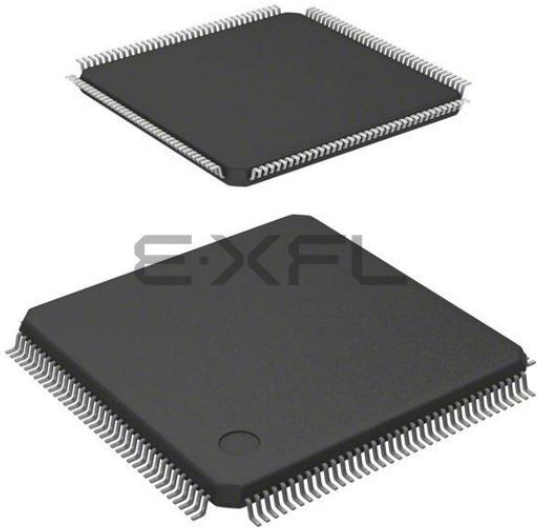


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	112
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f733zet6

List of figures

2. Available only on the STM32F733xx devices.

3 Functional overview

3.1 Arm® Cortex®-M7 with FPU

The Arm® Cortex®-M7 with FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and low interrupt latency.

The Cortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard caches (8 Kbytes of I-cache and 8 Kbytes of D-cache)
- 64-bit AXI4 interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The processor supports the following memory interfaces:

- Tightly Coupled Memory (TCM) interface.
- Harvard instruction and data caches and AXI master (AXIM) interface.
- Dedicated low-latency AHB-Lite peripheral (AHBP) interface.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

It supports single precision FPU (floating point unit), speeds up software development by using metalanguage development tools, while avoiding saturation.

Figure 5 shows the general block diagram of the STM32F732xx and STM32F733xx family.

Note: Cortex®-M7 with FPU core is binary compatible with the Cortex®-M4 core.

3.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

On the STM32F7x3xx devices, the USB OTG HS sub-system uses an additional power supply pin:

- The VDD12OTGHS pin is the output of PHY HS regulator (1.2V). An external capacitor of 2.2 µF must be connected on the VDD12OTGHS pin.

3.15 Power supply supervisor

3.15.1 Internal reset ON

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other packages, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.15.2 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled through the PDR_ON pin.

An external power supply supervisor should monitor V_{DD} and NRST and should maintain the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON should be connected to V_{SS}. Refer to *Figure 9: Power supply supervisor interconnection with internal reset OFF*.

Table 10. STM32F732xx and STM32F733xx pin and ball definition

Pin Number										Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F732xx					STM32F733xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	1	1	A2	1	C9	A2	A3	1	1	PE2	I/O	FT	-	TRACECLK, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, FMC_A23, EVENTOUT	-
-	2	2	A1	2	A10	A1	A2	2	2	PE3	I/O	FT	-	TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT	-
-	3	3	B1	3	D9	B1	B2	3	3	PE4	I/O	FT	-	TRACED1, SPI4_NSS, SAI1_FS_A, FMC_A20, EVENTOUT	-
-	4	4	B2	4	E8	B2	B3	4	4	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, FMC_A21, EVENTOUT	-
-	5	5	B3	5	B10	B3	B4	5	5	PE6	I/O	FT	-	TRACED3, TIM1_BKIN2, TIM9_CH2, SPI4_MOSI, SAI1_SD_A, SAI2_MCK_B, FMC_A22, EVENTOUT	-
1	6	6	C1	6	C10	C1	C2	6	6	VBAT	S	-	-	-	-

Table 10. STM32F732xx and STM32F733xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F732xx					STM32F733xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	-	D2	7	-	D2	-	-	7	PI8	I/O	FT	(2)(3)	EVENTOUT	RTC_TAMP2/ RTC_TS, WKUP5
2	7	7	D1	8	D10	D1	A1	7	8	PC13	I/O	FT	(2)(3)	EVENTOUT	RTC_TAMP1/ RTC_TS/ RTC_OUT, WKUP4
3	8	8	E1	9	E9	E1	B1	8	9	PC14-OSC32_IN(PC14)	I/O	FT	(2)(3)(5)	EVENTOUT	OSC32_IN
4	9	9	F1	10	E10	F1	C1	9	10	PC15-OSC32_OUT(PC15)	I/O	FT	(2)(3)(5)	EVENTOUT	OSC32_OUT
-	-	-	D3	11	-	D3	-	-	11	PI9	I/O	FT	-	UART4_RX, CAN1_RX, FMC_D30, EVENTOUT	-
-	-	-	E3	12	-	E3	-	-	12	PI10	I/O	FT	-	FMC_D31, EVENTOUT	-
-	-	-	E4	13	-	E4	-	-	13	PI11	I/O	FT	(4)	OTG_HS_ULPI_DIR, EVENTOUT	WKUP6
-	-	-	F2	14	-	F2	-	-	14	VSS	S	-	-	-	-
-	-	-	F3	15	-	F3	-	-	15	VDD	S	-	-	-	-

Table 10. STM32F732xx and STM32F733xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F732xx					STM32F733xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
39	65	98	G14	117	D2	G14	F11	98	117	PC8	I/O	FT	-	TRACED1, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, SDMMC1_D0, EVENTOUT	-
40	66	99	F14	118	D1	F14	E11	99	118	PC9	I/O	FTf	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, SDMMC1_D1, EVENTOUT	-
41	67	100	F15	119	D3	F15	E12	100	119	PA8	I/O	FTf	-	MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, EVENTOUT	-
42	68	101	E15	120	C3	E15	D12	101	120	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, EVENTOUT	OTG_FS_VBUS
43	69	102	D15	121	C2	D15	D11	102	121	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, OTG_FS_ID, EVENTOUT	-
44	70	103	C15	122	C1	C15	C12	103	122	PA11	I/O	FT	-	TIM1_CH4, USART1_CTS, CAN1_RX, OTG_FS_DM, EVENTOUT	-
45	71	104	B15	123	B2	B15	B12	104	123	PA12	I/O	FT	-	TIM1_ETR, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, EVENTOUT	-
46	72	105	A15	124	B1	A15	A12	105	124	PA13(JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-

Table 12. STM32F732xx and STM32F733xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1	I2C1/2/3/USART1	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5	SPI2/I2S2/SPI3/I2S3/SPI3/I2S3/SAI1/UART4	SPI2/I2S2/SPI3/I2S3/USART1/2/3/UART5	SAI2/USART6/UART4/5/7/8/OTG1_FS	CAN1/TIM12/13/14/QUADSPI/FMC/OTG2_HS	SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS	SDMMC2	UART7/FMC/SDMMC1/OTG2_FS	SYS
Port I	PI7	-	-	-	TIM8_CH3	-	-	-	-	-	-	SAI2_FS_A	-	FMC_D29	EVENTOUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PI9	-	-	-	-	-	-	-	-	UART4_RX	CAN1_RX	-	-	FMC_D30	EVENTOUT
	PI10	-	-	-	-	-	-	-	-	-	-	-	-	FMC_D31	EVENTOUT
	PI11	-	-	-	-	-	-	-	-	-	-	OTG_HS_ULPI_DIR	-	-	EVENTOUT
	PI12	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PI13	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PI14	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PI15	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.7 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 24*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 25*.

Figure 24. Pin loading conditions

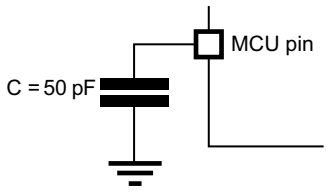


Figure 25. Pin input voltage

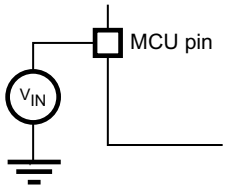


Table 16. General operating conditions (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{12}	Regulator ON: 1.2 V internal voltage on V_{CAP_1}/V_{CAP_2} pins	Power Scale 3 ((VOS[1:0] bits in PWR_CR register = 0x01), 144 MHz HCLK max frequency	1.08	1.14	1.20	V
		Power Scale 2 ((VOS[1:0] bits in PWR_CR register = 0x10), 168 MHz HCLK max frequency with over-drive OFF or 180 MHz with over-drive ON	1.20	1.26	1.32	
		Power Scale 1 ((VOS[1:0] bits in PWR_CR register = 0x11), 180 MHz HCLK max frequency with over-drive OFF or 216 MHz with over-drive ON	1.26	1.32	1.40	
	Regulator OFF: 1.2 V external voltage must be supplied from external regulator on V_{CAP_1}/V_{CAP_2} pins[7]	Max frequency 144 MHz	1.10	1.14	1.20	
		Max frequency 168MHz	1.20	1.26	1.32	
		Max frequency 180 MHz	1.26	1.32	1.38	
V_{IN}	Input voltage on RST and FT pins[8]	2 V ≤V_{DD} ≤3.6 V	− 0.3	-	5.5	
		V_{DD} ≤2 V	− 0.3	-	5.2	
	Input voltage on TTa pins	-	− 0.3	-	V_{DDA}+ 0.3	
	Input voltage on BOOT pin	-	0	-	9	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7[9]	LQFP64	-	-	881	mW
		LQFP100	-	-	1117	
		WLCSP100	-	-	558	
		LQFP144	-	-	1587	
		LQFP176	-	-	1869	
		UFBGA144	-	-	476	
		UFBGA176	-	-	485	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	− 40	-	85	°C
		Low power dissipation[10]	− 40	-	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	− 40	-	105	°C
		Low power dissipation[10]	− 40	-	125	
T_J	Junction temperature range	6 suffix version	− 40	-	105	°C
		7 suffix version	− 40	-	125	

1. The over-drive mode is not supported at the voltage ranges from 1.7 to 2.1 V.
2. 216 MHz maximum frequency for 6 suffix version (200 MHz maximum frequency for 7 suffix version).
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.15.2: Internal reset OFF*).
4. When the ADC is used, refer to *Table 67: ADC characteristics*.
5. If V_{REF+} pin is present, it must respect the following condition: V_{DDA}-V_{REF+} < 1.2 V.
6. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.

7. The over-drive mode is not supported when the internal regulator is OFF.
8. To sustain a voltage higher than VDD+0.3, the internal Pull-up and Pull-Down resistors must be disabled
9. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
10. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

Table 17. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$)	Maximum HCLK frequency vs Flash memory wait states (1)(2)	I/O operation	Possible Flash memory operations
V_{DD} =1.7 to 2.1 V(3)	Conversion time up to 1.2 Msps	20 MHz	180 MHz with 8 wait states and over-drive OFF	No I/O compensation	8-bit erase and program operations only
V_{DD} = 2.1 to 2.4 V	Conversion time up to 1.2 Msps	22 MHz	216 MHz with 9 wait states and over-drive ON	No I/O compensation	16-bit erase and program operations
V_{DD} = 2.4 to 2.7 V	Conversion time up to 2.4 Msps	24 MHz	216 MHz with 8 wait states and over-drive ON	I/O compensation works	16-bit erase and program operations
V_{DD} = 2.7 to 3.6 V(4)	Conversion time up to 2.4 Msps	30 MHz	216 MHz with 7 wait states and over-drive ON	I/O compensation works	32-bit erase and program operations

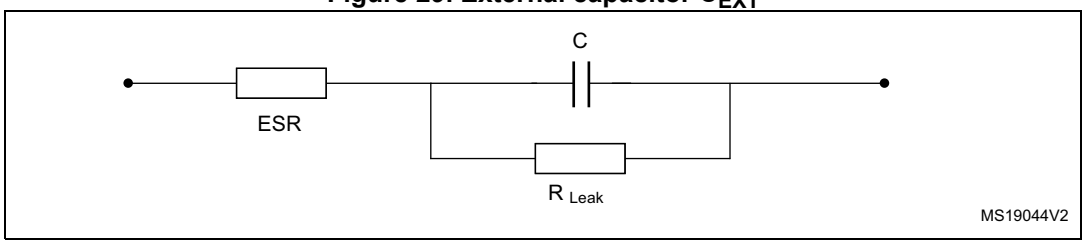
1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator on ITCM interface and L1-cache on AXI interface, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator or L1-cache allows to achieve a performance equivalent to 0-wait state program execution.
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.15.2: Internal reset OFF*).
4. The voltage range for USB full speed PHYs can drop down to 2.7 V. However the electrical characteristics of D- and D+ pins will be degraded between 2.7 and 3 V.

6.3.2 VCAP1/VCAP2 external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the VCAP1/VCAP2 pins. C_{EXT} is specified in *Table 18*.

Note: The VCAP2 pin is not available on the LQFP64 package.

Figure 29. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

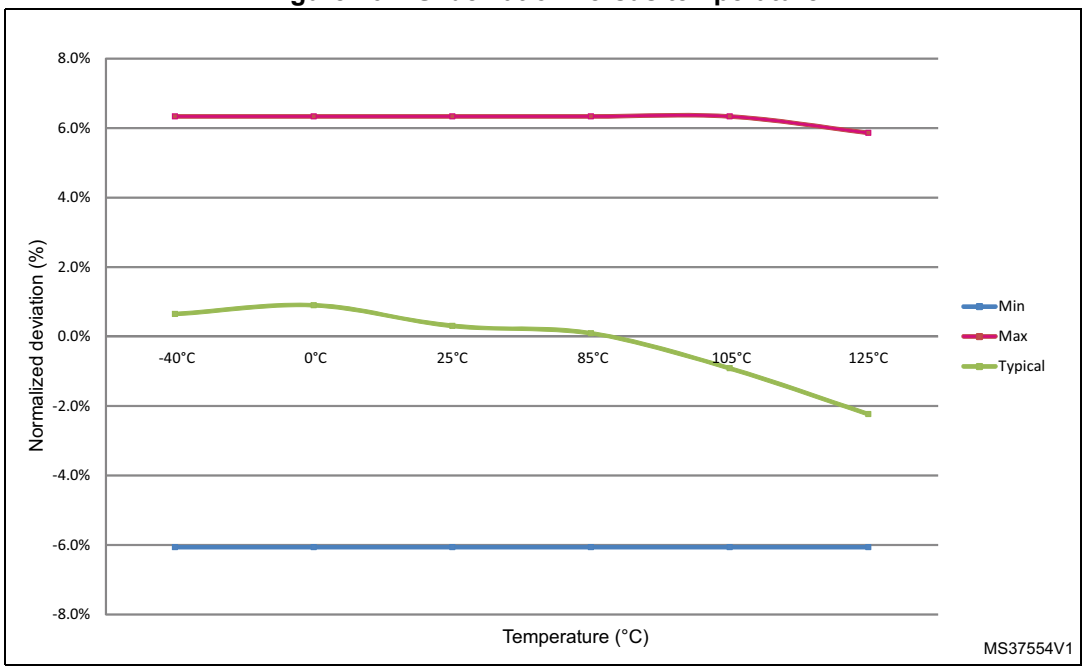
Low-speed internal (LSI) RC oscillator

Table 43. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	17	32	47	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design.

Figure 40. LSI deviation versus temperature



6.3.11 PLL characteristics

The parameters given in *Table 44* and *Table 45* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 16*.

Table 44. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)	-	0.95(2)	1	2.10	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	24	-	216	
f_{PLL48_OUT}	48 MHz PLL multiplier output clock	-	-	48	75	
f_{VCO_OUT}	PLL VCO output	-	100	-	432	

Table 45. PLLI2S characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Jitter(3)	Master I2S clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-	ps
			peak to peak	-	±280	-	ps
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	ps
	WS I2S clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	ps
$I_{DD(PLLI2S)}$(4)	PLLI2S power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$(4)	PLLI2S power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

Table 46. PLLISAI characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLLSAI_IN}	PLLSAI input clock(1)	-		0.95(2)	1	2.10	MHz
$f_{PLLSAIP\_OUT}$	PLLSAI multiplier output clock for 48 MHz	-		-	48	75	
$f_{PLLSAIQ\_OUT}$	PLLSAI multiplier output clock for SAI	-		-	-	216	
f_{VCO_OUT}	PLLSAI VCO output	-		100	-	432	
t_{LOCK}	PLLSAI lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Master SAI clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-	ps
			peak to peak	-	±280	-	ps
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	ps
	FS clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	ps

- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 57. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				25/200 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP176 package, conforming to IEC61967-2 ART/L1-cache OFF, over-drive ON, all peripheral clocks enabled, clock dithering disabled.	0.1 MHz to 30 MHz	23	dBµV
			30 MHz to 130 MHz	20	
			130 MHz to 1 GHz	34	
			1 GHz to 2 GHz	24	
			EMI Level	4	-

6.3.18 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/ESDA/JEDEC JS-001-2012 and ANSI/ESD S5.3.1-2009 standards.

Table 58. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001-2012	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD STM5.3.1-2009, all the packages excepted WLCSP100	3	250	

1. Guaranteed by characterization results.

Table 93. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	2Thclk -1	2Thclk +1	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	0.5	
$t_{w(NOE)}$	FMC_NOE low time	2Thclk -1	2Thclk +1	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL\_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	Thclk -1.5	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	Thclk -1.5	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	Thclk -0.5	

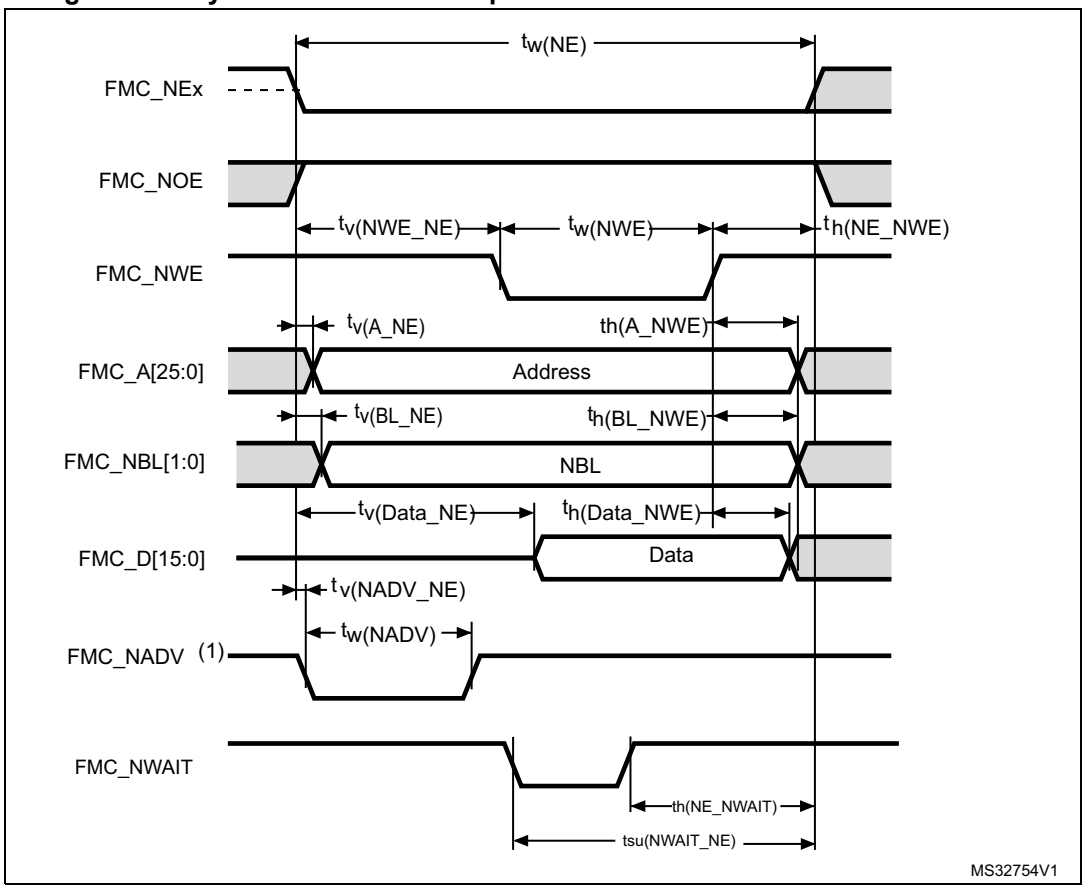
1. C_L = 30 pF.

Table 94. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	7Thclk +1	7Thclk +1	ns
$t_{w(NOE)}$	FMC_NWE low time	5Thclk -1	5Thclk +1	
$t_{w(NWAIT)}$	FMC_NWAIT low time	Thclk -0.5	-	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	5Thclk +1.5	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4Thclk +1	-	

1. Guaranteed by characterization results.

Figure 61. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 95. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	3Thclk +1	3Thclk +1	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	Thclk - 0.5	Thclk +0.5	
$t_{w(NWE)}$	FMC_NWE low time	Thclk - 1.5	Thclk +0.5	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	Thclk	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	Thclk - 0.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	Thclk - 0.5	-	
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	Thclk +1.5	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	Thclk +0.5	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	Thclk - 0.5	

1. Guaranteed by characterization results.

Figure 63. Asynchronous multiplexed PSRAM/NOR write waveforms

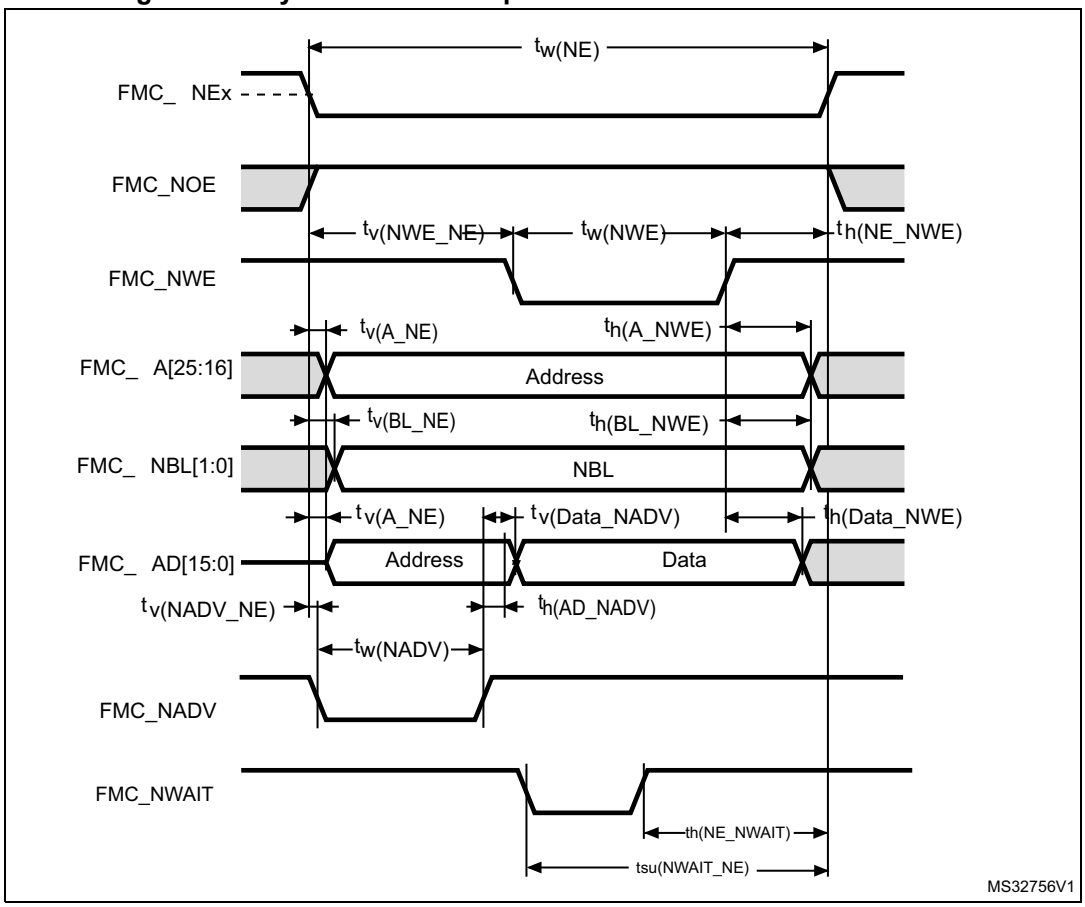


Table 99. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	4Thclk -1	4Thclk +1	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	Thclk -0.5	Thclk +0.5	
$t_{w(NWE)}$	FMC_NWE low time	2Thclk -0.5	2Thclk +0.5	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	Thclk -0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	Thclk	Thclk +1	
$t_{h(AD\_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high)	Thclk +0.5	-	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	Thclk +0.5	-	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	Thclk -0.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	Thclk +1.5	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	Thclk +0.5	-	

1. Guaranteed by characterization results.

Table 100. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	9Thclk - 1	9Thclk + 1	ns
$t_{w(NWE)}$	FMC_NWE low time	7Thclk -0.5	7Thclk + 0.5	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	6Thclk + 2	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4Thclk - 1	-	

1. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 64 through *Figure 67* represent synchronous waveforms and *Table 101* through *Table 104* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM
- CL = 30 pF on data and address lines. CL = 10 pF on FMC_CLK unless otherwise specified.

In all timing tables, the T_{HCLK} is the HCLK clock period.

- For 2.7 V≤V_{DD}≤3.6 V, maximum FMC_CLK = 108 MHz at CL=20 pF or 90 MHz at CL=30 pF (on FMC_CLK).
- For 1.71 V≤V_{DD}<2.7 V, maximum FMC_CLK = 70 MHz at CL=10 pF (on FMC_CLK).

SDRAM waveforms and timings

- CL = 30 pF on data and address lines. CL = 10 pF on FMC_SDCLK unless otherwise specified.

In all timing tables, the T_{HCLK} is the HCLK clock period.

- For 3.0 V≤V_{DD}≤3.6 V, maximum FMC_SDCLK= 100 MHz at CL=20 pF (on FMC_SDCLK).
- For 2.7 V≤V_{DD}≤3.6 V, maximum FMC_SDCLK = 90 MHz at CL=30 pF (on FMC_SDCLK).
- For 1.71 V≤V_{DD}<1.9 V, maximum FMC_SDCLK = 70 MHz at CL=10 pF (on FMC_SDCLK).

Figure 72. SDRAM read access waveforms (CL = 1)

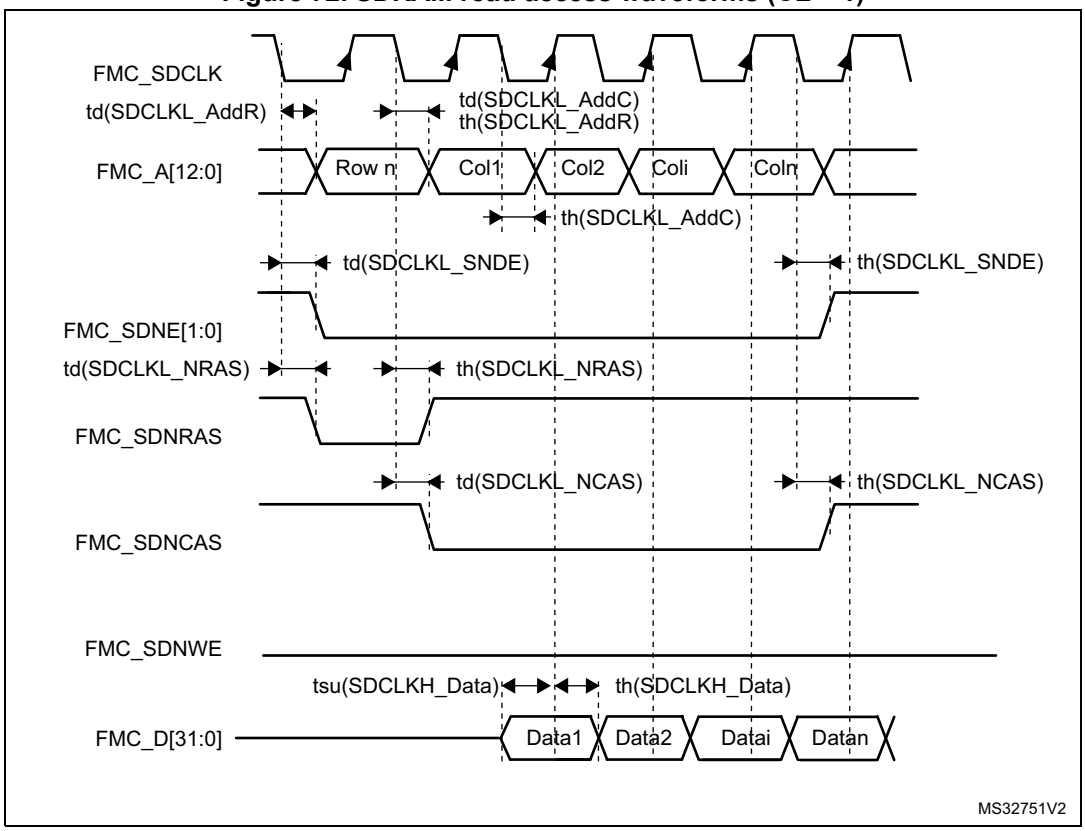


Table 119. UFBGA144 - 144-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 91. UFBGA144 - 144-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint

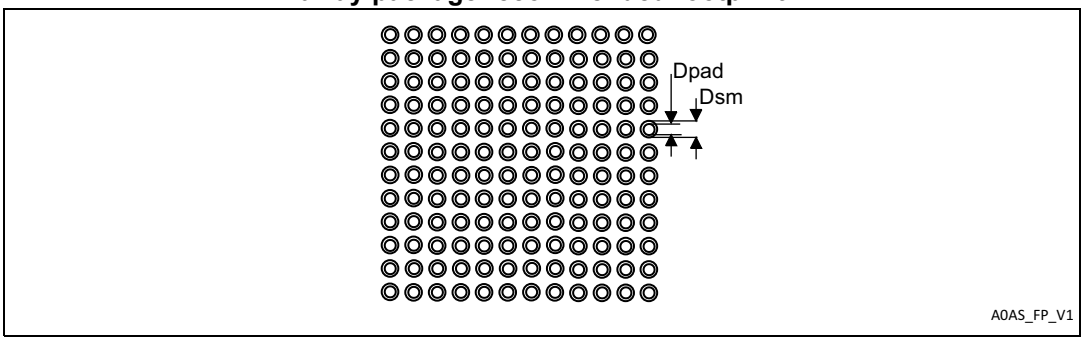


Table 120. UFBGA144 recommended PCB design rules (0.50 mm pitch BGA)

Dimension	Recommended values
Pitch	0.50 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm