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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	-
Number of Cores/Bus Width	-
Speed	-
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc13212r2

- HVAC
- Automated meter reading

- Health Care
  - Patient monitoring
  - Fitness monitoring
- Consumer
  - Human interface devices (keyboard, mice, etc.)
  - Remote control
  - Wireless toys

1.1 Ordering Information

Table 1 provides additional details about the MC1321x family.

NOTE

The device marking for silicon revision 1.1 and newer is different than version 1.0 and older. For more details about the 71-pin LGA package used for the MC1321x family, see the *802.15.4/ZigBee Hardware Design Considerations Reference Manual* (ZHDCRM).

Table 1. Orderable Parts Details

Device	Operating Temp Range (TA.)	Package	Memory Options	Description
MC13211	-40° to 85° C	LGA	1KB RAM, 16KB Flash	Intended for proprietary applications and Freescale Simple MAC (SMAC)
MC13211R2	-40° to 85° C	LGA Tape and Reel	1KB RAM, 16KB Flash	Intended for proprietary applications and Freescale Simple MAC (SMAC)
MC13212	-40° to 85° C	LGA	2KB RAM, 32KB Flash	Intended for 802.15.4 Standard compliant applications and Freescale 802.15.4 MAC
MC13212R2	-40° to 85° C	LGA Tape and Reel	2KB RAM, 32KB Flash	Intended for 802.15.4 Standard compliant applications and Freescale 802.15.4 MAC
MC13213	-40° to 85° C	LGA	4KB RAM, 60KB Flash	Intended for 802.15.4 Standard compliant applications and the Freescale 802.15.4 MAC and fully ZigBee compliant Freescale BeeStack.
MC13213R2	-40° to 85° C	LGA Tape and Reel	4KB RAM, 60KB Flash	Intended for 802.15.4 Standard compliant applications and Freescale 802.15.4 MAC and fully ZigBee compliant Freescale BeeStack.

2.1 Pin Definitions

Table 2 details the MC1321x pinout and functionality.

Table 2. Pin Function Description

Pin #	Pin Name	Type	Description	Functionality
1	PTA3/KBI1P3	Digital Input/Output	MCU Port A Bit 3 / Keyboard Input Bit 3	
2	PTA4/KBI1P4	Digital Input/Output	MCU Port A Bit 4 / Keyboard Input Bit 4	
3	PTA5/KBI1P5	Digital Input/Output	MCU Port A Bit 5 / Keyboard Input Bit 5	
4	PTA6/KBI1P6	Digital Input/Output	MCU Port A Bit 6 / Keyboard Input Bit 6	
5	PTA7/KBI1P7	Digital Input/Output	MCU Port A Bit 7 / Keyboard Input Bit 7	
6	VDDAD	Power Input	MCU power supply to ATD	Decouple to ground.
7	PTG0/BKGND/MS	Digital Input/Output/	MCU Port G Bit 0 / Background / Mode Select	PTG0 is output only. Pin is I/O when used as BDM function.
8	PTG1/XTAL	Digital Input/Output	MCU Port G Bit 1 / Crystal oscillator output	Full I/O when not used as clock source.
9	PTG2/EXTAL	Digital Input/Output/	MCU Port G Bit 2 / Crystal oscillator input	Full I/O when not used as clock source.
10	CLKO	Digital Output	Modem Clock Output	Programmable frequencies of: 16 MHz, 8 MHz, 4 MHz, 2 MHz, 1 MHz, 62.5 kHz, 32.786+ kHz (default), and 16.393+ kHz.
11	$\overline{\text{RESET}}$	Digital Input/Output	MCU reset. Active low	
12	PTC0/TXD2	Digital Input/Output	MCU Port C Bit 0 / SCI2 TX data out	
13	PTC1/RXD2	Digital Input/Output	MCU Port C Bit 1/ SCI2 RX data in	
14	PTC2/SDA1	Digital Input/Output	MCU Port C Bit 1/ IIC bus data	
15	PTC3/SCL1	Digital Input/Output	MCU Port C Bit 1/ IIC bus clock	
16	PTC4	Digital Input/Output	MCU Port C Bit 4	
17	PTC5	Digital Input/Output	MCU Port C Bit 5	
18	PTC6	Digital Input/Output	MCU Port C Bit 6	

Table 2. Pin Function Description (continued)

Pin #	Pin Name	Type	Description	Functionality
19	PTC7	Digital Input/Output	MCU Port C Bit 7	
20	PTE0/TXD1	Digital Input/Output	MCU Port E Bit 0 / SCI1 TX data out	
21	PTE1/RXD1	Digital Input/Output	MCU Port E Bit 1/ SCI1 RX data in	
22	VDDD	Power Output	Modem regulated output supply voltage	Decouple to ground.
23	VDDINT	Power Input	Modem digital interface supply	2.0 to 3.4 V. Decouple to ground. Connect to Battery.
24	GPIO5[1]	Digital Input/Output	General Purpose Input/Output 5.	See Footnote 1
25	GPIO6[1]	Digital Input/Output	Modem General Purpose Input/Output 6	See Footnote 1
26	GPIO7[1]	Digital Input/Output	Modem General Purpose Input/Output 7	See Footnote 1
27	XTAL1	Input	Modem crystal reference oscillator input	Connect to 16 MHz crystal and load capacitor.
28	XTAL2	Input/Output	Modem crystal reference oscillator output	Connect to 16 MHz crystal and load capacitor. Do not load this pin by using it as a 16 MHz source. Measure 16 MHz output at CLKO, programmed for 16 MHz.
29	VDDLO2	Power Input	Modem LO2 VDD supply	Connect to VDDA externally.
30	VDDLO1	Power Input	Modem LO1 VDD supply	Connect to VDDA externally.
31	VDDVCO	Power Output	Modem VCO regulated supply bypass	Decouple to ground.
32	VBATT	Power Input	Modem voltage regulators' input	Decouple to ground. Connect to Battery.
33	VDDA	Power Output	Modem analog regulated supply output	Decouple to ground. Connect to directly VDDLO1 and VDDLO2 externally and to PAO_P and PAO_M through a bias network.
34	CT_Bias	RF Control Output	Modem bias voltage/control signal for RF external components	When used with internal T/R switch, provides ground reference for RX and VDDA reference for TX. Can also be used as a control signal with external LNA, antenna switch, and/or PA (high level is VDDA).
35	RFIN_M	RF Input (Output)	Modem RF input/output negative	When used with internal T/R switch, this is a bi-directional RF port for the internal LNA and PA
36	RFIN_P	RF Input (Output)	Modem RF input/output positive	When used with internal T/R switch, this is a bi-directional RF port for the internal LNA and PA
37	NC		Not used	May be grounded or left open

2.2 Internal Functional Interconnects

The MCU provides control for the 802.15.4 modem. The required interconnects between the devices are routed onboard the SiP. In addition, the signals are brought out to external pads primarily for use as test points. These signals can be useful when writing and debugging software.

Table 3. Internal Functional Interconnects

Pin #	MCU Signal	Modem Signal	Description
43	PTE6	GPIO2	Modem GPIO2 output acts as “CRC Valid” status indicator for Stream Data Mode to MCU.
44	PTE7	GPIO1	Modem GPIO1 output acts as “Out of Idle” status indicator for Stream Data Mode to MCU.
46	PTD0	$\overline{\text{ATTN}}$	MCU Port D Bit 0 drives the attention ($\overline{\text{ATTN}}$) input of the modem to wake modem from Hibernate or Doze Mode.
	PTE5/SPSCK1	SPICLK[1]	MCU SPI master SPI clock output drives modem SPICLK slave clock input.
	PTE4/MOSI1	MOSI[1]	MCU SPI master MOSI output drives modem slave MOSI input
	PTE3/MISO1	MISO[2]	Modem SPI slave MISO output drives MCU master MISO input
	PTE2/$\overline{\text{SS1}}$	$\overline{\text{CE}}$[1]	MCU SPI master SS output drives modem slave $\overline{\text{CE}}$ input
	IRQ	$\overline{\text{M\_IRQ}}$	Modem interrupt request $\overline{\text{M\_IRQ}}$ output drives MCU IRQ input
	PTD1	RXTXEN[1]	MCU Port D Bit 1 drives the RXTXEN input to the modem to enable TX or RX or CCA operations.
	PTD3	$\overline{\text{M\_RST}}$	MCU Port D Bit 3 drives the reset $\overline{\text{M\_RST}}$ input to the modem.

1 During low power modes, input must remain driven by MCU.

2 By default MISO is tri-stated when $\overline{\text{CE}}$ is negated. For low power operation, miso_hiz_en (Bit 11, Register 07) should be set to zero so that MISO is driven low when $\overline{\text{CE}}$ is negated.

NOTE

To use the MCU and modem signals as described in Table 3, the MCU needs to be programmed appropriately for the stated function.

3 MC1321x Serial Peripheral Interface (SPI)

The MC1321x modem and CPU communicate primarily through the onboard SPI command channel. Figure 4 shows the SiP internal interconnects with the SPI bus highlighted. The MCU has a single SPI module that is dedicated to the modem SPI interface. The modem is a slave only and the MCU SPI must be programmed and used as a master only. Further, the SPI performance is limited by the modem constraints of 8 MHz SPI clock frequency, and use of the SPI must be programmed to meet the modem SPI protocol.

3.1 SiP Level SPI Pin Connections

The SiP level SPI pin connections are all internal to the device. Figure 4 shows the SiP interconnections with the SPI bus highlighted.

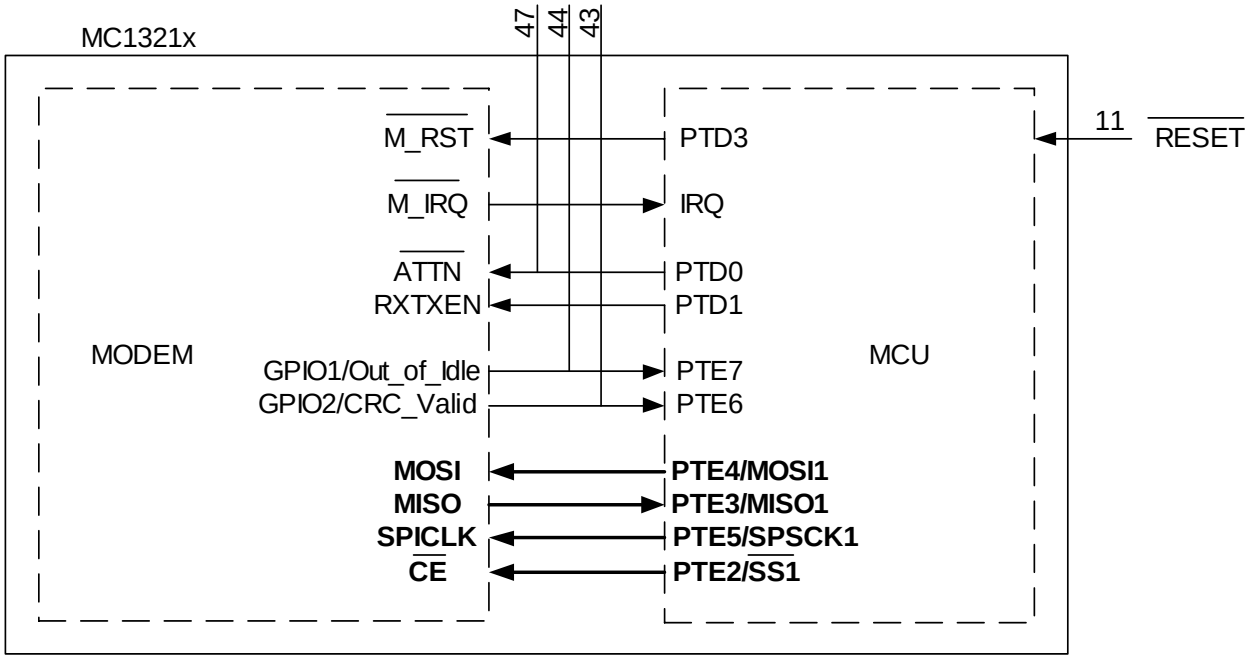


Figure 4. MC1321x Internal Interconnects Highlighting SPI Bus

Table 4. MC1321x Internal SPI Connections

MCU Signal	Modem Signal	Description
PTE5/SPSCK1	SPICLK	MCU SPI master SPI clock output drives modem SPICLK slave clock input.
PTE4/MOSI1	MOSI	MCU SPI master MOSI output drives modem slave MOSI input
PTE3/MISO1	MISO	Modem SPI slave MISO output drives MCU master MISO input
PTE2/$\overline{SS1}$	$\overline{CE}$	MCU SPI master SS output drives modem slave $\overline{CE}$ input

4 802.15.4 Standard Modem

4.1 Block Diagram

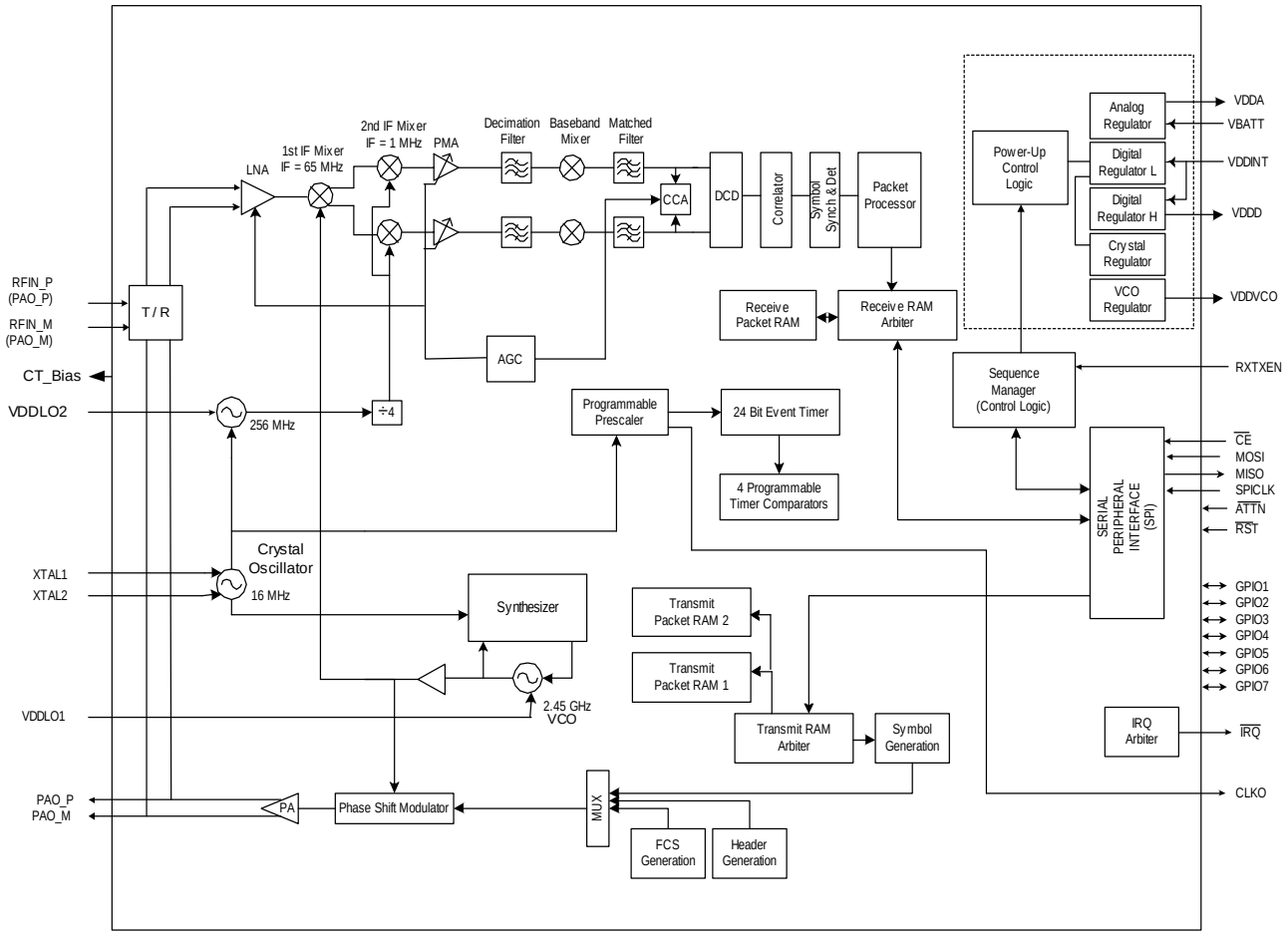


Figure 6. 802.15.4 Standard Modem Block Diagram

4.2 Data Transfer Modes

The 802.15.4 modem has two data transfer modes:

1. Packet Mode — Data is buffered in on-chip RAM
2. Streaming Mode — Data is processed word-by-word

The Freescale 802.15.4 MAC software only supports the streaming mode of data transfer. For proprietary applications, packet mode can be used to conserve MCU resources.

4.3 Packet Structure

Figure 7 shows the packet structure of the 802.15.4 modem. Payloads of up to 125 bytes are supported. The 802.15.4 modem adds a four-byte preamble, a one-byte Start of Frame Delimiter (SFD), and a one-byte Frame Length Indicator (FLI) before the data. A Frame Check Sequence (FCS) is calculated and appended to the end of the data.

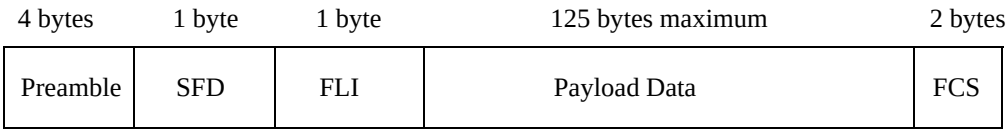


Figure 7. 802.15.4 modem Packet Structure

4.4 Receive Path Description

In the receive signal path, the RF input is converted to low IF In-phase and Quadrature (I & Q) signals through two down-conversion stages. A Clear Channel Assessment (CCA) can be performed based upon the baseband energy integrated over a specific time interval. The digital back end performs Differential Chip Detection (DCD), the correlator “de-spreads” the Direct Sequence Spread Spectrum (DSSS) Offset QPSK (O-QPSK) signal, determines the symbols and packets, and detects the data.

The preamble, SFD, and FLI are parsed and used to detect the payload data and FCS (which are stored in RAM in Packet Mode). A two-byte FCS is calculated on the received data and compared to the FCS value appended to the transmitted data, which generates a Cyclical Redundancy Check (CRC) result. A parameter of received energy during the reception called the Link Quality Indicator is measured over a 64 µs period after the packet preamble and stored in an SPI register.

If the 802.15.4 modem is in Packet Mode, the data is stored in RAM and processed as an entire packet. The MCU is notified that an entire packet has been received via an interrupt.

If the 802.15.4 modem is in streaming mode, the MCU is notified by a recurring interrupt on a word-by-word basis.

Figure 8 shows CCA reported power level versus input power. Note that CCA reported power saturates at about -57 dBm input power which is well above 802.15.4 Standard requirements.

4.6.2 Serial Peripheral Interface (SPI)

The MCU directs the 802.15.4 modem, checks its status, and reads/writes data to the device through the 4-wire SPI port. The transceiver operates as a SPI slave device only. A transaction between the host and the 802.15.4 modem occurs as multiple 8-bit bursts on the SPI. The modem SPI signals are:

1. Chip Enable ($\overline{CE}$) - A transaction on the SPI port is framed by the active low $\overline{CE}$ input signal. A transaction is a minimum of 3 SPI bursts and can extend to a greater number of bursts.
2. SPI Clock (SPICLK) - The host drives the SPICLK input to the 802.15.4 modem. Data is clocked into the master or slave on the leading (rising) edge of the return-to-zero SPICLK and data out changes state on the trailing (falling) edge of SPICLK.

NOTE

For the MCU, the SPI clock format is the clock phase control bit CPHA = 0 and the clock polarity control bit CPOL = 0.

3. Master Out/Slave In (MOSI) - Incoming data from the host is presented on the MOSI input.
4. Master In/Slave Out (MISO) - The 802.15.4 modem presents data to the master on the MISO output.

Although the SPI port is fully static, internal memory, timer and interrupt arbiters require an internal clock (CLK_{core}), derived from the crystal reference oscillator, to communicate from the SPI registers to internal registers and memory.

4.6.2.1 SPI Burst Operation

The SPI port of the MCU transfers data in bursts of 8 bits with most significant bit (MSB) first. The master (MCU) can send a byte to the slave (transceiver) on the MOSI line and the slave can send a byte to the master on the MISO line. Although an 802.15.4 modem transaction is three or more SPI bursts long, the timing of a single SPI burst is shown in Figure 10. The maximum SPI clock rate is 8 Mhz from the MCU because the modem is limited by this number.

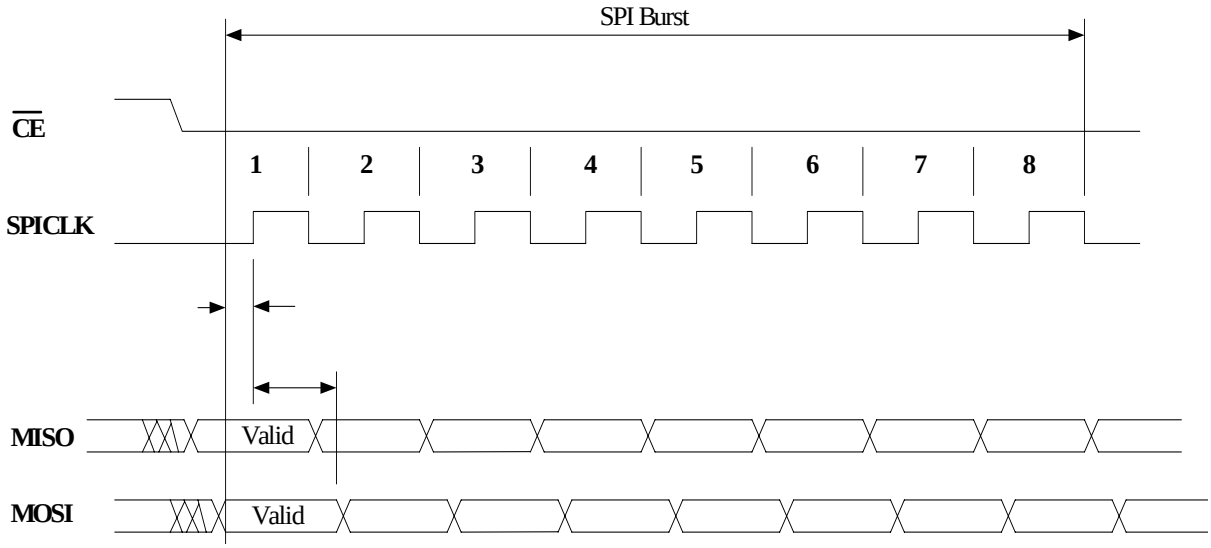
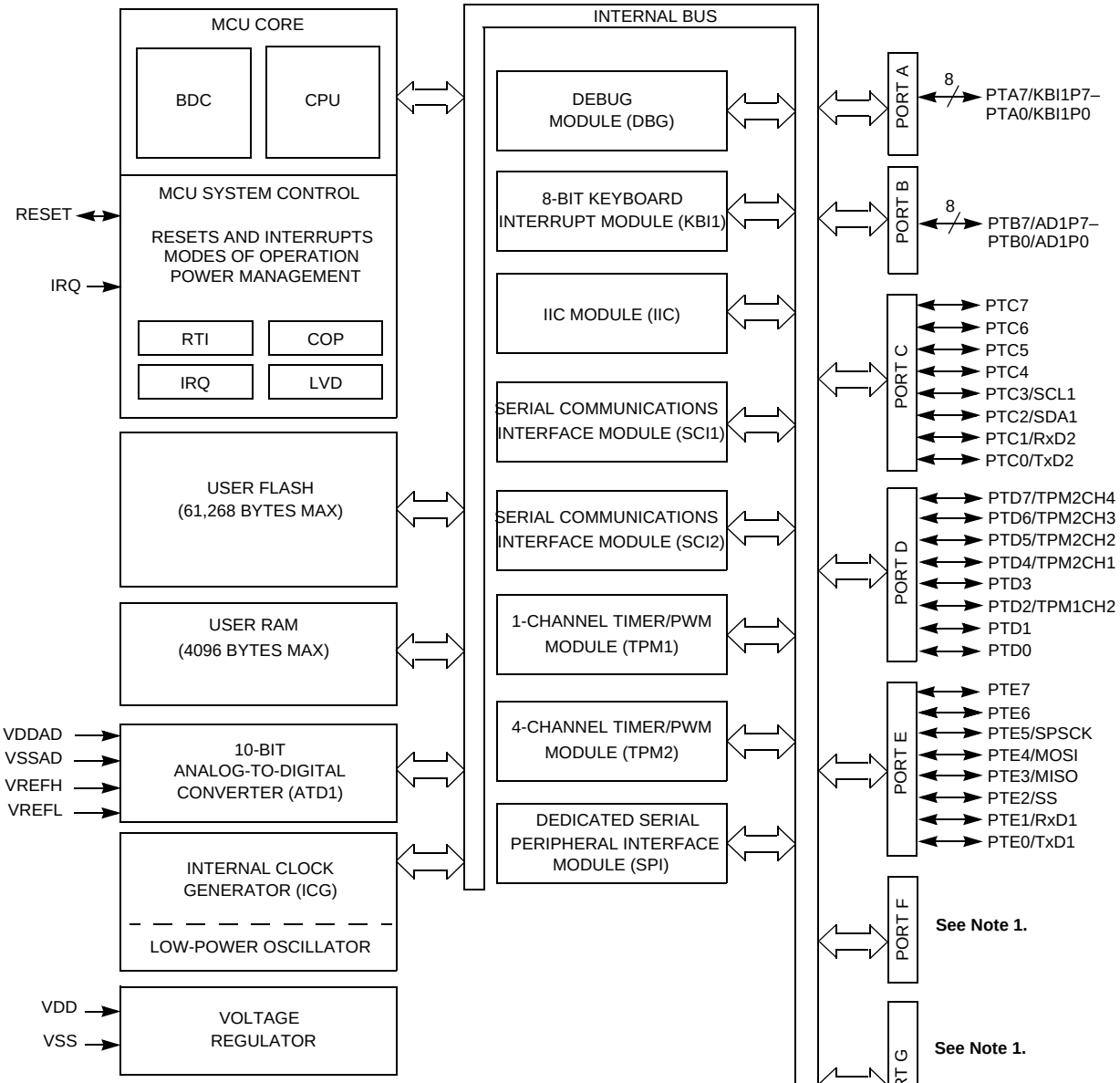


Figure 10. SPI Single Burst Timing Diagram

5 MCU

5.1 MCU Block Diagram



Notes
1. All Port F and Port G signals are present on the MCU, but only the signals used by the MC1321x are designated. For lowest power operation, all unused I/O should be programmed as outputs during initialization.

2. Timer channels are limited as noted due to use of Port D I/O for internal signals.

Figure 15. MCU Block Diagram (HCS08, Version A)

Before entering Stop2 Mode, the user must save the contents of the I/O port registers, as well as any other memory-mapped registers they want to restore after exit of Stop2, to locations in RAM. Upon exit of Stop2, these values can be restored by user software before pin latches are opened.

When the MCU is in Stop2 Mode, all internal circuits that are powered from the voltage regulator are turned off, except for the RAM. The voltage regulator is in a low-power standby state, as is the ATD. Upon entry into Stop2, the states of the I/O pins are latched. The states are held while in Stop2 Mode and after exiting Stop2 Mode until a 1 is written to PPDACK in SPMSC2.

Exit from Stop2 is performed by asserting either of the wake-up pins: $\overline{\text{RESET}}$ or IRQ, or by an RTI interrupt. IRQ is always an active low input when the MCU is in Stop2, regardless of how it was configured before entering Stop2.

Upon wake-up from Stop2 Mode, the MCU will start up as from a power-on reset (POR) except pin states remain latched. The CPU will take the reset vector. The system and all peripherals will be in their default reset states and must be initialized.

After waking up from Stop2, the PPDF bit in SPMSC2 is set. This flag may be used to direct user code to go to a Stop2 recovery routine. PPDF remains set and the I/O pin states remain latched until a 1 is written to PPDACK in SPMSC2.

To maintain I/O state for pins that were configured as general-purpose I/O, the user must restore the contents of the I/O port registers, which have been saved in RAM, to the port registers before writing to the PPDACK bit. If the port registers are not restored from RAM before writing to PPDACK, then the register bits will assume their reset states when the I/O pin latches are opened and the I/O pins will switch to their reset states.

For pins that were configured as peripheral I/O, the user must reconfigure the peripheral module that interfaces to the pin before writing to the PPDACK bit. If the peripheral module is not enabled before writing to PPDACK, the pins will be controlled by their associated port control registers when the I/O latches are opened.

A separate self-clocked source (approximately 1 kHz) for the real-time interrupt allows a walk-up from Stop2 or Stop3 Modes with no external components. When RTIS2:RTIS1:RTIS0 = 0:0:0, the real-time interrupt function and this 1-kHz source are disabled. Power consumption is lower when the 1-kHz source is disabled, but in that case the real-time interrupt cannot wake the MCU from stop.

5.2.4 Stop3

Upon entering the Stop3 Mode, all of the clocks in the MCU, including the oscillator itself, are halted. The ICG is turned off, the ATD is disabled, and the voltage regulator is put in standby. The states of all of the internal registers and logic, as well as the RAM content, are maintained. The I/O pin states are not latched at the pin as in Stop2. Instead they are maintained by virtue of the states of the internal logic driving the pins being maintained.

Exit from Stop3 is performed by asserting $\overline{\text{RESET}}$, an asynchronous interrupt pin, or through the real-time interrupt. The asynchronous interrupt pins are the IRQ or KBI pins.

5.4 MCU Internal Clock Generator (ICG)

The ICG provides multiple options for MCU clock sources. This block along with the ability to provide the MCU clock form the modem offers a user great flexibility when making choices between cost, precision, current draw, and performance. As seen in Figure 17, the ICG consists of four functional blocks.

- **Oscillator Block** — The Oscillator Block provides means for connecting an external crystal or resonator. Two frequency ranges are software selectable to allow optimal start-up and stability. Alternatively, the oscillator block can be used to route an external square wave to the MCU system clock. External sources such as the modem CLKO output can provide a low cost source or a very precise clock source. The oscillator is capable of being configured for low power mode or high amplitude mode as selected by HGO.
- **Internal Reference Generator** — The Internal Reference Generator consists of two controlled clock sources. One is designed to be approximately 8 MHz and can be selected as a local clock for the background debug controller. The other internal reference clock source is typically 243 kHz and can be trimmed for finer accuracy via software when a precise timed event is input to the MCU. This provides a highly reliable, low-cost clock source.
- **Frequency-Locked Loop** — A Frequency-Locked Loop (FLL) stage takes either the internal or external clock source and multiplies it to a higher frequency. Status bits provide information when the circuit has achieved lock and when it falls out of lock. Additionally, this block can monitor the external reference clock and signals whether the clock is valid or not.
- **Clock Select Block** — The Clock Select Block provides several switch options for connecting different clock sources to the system clock tree. ICGDCLK is the multiplied clock frequency out of the FLL, ICGERCLK is the reference clock frequency from the crystal or external clock source, and FFE (fixed frequency enable) is a control signal used to control the system fixed frequency clock (XCLK). ICGLCLK is the clock source for the background debug controller (BDC).

The module is intended to be very user friendly with many of the features occurring automatically without user intervention.

5.4.1 Features

Features of the ICG and clock distribution system:

- Several options for the MCU primary clock source allow a wide range of cost, frequency, and precision choices:
  - 32 kHz–100 kHz crystal or resonator
  - 1 MHz–16 MHz crystal or resonator
  - External clock supplied by modem CLKO or other source
  - Internal reference generator
- Defaults to self-clocked mode to minimize startup delays
- Frequency-locked loop (FLL) generates 8 MHz to 40 MHz (for bus rates up to 20 MHz). When using modem CLKO as external source, maximum FLL frequency is 32 MHz (16 MHz bus rate) with CLKO = 16 MHz or maximum FLL frequency is 40 MHz (20 MHz bus rate) with CLKO = 4 MHz.

— Uses external or internal clock as reference frequency

- Automatic lockout of non-running clock sources
- Reset or interrupt on loss of clock or loss of FLL lock
- Digitally-controlled oscillator (DCO) preserves previous frequency settings, allowing fast frequency lock when recovering from stop3 mode
- DCO will maintain operating frequency during a loss or removal of reference clock. When FLL is engaged (FEE or FEI) loss of lock or loss of clock adds a divide-by-2 to ICG to prevent over-clocking of the system.
- Post-FLL divider selects 1 of 8 bus rate divisors (/1 through /128)
- Separate self-clocked source for real-time interrupt
- Trimmable internal clock source supports SCI communications without additional external components
- Automatic FLL engagement after lock is acquired
- Selectable low-power/high-gain oscillator modes

5.4.2 Modes of Operation

This section provides a high-level description only.

- Mode 1 — Off

  The output clock, ICGOUT, is static. This mode may be entered when the STOP instruction is executed.
- Mode 2 — Self-clocked (SCM)

  Default mode of operation that is entered out of reset. The ICG's FLL is open loop and the digitally controlled oscillator (DCO) is free running at a frequency set by the filter bits.
- Mode 3 — FLL engaged internal (FEI)

  In this mode, the ICG's FLL is used to create frequencies that are programmable multiples of the internal reference clock.
  - FLL engaged internal unlocked is a transition state which occurs while the FLL is attempting to lock. The FLL DCO frequency is off target and the FLL is adjusting the DCO to match the target frequency.
  - FLL engaged internal locked is a state which occurs when the FLL detects that the DCO is locked to a multiple of the internal reference.
- Mode 4 — FLL bypassed external (FBE)

  In this mode, the ICG is configured to bypass the FLL and use an external clock as the clock source.
- Mode 5 — FLL engaged external (FEE)

  The ICG's FLL is used to generate frequencies that are programmable multiples of the external clock reference.
  - FLL engaged external unlocked is a transition state which occurs while the FLL is attempting to lock. The FLL DCO frequency is off target and the FLL is adjusting the DCO to match the target frequency.

- Inherent — Operands in internal registers
- Relative — 8-bit signed offset to branch destination
- Immediate — Operand in next object code byte(s)
- Direct — Operand in memory at 0x0000–0x00FF
- Extended — Operand anywhere in 64-Kbyte address space
- Indexed relative to H:X — Five submodes including auto increment
- Indexed relative to SP — Improves C efficiency dramatically

- Memory-to-memory data move instructions with four address mode combinations
- Overflow, half-carry, negative, zero, and carry condition codes support conditional branching on the results of signed, unsigned, and binary-coded decimal (BCD) operations
- Efficient bit manipulation instructions
- Fast 8-bit by 8-bit multiply and 16-bit by 8-bit divide instructions
- STOP and WAIT instructions to invoke low-power operating modes

5.5.2 Programmer's Model and CPU Registers

Figure 18 shows the five CPU registers. CPU registers are not part of the memory map.

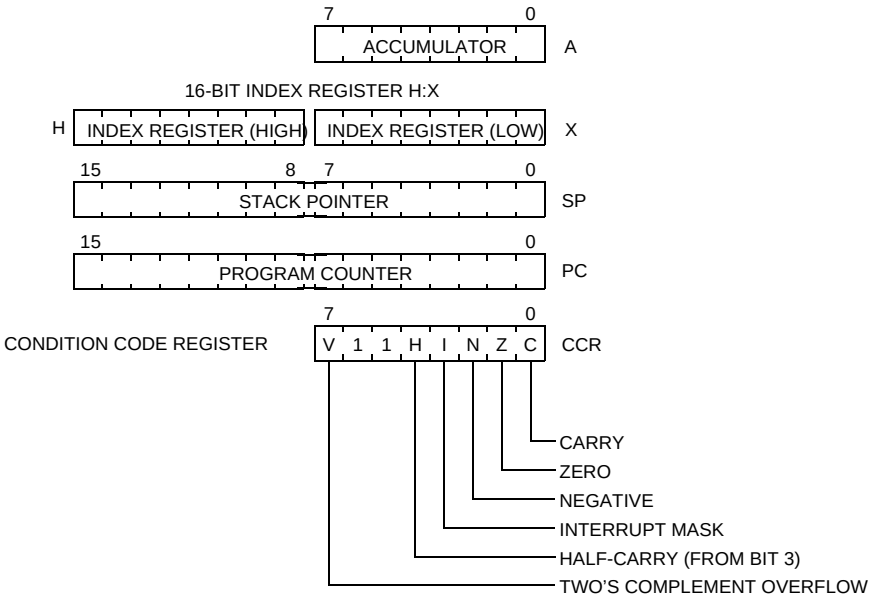


Figure 18. CPU Registers

5.6 Parallel Input/Output

The MC1321x HCS08 has seven I/O ports which include a total of 56 general-purpose I/O signals (one of these pins, PTG0, is output only). The MC1321x family does not use all the these signals as denoted in Figure 15. Port F and part of port G are not utilized. The MC1321x family makes use of the remaining I/O as pinned-out I/O or as internally dedicated signal for communication with the 802.15.4 modem.

As stated above port F and part of port G are not utilized. These signals and any unused IO should be programmed as outputs during initialization for lowest power operation. Many of these pins are shared with on-chip peripherals such as timer systems, various communication ports, or keyboard interrupts. When these other modules are not controlling the port pins, they revert to general-purpose I/O control. For each I/O pin, a port data bit provides access to input (read) and output (write) data, a data direction bit controls the direction of the pin, and a pullup enable bit enables an internal pullup device (provided the pin is configured as an input), and a slew rate control bit controls the rise and fall times of the pins.Parallel I/O features include:

- A total of 32 general-purpose I/O pins in seven ports (PTG0 is output only)
- High-current drivers on port C
- Hysteresis input buffers
- Software-controlled pullups on each input pin
- Software-controlled slew rate output buffers
- Eight port A pins shared with KBI1
- Eight port B pins shared with ATD1
- Eight high-current port C pins shared with SCI2 and IIC1
- Eight port D pins shared with TPM1 and TPM2
- Eight port E pins shared with SCI1 and SPI1
- Eight port G pins shared with EXTAL, XTAL, and BKGD/MS

NOTE

Not all port G signals and no port F signals are bonded out, but are present in the MCU hardware (see Figure 15). These port I/O signals should be programmed as outputs set to the low state.

5.7 MCU Peripherals

5.7.1 Modem Dedicated Serial Peripheral Interface (SPI) Module

The HCS08 provides one serial peripheral interface (SPI) module which is connected within the SiP to the modem SPI port. The four pins associated with SPI functionality are shared with port E pins 2–5. When the SPI is enabled, the direction of pins is controlled by module configuration.

The MCU SPI port is used only in master mode on the MC1321x family. The user must program the SPI module for the proper characteristics as listed in the features below and also program the $\overline{SS}$ signal to have the proper use to support the modem transaction protocol for the modem $\overline{CE}$ signal.

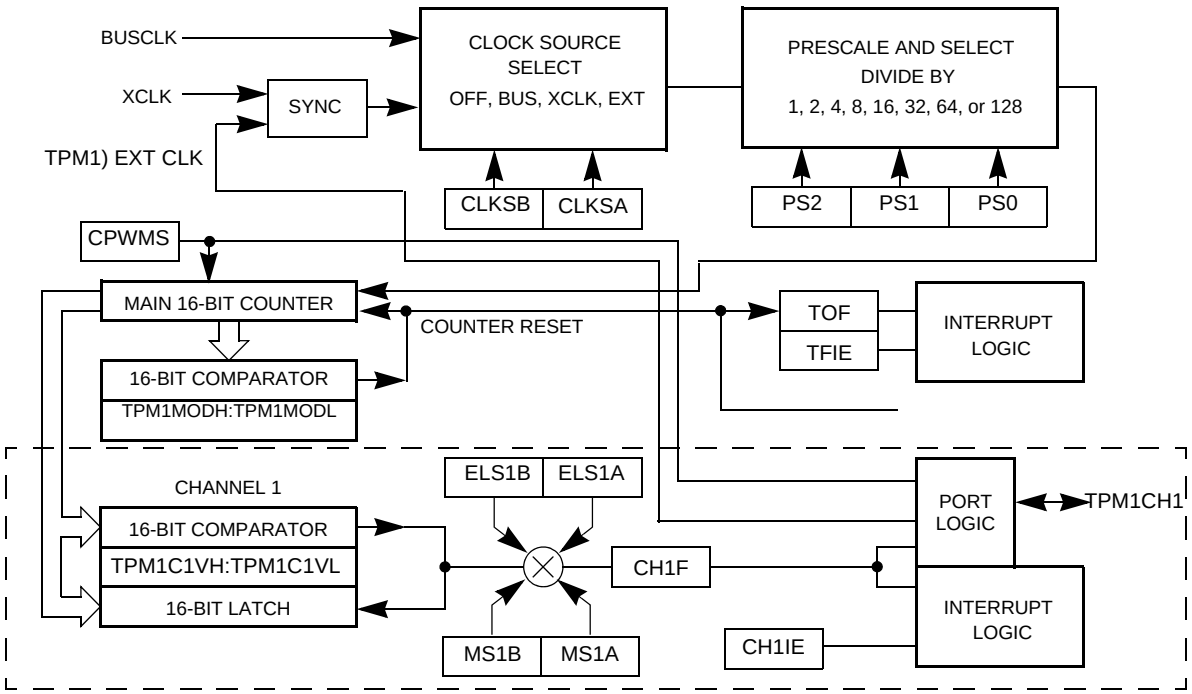


Figure 21. TPM Block Diagram

5.7.5 Serial Communications Interface (SCI) Module

The HCS08 includes two independent serial communications interface (SCI) modules — sometimes called universal asynchronous receiver/transmitters (UARTs). Typically, these systems are used to connect to the RS232 serial input/output (I/O) port of a personal computer or workstation, and they can also be used to communicate with other embedded controllers.

A flexible, 13-bit, modulo-based baud rate generator supports a broad range of standard baud rates beyond 115.2 kbaud. Transmit and receive within the same SCI use a common baud rate, and each SCI module has a separate baud rate generator.

This SCI system offers many advanced features not commonly found on other asynchronous serial I/O peripherals on other embedded controllers. The receiver employs an advanced data sampling technique that ensures reliable communication and noise detection. Hardware parity, receiver wakeup, and double buffering on transmit and receive are also included.

5.7.5.1 SCI Features

Features of SCI module include:

- Full-duplex, standard non-return-to-zero (NRZ) format
- Double-buffered transmitter and receiver with separate enables
- Programmable baud rates (13-bit modulo divider)
- Interrupt-driven or polled operation:
  - Transmit data register empty and transmission complete

Table 9. Receiver AC Electrical Characteristics

(V_{BATT}, V_{DDINT} = 2.7 V, T_A = 25 °C, f_{ref} = 16 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Error Tolerance		-	-	200	kHz
Symbol Rate Error Tolerance		-	-	80	ppm

Table 10. Transmitter AC Electrical Characteristics

(V_{BATT}, V_{DDINT} = 2.7 V, T_A = 25 °C, f_{ref} = 16 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Spectral Density (-40 to +85 °C) Absolute limit		-	-47	-	dBm
Power Spectral Density (-40 to +85 °C) Relative limit		-	47	-	
Nominal Output Power[1]	P_{out}	-4	0	2	dBm
Maximum Output Power[2]			3		dBm
Error Vector Magnitude	EVM	-	18	35	%
Ouput Power Control Range		-	30	-	dB
Over the Air Data Rate		-	250	-	kbps
2nd Harmonic[3]		-	-48	-	dBc
3rd Harmonic[3]		-	-70	-	dBc

1 SPI Register 12 is default value of 0x00BC which sets output power to nominal (-1 dBm typical).

2 SPI Register 12 programmed to 0xFF which sets output power to maximum.

3 Measured with output power set to nominal (0 dBm) and temperature @ 25 °C

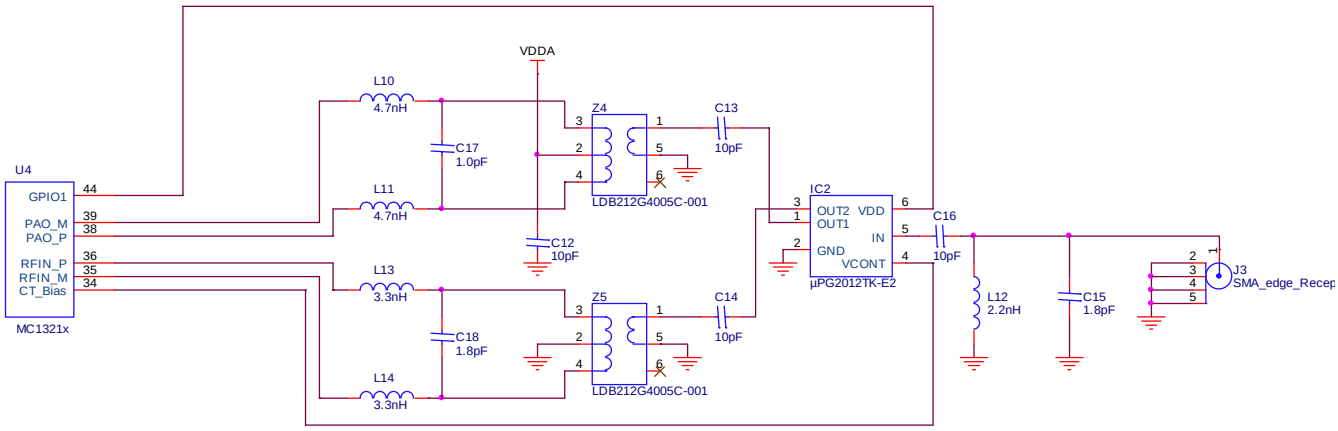


Figure 26. RF Parametric Evaluation Circuit

Table 17. MCU ICG Frequency Specifications (continued)
(V_{DDA} = V_{DDA} (min) to V_{DDA} (max), Temperature Range = –40 to 85°C Ambient)

Characteristic	Symbol	Min	Typical	Max	Unit
ICGOUT period jitter, [4, 7] measured at f_{ICGOUT} Max Long term jitter (averaged over 2 ms interval)	C_{Jitter}	 —		 0.2	% f_{ICG}
Internal oscillator deviation from trimmed frequency V_{DD} = 1.8 – 3.6 V, (constant temperature) V_{DD} = 3.0 V ±10%, –40° C to 85° C	ACC_{int}	 — —	 ±0.5 ±0.5	 ±2 ±2	%

1 Self-clocked mode frequency is the frequency that the DCO generates when the FLL is open-loop.

2 Loss of reference frequency is the reference frequency detected internally, which transitions the ICG into self-clocked mode if it is not in the desired range.

3 Loss of DCO frequency is the DCO frequency detected internally, which transitions the ICG into FLL bypassed external mode (if an external reference exists) if it is not in the desired range.

4 This parameter is characterized before qualification rather than 100% tested.

5 Proper PC board layout procedures must be followed to achieve specifications.

6 This specification applies to the period of time required for the FLL to lock after entering FLL engaged internal or external modes. If a crystal/resonator is being used as the reference, this specification assumes it is already running.

7 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{ICGOUT}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DDA} and V_{SSA} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

6.4 MCU AC Peripheral Characteristics

This section describes ac timing characteristics for each peripheral system.

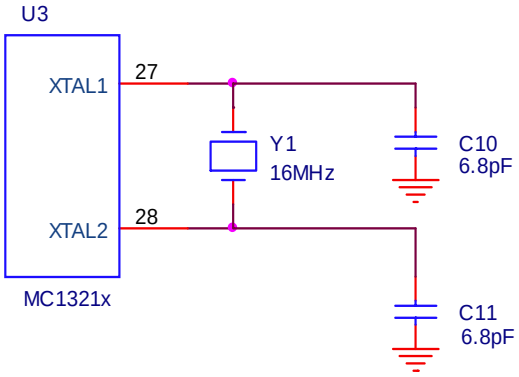
6.4.1 MCU Control Timing

Table 18. MCU Control Timing

Parameter	Symbol	Min	Typical	Max	Unit
Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	20	MHz
Real-time interrupt internal oscillator period	t_{RTI}	700		1300	µs
External reset pulse width[1]	t_{extrst}	1.5 x f_{Self_reset}		—	ns
Reset low drive[2]	t_{rstdrv}	34 x f_{Self_reset}		—	ns
Active background debug mode latch setup time	t_{MSSU}	25		—	ns
Active background debug mode latch hold time	t_{MSH}	25		—	ns
IRQ pulse width[3]	t_{ILIH}	1.5 x t_{cyc}		—	ns
Port rise and fall time (load = 50 pF)[4] Slew rate control disabled Slew rate control enabled	t_{Rise}, t_{Fall}	 — —	 3 30		ns

Since the MC1321x contains an on-chip reference frequency trim capability, it is possible to trim out virtually all of the initial tolerance factors and put the frequency within 0.12 ppm on a board-by-board basis. Individual trimming of each board in a production environment allows use of the lowest cost crystal, but requires that each board go through a trimming procedure. This step can be avoided by using/specifying a crystal with a tighter stability tolerance, but the crystal will be slightly higher in cost.

A tolerance analysis budget may be created using all the previously stated factors. It is an engineering judgment whether the worst case tolerance will assume that all factors will vary in the same direction or if the various factors can be statistically rationalized using RSS (Root-Sum-Square) analysis. The aging factor is usually specified in ppm/year and the product designer can determine how many years are to be assumed for the product lifetime. Taking all of the factors into account, the product designer can determine the needed specifications for the crystal and external load capacitors to meet the 802.15.4 Standard.



Y1 = Daishinku KDS - DSX321G ZD00882

Figure 34. MC1321x Modem Crystal Circuit

7.1.2 Crystal Requirements

The suggested crystal specification for the MC1321x is shown in Table 22. A number of the stated parameters are related to desired package, desired temperature range and use of crystal capacitive load trimming. For more design details and suggested crystals, see application note *AN3251, Reference Oscillator Crystal Requirements for MC1319x, MC1320x, and MC1321x.*

Table 22. MC1321x Crystal Specifications[1]

Parameter	Value	Unit	Condition
Frequency	16.000000	MHz	
Frequency tolerance (cut tolerance)[2]	± 10	ppm	at 25 °C
Frequency stability (temperature drift)[3]	± 15	ppm	Over desired temperature range
Aging[4]	± 2	ppm	max
Equivalent series resistance[5]	43	Ω	max
Load capacitance[6]	5 - 9	pF	

8 Mechanical Diagrams

Figure 37 and Figure 38 show the MC1321x mechanical information.

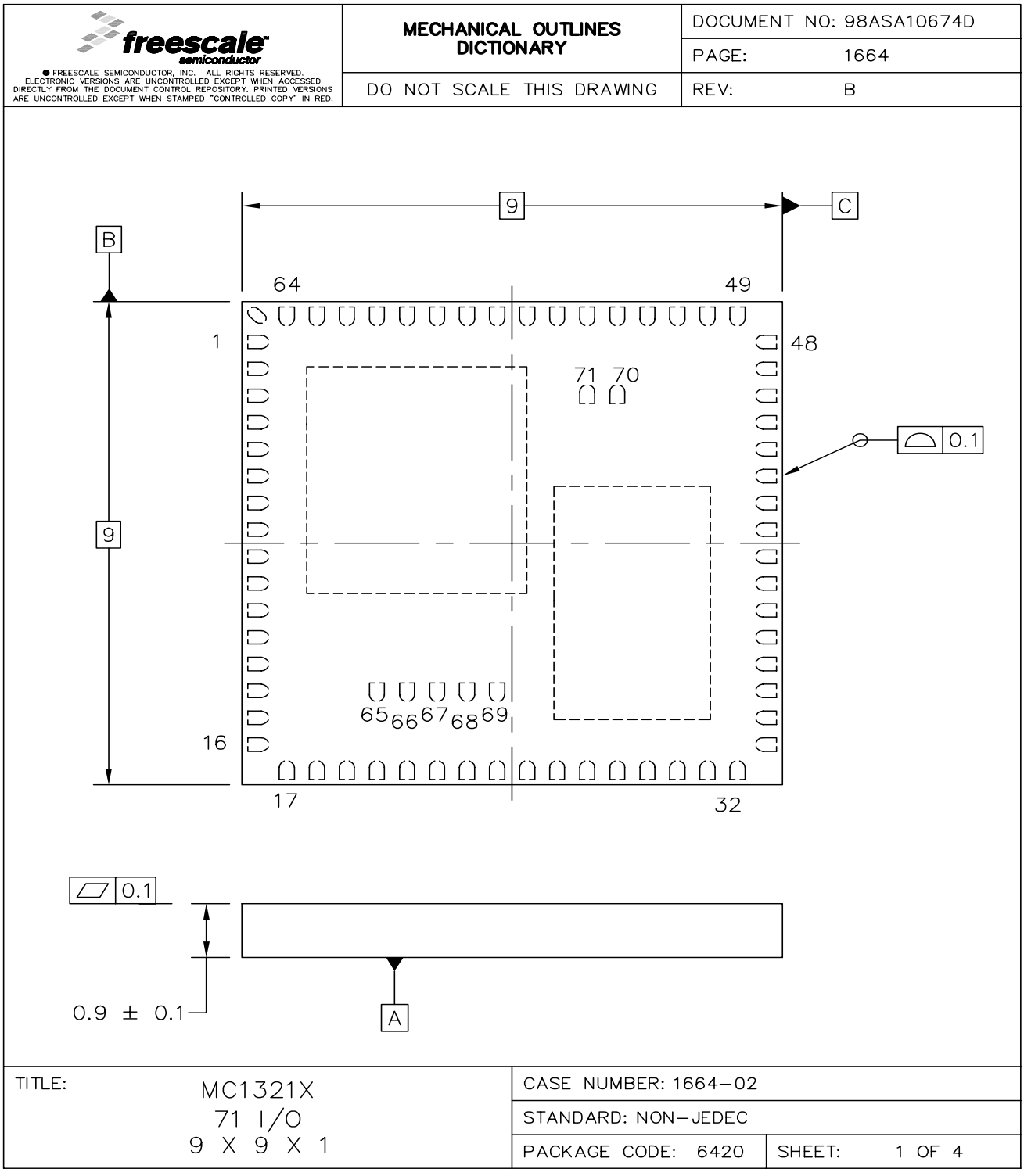


Figure 37. MC1321x Mechanical (1 of 2)

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