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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | AVR |
| Core Size | 8-Bit |
| Speed | 6MHz |
| Connectivity | SPI, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 32 |
| Program Memory Size | 128KB (64K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TQFP |
| Supplier Device Package | 64-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atmega103-6ai |

## Description

The ATmega103(L) is a low-power, CMOS, 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega103(L) achieves throughputs approaching 1 MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed.

The AVR core is based on an enhanced RISC architecture that combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega103(L) provides the following features: 128K bytes of In-System Programmable Flash, 4K bytes EEPROM, 4K bytes SRAM, 32 general purpose I/O lines, 8 input lines, 8 output lines, 32 general purpose working registers, Real Time Counter (RTC), 4 flexible Timer/Counters with compare modes and PWM, UART, programmable Watchdog Timer with internal Oscillator, an SPI serial port and 3 software-selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next Interrupt or Hardware Reset. In Power-save mode, the Timer Oscillator continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The On-chip ISP Flash allows the Program memory to be reprogrammed In-System through a serial interface or by a conventional nonvolatile memory programmer. By combining an 8-bit RISC CPU with a large array of ISP Flash on a monolithic chip, the Atmel ATmega103(L) is a powerful microcontroller that provides a highly flexible and cost-effective solution to many embedded control applications.

The ATmega103(L) AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, In-Circuit Emulators and evaluation kits.

Program execution continues at address PC + k + 1. The relative address k is -2048 to 2047.

## EEPROM Data Memory

The EEPROM memory is organized as a separate Data space in which single bytes can be read and written. The EEPROM has an endurance of at least 100,000 write/erase cycles. The access between the EEPROM and the CPU is described on page 57 specifying the EEPROM Address Register, the EEPROM Data Register and the EEPROM Control Register.

## Memory Access Times and Instruction Execution Timing

This section describes the general access timing concepts for instruction execution and internal memory access.

The AVR CPU is driven by the System Clock Ø, directly generated from the external clock crystal for the chip. No internal clock division is used.

Figure 20 shows the parallel instruction fetches and instruction executions enabled by the Harvard architecture and the fast-access Register File concept. This is the basic pipelining concept to obtain up to 1 MIPS per MHz with the corresponding unique results for functions per cost, functions per clocks and functions per power unit.

**Figure 20.** The Parallel Instruction Fetches and Instruction Executions

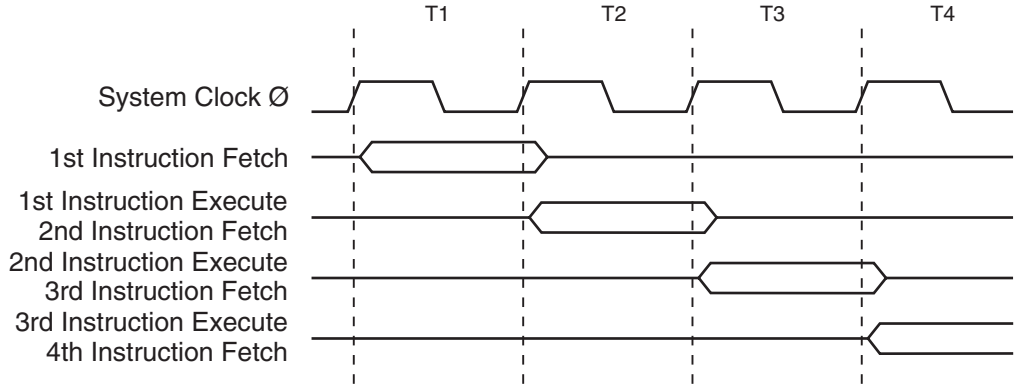



Figure 21 shows the internal timing concept for the Register File. In a single clock cycle, an ALU operation using two register operands is executed and the result is stored back to the destination register.

**Figure 21.** Single Cycle ALU Operation

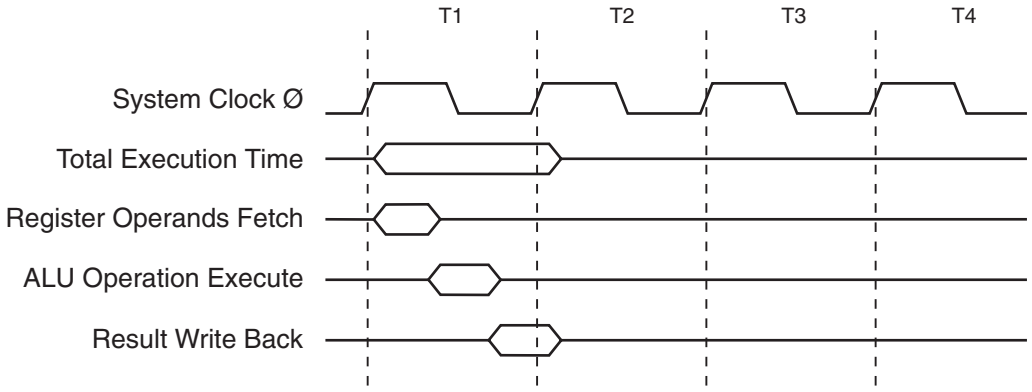
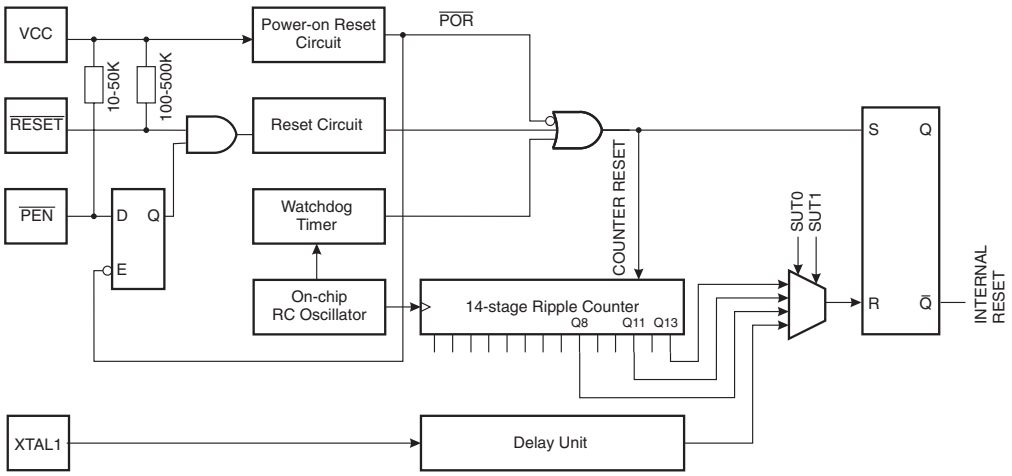


**Figure 23.** Reset Logic



an external or Watchdog reset occurs, the source of reset can be found by using the following truth table, Table 8.

**Table 8.** Reset Source Identification

| Reset Source | EXTRF | PORF |
|---|---|---|
| Watchdog Reset | 0 | 0 |
| Power-on Reset | 0 | 1 |
| External Reset | 1 | 0 |
| Power-on Reset | 1 | 1 |

## Interrupt Handling

The ATmega103(L) has two dedicated 8-bit Interrupt Mask Control Registers; EIMSK (External Interrupt Mask Register) and TIMSK (Timer/Counter Interrupt Mask Register). In addition, other enable and mask bits can be found in the peripheral control registers.

When an interrupt occurs, the Global Interrupt Enable I-bit is cleared (zero) and all interrupts are disabled. The user software can set (one) the I-bit to enable nested interrupts. The I-bit is set (one) when a Return from Interrupt instruction (RETI) is executed.

When the Program Counter is vectored to the actual Interrupt Vector in order to execute the interrupt handling routine, hardware clears the corresponding flag that generated the interrupt. Some of the Interrupt Flags can also be cleared by writing a logical “1” to the flag bit position(s) to be cleared.

If an interrupt condition occurs when the corresponding interrupt enable bit is cleared (zero), the Interrupt Flag will be set and remembered until the interrupt is enabled or the flag is cleared by software.

If one or more interrupt conditions occur when the Global Interrupt Enable bit is cleared (zero), the corresponding Interrupt Flag(s) will be set and remembered until the Global Interrupt Enable bit is set (one), and will be executed by order of priority.

Note that external level interrupt does not have a flag and will only be remembered for as long as the interrupt condition is active.

Note that the Status Register is not automatically stored when entering an interrupt routine or restored when returning from an interrupt routine. This must be handled by software.

## External Interrupt Mask Register – EIMSK

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| $39 ($59) | INT7 | INT6 | INT5 | INT4 | INT3 | INT2 | INT1 | INT0 | EIMSK |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

- **Bits 7..4 – INT7 - INT4: External Interrupt Request 7 - 4 Enable**

When an INT7 - INT4 bit is set (one) and the I-bit in the Status Register (SREG) is set (one), the corresponding external pin interrupt is enabled. The Interrupt Sense Control bits in the External Interrupt Control Register (EICR) define whether the external interrupt is activated on rising or falling edge or is level-sensed. Activity on any of these pins will trigger an interrupt request even if the pin is enabled as an output. This provides a way of generating a software interrupt.

- **Bit 0 – TOIE0: Timer/Counter0 Overflow Interrupt Enable**

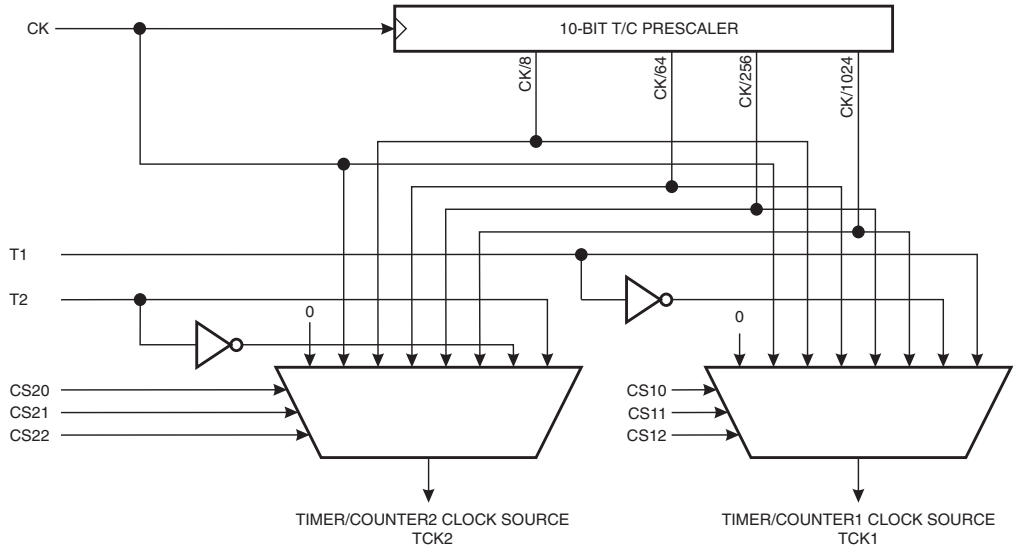
When the TOIE0 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter0 Overflow interrupt is enabled. The corresponding interrupt (at vector $0020) is executed if an overflow in Timer/Counter0 occurs, i.e., when the TOV0 bit is set in the Timer/Counter Interrupt Flag Register.

## Timer/Counters

The ATmega103(L) provides three general purpose Timer/Counters – two 8-bit T/Cs and one 16-bit T/C. Timer/Counter0 optionally can be asynchronously clocked from an external Oscillator. This Oscillator is optimized for use with a 32.768 kHz crystal, enabling use of Timer/Counter0 as a Real Time Clock (RTC). Timer/Counter0 has its own prescaler. Timer/Counters 1 and 2 have individual prescaling selection from the same 10-bit prescaling timer. These Timer/Counters can either be used as a Timer with an internal clock time base or as a counter with an external pin connection that triggers the counting.

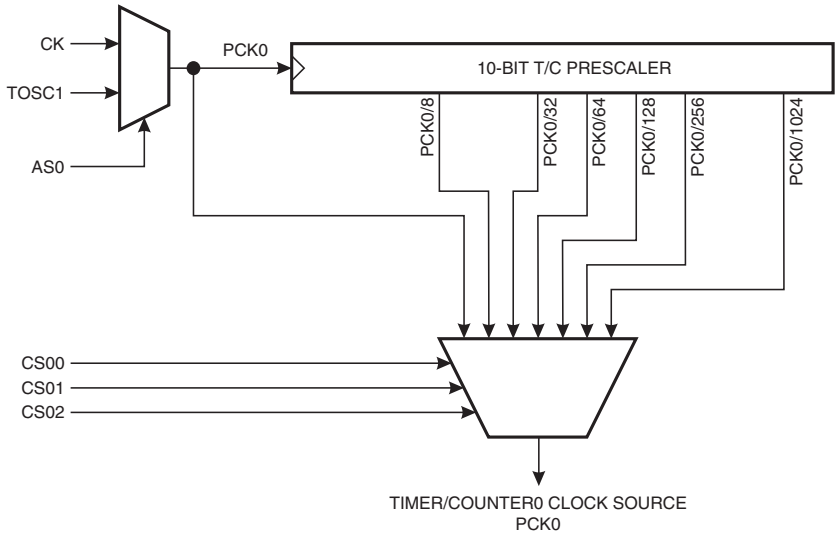
## Timer/Counter Prescalers

**Figure 28.** Prescaler for Timer/Counter1 and Timer/Counter2




For Timer/Counters 1 and 2, the four different prescaled selections are: CK/8, CK/64, CK/256 and CK/1024, where CK is the CPU clock. Observe that CPU clock frequency can be lower than the XTAL frequency if the XTAL divider is enabled. For Timer/Counters 1 and 2, added selections as CK, external source and stop can be selected as clock sources.

**Figure 29.** The Timer/Counter0 Prescaler



### Timer/Counter0 Control Register – TCCR0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| 33 ($53) | – | PWM0 | COM01 | COM00 | CTC0 | CS02 | CS01 | CS00 | TCCR0 |
| Read/Write | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

### Timer/Counter2 Control Register – TCCR2

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| $25 ($45) | – | PWM2 | COM21 | COM20 | CTC2 | CS22 | CS21 | CS20 | TCCR2 |
| Read/Write | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

- **Bit 7 – Res: Reserved Bit**

This bit is a reserved bit in the ATmega103(L) and always reads as zero.

- **Bit 6 – PWM0/PWM2: Pulse Width Modulator Enable**

When set (one), this bit enables PWM mode for Timer/Counter0 or Timer/Counter2. This mode is described on page 43.

- **Bits 5, 4 – COM01, COM00/COM21, COM20: Compare Output Mode, Bits 1 and 0**

The COMn1 and COMn0 control bits determine any output pin action following a compare match in Timer/Counter2. Any output pin actions affect pins PB4 (OC0/PWM0) or PB7 (OC2/PWM2). Since this is an alternative function to an I/O port, the corresponding direction control bit must be set (one) to control an output pin. The control configuration is shown in Table 10.

**Table 10.** Compare Mode Select

| COMn1 | COMn0 | Description |
|---|---|---|
| 0 | 0 | Timer/Counter disconnected from output pin OCn/PWMn |
| 0 | 1 | Toggle the OCn/PWMn output line. |
| 1 | 0 | Clear the OCn/PWMn output line (to zero). |
| 1 | 1 | Set the OCn/PWMn output line (to one). |

Note: n = 0 or 2
In PWM mode, these bits have a different function. Refer to Table 13 for a detailed description.

- **Bit 3 – CTC0/CTC2: Clear Timer/Counter on Compare Match**

When the CTC0 or CTC2 control bit is set (one), the Timer/Counter is reset to $00 in the CPU clock cycle after a compare match. If the control bit is cleared, the Timer continues counting and is unaffected by a compare match. Since the compare match is detected in the CPU clock cycle following the match, this function will behave differently when a prescaling higher than 1 is used for the Timer. When a prescaling of 1 is used and the Compare Register is set to C, the Timer will count as follows if CTC0/2 is set:

... | C-2 | C-1 | C | 0 | 1 | ...

When the prescaler is set to divide by 8, the Timer will count like this:

... | C-2, C-2, C-2, C-2, C-2, C-2, C-2, C-2 | C-1, C-1, C-1, C-1, C-1, C-1, C-1, C-1 | C, 0, 0, 0, 0, 0, 0, 0 | 1, 1, 1, ...

If the Noise Canceler function is enabled, the actual trigger condition for the capture event is monitored over four samples, and all four must be equal to activate the capture flag.

### Timer/Counter1 Control Register A – TCCR1A

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| $2F ($4F) | COM1A1 | COM1A0 | COM1B1 | COM1B0 | – | – | PWM11 | PWM10 | TCCR1A |
| Read/Write | R/W | R/W | R/W | R/W | R | R | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

- **Bits 7..6 – COM1A1, COM1A0: Compare Output Mode1A, Bits 1 and 0**

The COM1A1 and COM1A0 control bits determine any output pin action following a compare match in Timer/Counter1. Any output pin actions affect pin OC1A – Output Compare A pin 1. This is an alternative function to an I/O port, and the corresponding direction control bit must be set (one) to control an output pin. The control configuration is shown in Table 15

- **Bits 5..4 – COM1B1, COM1B0: Compare Output Mode1B, Bits 1 and 0**

The COM1B1 and COM1B0 control bits determine any output pin action following a compare match in Timer/Counter1. Any output pin actions affect pin OC1B – Output Compare B. Since this is an alternative function to an I/O port, the corresponding direction control bit must be set (one) to control an output pin. The control configuration is given in Table 15.

**Table 15.** Compare1 Mode Select

| COM1X1 | COM1X0 | Description |
|---|---|---|
| 0 | 0 | Timer/Counter1 disconnected from output pin OC1X |
| 0 | 1 | Toggle the OC1X output line. |
| 1 | 0 | Clear the OC1X output line (to zero). |
| 1 | 1 | Set the OC1X output line (to one). |

Note: X = A or B.
In PWM mode, these bits have a different function. Refer to Table 16 for a detailed description.

- **Bits 3..2 – Res: Reserved Bits**

These bits are reserved bits in the ATmega103(L) and always read as zero.

- **Bits 1..0 – PWM11, PWM10: Pulse Width Modulator Select Bits**

These bits select PWM operation of Timer/Counter1 as specified in Table 18 on page 53. This mode is described on page 53.

**Table 16.** PWM Mode Select

| PWM11 | PWM10 | Description |
|---|---|---|
| 0 | 0 | PWM operation of Timer/Counter1 is disabled. |

1. In the same operation, write a logical “1” to WDTOE and WDE. A logical “1” must be written to WDE even though it is set to one before the disable operation starts.
2. Within the next four clock cycles, write a logical “0” to WDE. This disables the Watchdog.

- **Bits 2..0 – WDP2, WDP1, WDP0: Watchdog Timer Prescaler 2, 1 and 0**

The WDP2, WDP1 and WDP0 bits determine the Watchdog Timer prescaling when the Watchdog Timer is enabled. The different prescaling values and their corresponding Time-out periods are shown in Table 21.

**Table 21.** Watchdog Timer Prescale Select

| WDP2 | WDP1 | WDP0 | Number of WDT Oscillator Cycles | Typical Time-out at $V_{CC}$ = 3.0V | Typical Time-out at $V_{CC}$ = 5.0V |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 16K cycles | 47 ms | 15 ms |
| 0 | 0 | 1 | 32K cycles | 94 ms | 30 ms |
| 0 | 1 | 0 | 64K cycles | 0.19 s | 60 ms |
| 0 | 1 | 1 | 128K cycles | 0.38 s | 0.12 s |
| 1 | 0 | 0 | 256K cycles | 0.75 s | 0,24 s |
| 1 | 0 | 1 | 512K cycles | 1.5 s | 0.49 s |
| 1 | 1 | 0 | 1,024K cycles | 3.0 s | 0.97 s |
| 1 | 1 | 1 | 2,048K cycles | 6.0 s | 1.9 s |

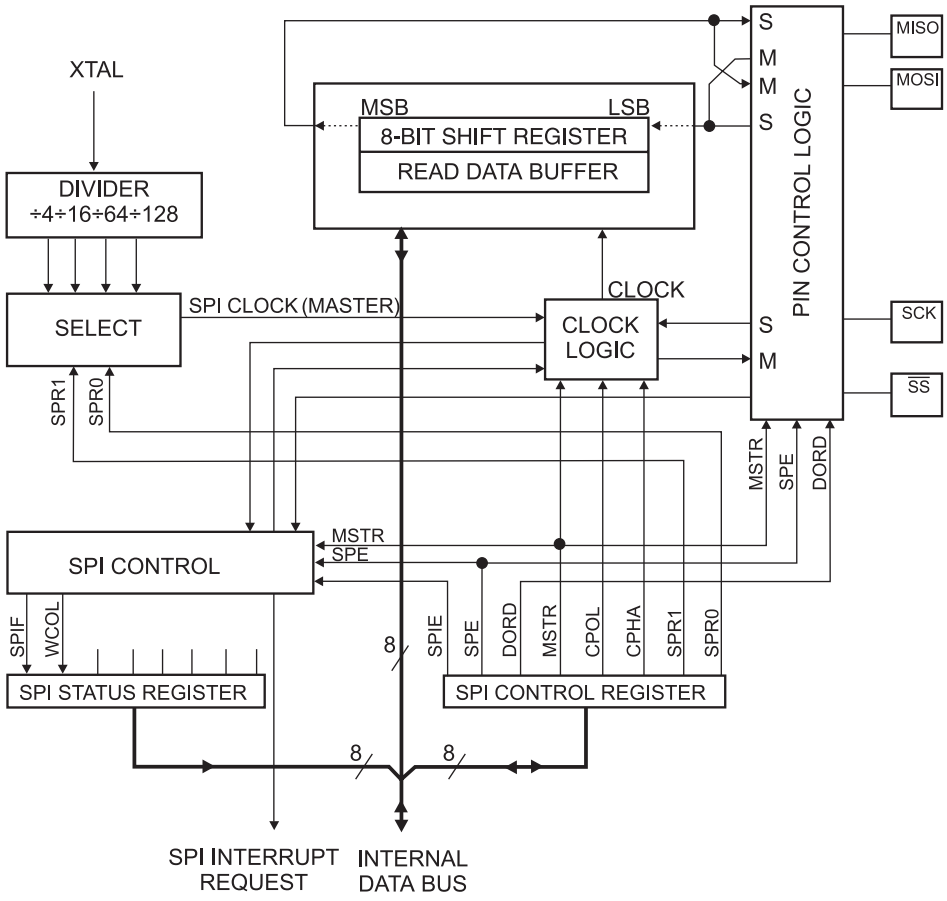
Note: The frequency of the Watchdog Oscillator is voltage-dependent as shown in the Electrical Characteristics section.
The WDR (Watchdog Reset) instruction should always be executed before the Watchdog Timer is enabled. This ensures that the reset period will be in accordance with the Watchdog Timer prescale settings. If the Watchdog Timer is enabled without reset, the Watchdog Timer may not start counting from zero.
To avoid unintentional MCU Reset, the Watchdog Timer should be disabled or reset before changing the Watchdog Timer Prescale Select.

## Serial Peripheral Interface – SPI

The Serial Peripheral Interface (SPI) allows high-speed synchronous data transfer between the ATmega103(L) and peripheral devices or between several AVR devices. The ATmega103(L) SPI features include the following:

- **Full-duplex, Three-wire Synchronous Data Transfer**
- **Master or Slave Operation**
- **LSB First or MSB First Data Transfer**
- **Four Programmable Bit Rates**
- **End-of-Transmission Interrupt Flag**
- **Write Collision Flag Protection**
- **Wake-up from Idle Mode (Slave Mode only)**

**Figure 37.** SPI Block Diagram




The interconnection between Master and Slave CPUs with SPI is shown in Figure 38. The PB1 (SCK) pin is the clock output in the Master mode and is the clock input in the Slave mode. Writing to the SPI Data Register of the Master CPU starts the SPI clock generator, and the data written shifts out of the PB2 (MOSI) pin and into the PB2 (MOSI) pin of the Slave CPU. After shifting one byte, the SPI clock generator stops, setting the End-of-Transmission Flag (SPIF). If the SPI interrupt enable bit (SPIE) in the SPCR Register is set, an interrupt is requested. The Slave Select input, PB0($\overline{SS}$), is set low to select an individual Slave SPI device. The two Shift Registers in the Master and the Slave can be considered as one distributed 16-bit circular Shift Register. This is shown in Figure 38. When data is shifted from the Master to the Slave, data is also shifted in the opposite direction, simultaneously. This means that during one shift cycle, data in the Master and the Slave are interchanged.

## UART

The ATmega103(L) features a full duplex (separate Receive and Transmit Registers) Universal Asynchronous Receiver and Transmitter (UART). The main features are:

- **Baud Rate Generator that can Generate a large Number of Baud Rates (bps)**
- **High Baud Rates at Low XTAL Frequencies**
- **8 or 9 Bits Data**
- **Noise Filtering**
- **OverRun Detection**
- **Framing Error Detection**
- **False Start Bit Detection**
- **Three separate Interrupts on TX Complete, TX Data Register Empty and RX Complete**

### Data Transmission

A block schematic of the UART Transmitter is shown in Figure 41.

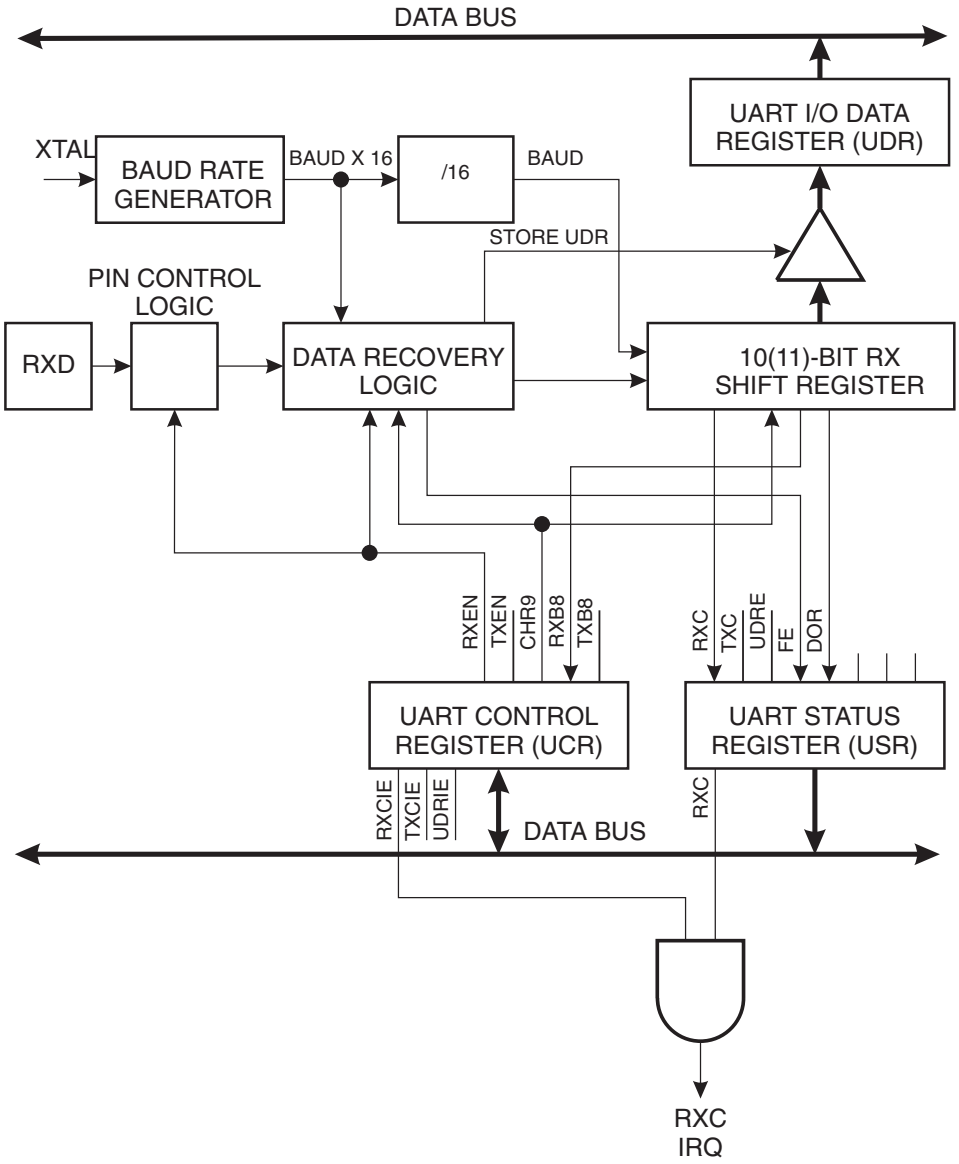
Data transmission is initiated by writing the data to be transmitted to the UART I/O Data Register, UDR. Data is transferred from UDR to the Transmit Shift Register when:

- A new character has been written to UDR after the stop bit from the previous character has been shifted out. The Shift Register is loaded immediately.
- A new character has been written to UDR before the stop bit from the previous character has been shifted out. The Shift Register is loaded when the stop bit of the character currently being transmitted has been shifted out.

If the 10(11)-bit Transmit Shift Register is empty, data is transferred from UDR to the Shift Register. At this time the UDRE (UART Data Register Empty) bit in the UART Status Register, USR, is set. When this bit is set (one), the UART is ready to receive the next character. Writing to UDR clears UDRE. At the same time as the data is transferred from UDR to the 10(11)-bit Shift Register, bit 0 of the Shift Register is cleared (start bit) and bit 9 or 10 is set (stop bit). If 9-bit data word is selected (the CHR9 bit in the UART Control Register, UCR is set), the TXB8 bit in UCR is transferred to bit 9 in the Transmit Shift Register.

## Data Reception

**Figure 42.** UART Receiver




The Receiver front-end logic samples the signal on the RXD pin at a frequency 16 times the baud rate. While the line is idle, one single sample of logical “0” will be interpreted as the falling edge of a start bit, and the start bit detection sequence is initiated. Let sample 1 denote the first zero-sample. Following the 1-to-0 transition, the Receiver samples the RXD pin at samples 8, 9, and 10. If two or more of these three samples are found to be logical “1”s, the start bit is rejected as a noise spike and the Receiver starts looking for the next 1-to-0 transition.

If, however, a valid start bit is detected, sampling of the data bits following the start bit is performed. These bits are also sampled at samples 8, 9 and 10. The logical value found in at least two of the three samples is taken as the bit value. All bits are shifted into the Transmitter Shift Register as they are sampled. Sampling of an incoming character is shown in Figure 43.

- **Bit 1 – RXB8: Receive Data Bit 8**

When CHR9 is set (one), RXB8 is the ninth data bit of the received character.

- **Bit 0 – TXB8: Transmit Data Bit 8**

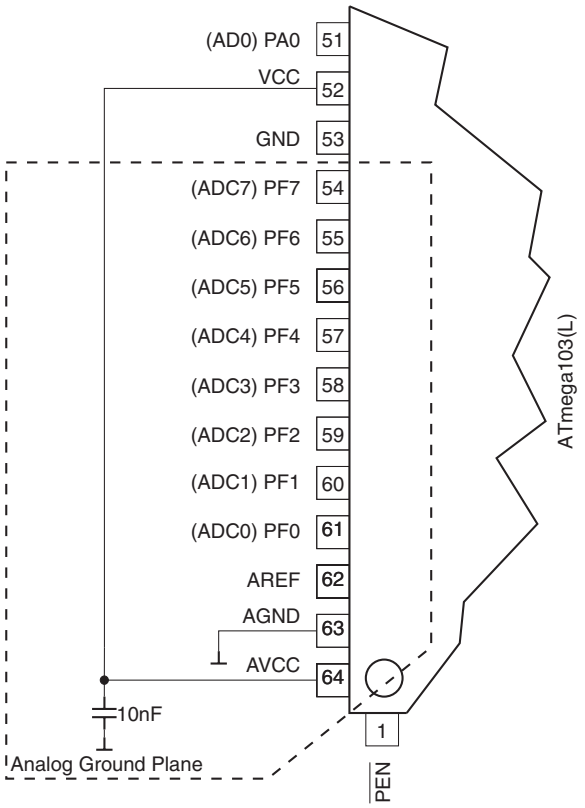
When CHR9 is set (one), TXB8 is the ninth data bit in the character to be transmitted.

## ADC Noise Canceling Techniques

Digital circuitry inside and outside the ATmega103(L) generates EMI, which might affect the accuracy of analog measurements. If conversion accuracy is critical, the noise level can be reduced by applying the following techniques:

1. The analog part of the ATmega103(L) and all analog components in the application should have a separate analog ground plane on the PCB. This ground plane is connected to the digital ground plane via a single point on the PCB.
2. Keep analog signal paths as short as possible. Make sure analog tracks run over the analog ground plane, and keep them well away from high-speed switching digital tracks.
3. The $AV_{CC}$ pin on the ATmega103(L) should have its own decoupling capacitor as shown in Figure 49.
4. Use the ADC Noise Canceler function to reduce induced noise from the CPU.
5. If some Port F pins are used as digital inputs, it is essential that these do not switch while a conversion is in progress.

**Figure 49.** ADC Power Connections



pins are tri-stated when a reset condition becomes active, even if the clock is not running.

**Table 28.** DDAn Effects on Port A Pins

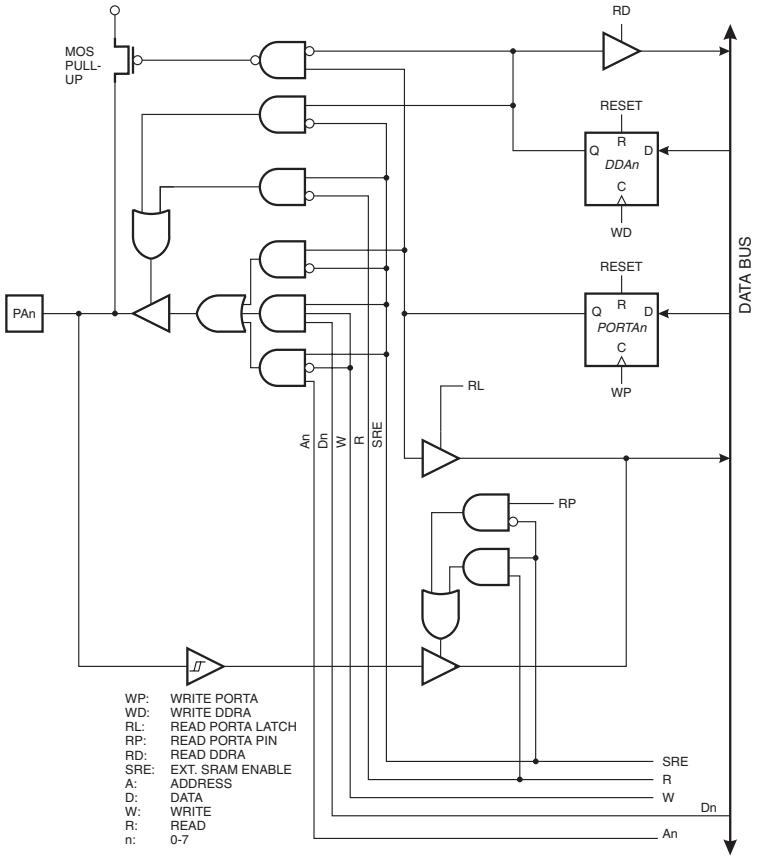
| DDAn | PORTAn | I/O | Pull-up | Comment |
|---|---|---|---|---|
| 0 | 0 | Input | No | Tri-state (high-Z) |
| 0 | 1 | Input | Yes | PAn will source current if ext. pulled low. |
| 1 | 0 | Output | No | Push-pull Zero Output |
| 1 | 1 | Output | No | Push-pull One Output |

Note: n: 7,6...0, pin number

### Port A Schematics

Note that all port pins are synchronized. The synchronization latch is, however, not shown in the figure.

**Figure 53.** Port A Schematic Diagrams (Pins PA0 - PA7)




## Port B

Port B is an 8-bit bi-directional I/O port with internal pull-ups.

Three I/O memory address locations are allocated for Port B, one each for the Data Register – PORTB, $18($38), Data Direction Register – DDRB, $17($37) and the Port B Input Pins – PINB, $16($36). The Port B Input Pins address is read-only, while the Data Register and the Data Direction Register are read/write.

All port pins have individually selectable pull-up resistors. The Port B output buffers can sink 20 mA and thus drive LED displays directly. When pins PB0 to PB7 are used as

**Figure 55.** Port B Schematic Diagram (Pin PB1)

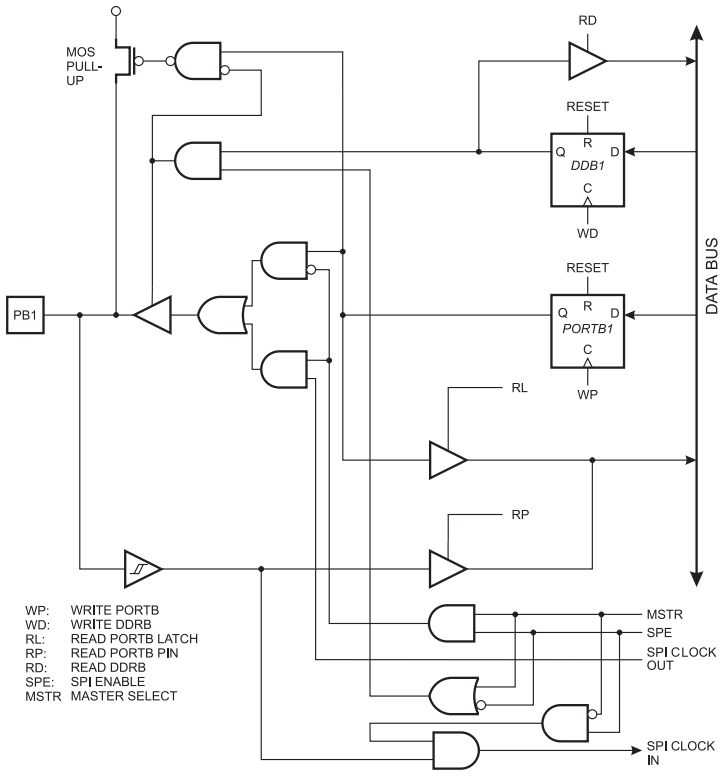



**Figure 56.** Port B Schematic Diagram (Pin PB2)

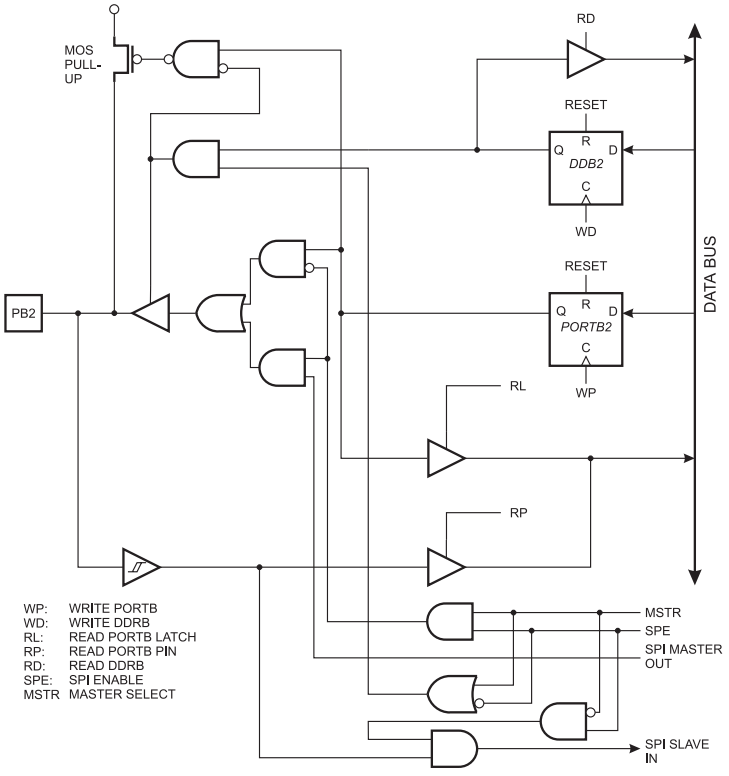
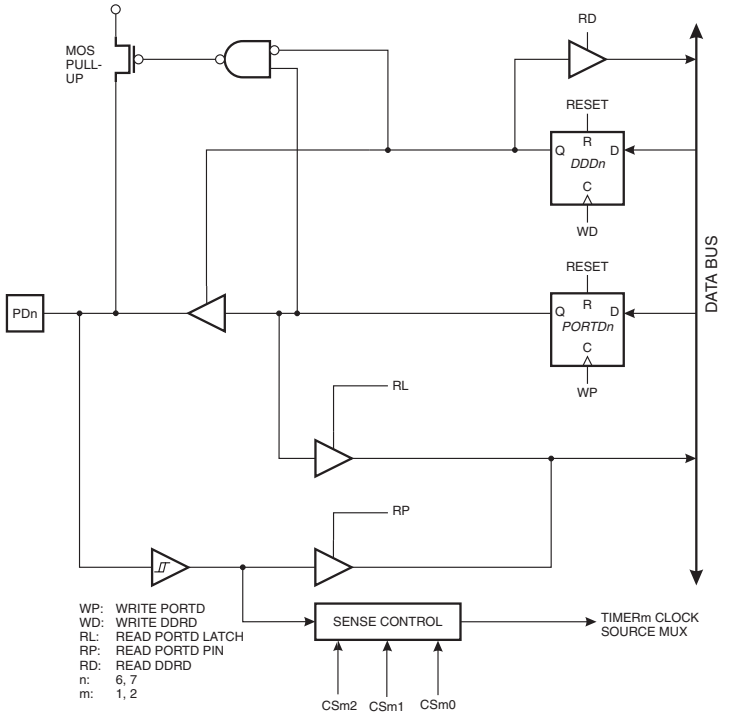


**Figure 65.** Port D Schematic Diagram (Pins PD6 and PD7)




## Port E

Port E is an 8-bit bi-directional I/O port with internal pull-up resistors.

Three I/O memory address locations are allocated for the Port E, one each for the Data Register – PORTE, $03($23), Data Direction Register – DDRE, $02($22) and the Port E Input Pins – PINE, $01($21). The Port E Input Pins address is read-only, while the Data Register and the Data Direction Register are read/write.

The Port E output buffers can sink 20 mA. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated.

All Port E pins have alternate functions as shown in Table 33.

**Table 33.** Port E Pin Alternate Functions

| Port Pin | Alternate Function |
|---|---|
| PE0 | PDI/RXD (Programming Data Input or UART Receive Pin) |
| PE1 | PDO/TXD (Programming Data Output or UART Transmit Pin) |
| PE2 | AC+ (Analog Comparator Positive Input) |
| PE3 | AC- (Analog Comparator Negative Input) |
| PE4 | INT4 (External Interrupt4 Input) |
| PE5 | INT5 (External Interrupt5 Input) |
| PE6 | INT6 (External Interrupt6 Input) |
| PE7 | INT7 (External Interrupt7 Input) |

When the pins are used for the alternate function, the DDRE and PORTE Registers have to be set according to the alternate function description.

# Electrical Characteristics

## Absolute Maximum Ratings*

| | |
|---|---|
| Operating Temperature | -40°C to +105°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin except $\overline{\text{RESET}}$ with Respect to Ground | -1.0V to $V_{CC}$ + .5V |
| Voltage on $\overline{\text{RESET}}$ with Respect to Ground | -1.0V to + 13.0V |
| Maximum Operating Voltage | 6.6V |
| DC Current per I/O Pin | 40.0 mA |
| DC Current $V_{CC}$ and GND | 400.0 mA |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC Characteristics

$T_A$ = -40°C to 85°C, $V_{CC}$ = 2.7V to 3.6V and 4.0V to 5.5V (unless otherwise noted)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | Except (XTAL) | -0.5 | | 0.3 $V_{CC}$[1] | V |
| $V_{IL1}$ | Input Low Voltage | XTAL | -0.5 | | 0.2 $V_{CC}$ - 0.1[1] | V |
| $V_{IH}$ | Input High Voltage | Except (XTAL, $\overline{\text{RESET}}$) | 0.6 $V_{CC}$[2] | | $V_{CC}$ + 0.5 | V |
| $V_{IH1}$ | Input High Voltage | XTAL | 0.7 $V_{CC}$[2] | | $V_{CC}$ + 0.5 | V |
| $V_{IH2}$ | Input High Voltage | RESET | 0.85 $V_{CC}$[2] | | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low Voltage[3] Ports A, B, C, D, E | $I_{OL}$ = 20 mA, $V_{CC}$ = 5V<br>$I_{OL}$ = 10 mA, $V_{CC}$ = 3V | | | 0.6<br>0.5 | V<br>V |
| $V_{OH}$ | Output High Voltage[4] Ports A, B, C, D, E | $I_{OH}$ = -3 mA, $V_{CC}$ = 5V<br>$I_{OH}$ = -1.5 mA, $V_{CC}$ = 3V | 4.3<br>2.2 | | | V<br>V |
| $I_{IL}$ | Input Leakage Current I/O Pin | $V_{CC}$ = 6V, Pin Low (absolute value) | | | 8.0 | µA |
| $I_{IH}$ | Input Leakage Current I/O Pin | $V_{CC}$ = 6V, Pin High (absolute value) | | | 8.0 | µA |
| RRST | Reset Pull-up | | 100 | | 500 | kΩ |
| $R_{I/O}$ | I/O Pin Pull-up | | 35 | | 120 | kΩ |
| $I_{CC}$ | Power Supply Current | Active 4 MHz, $V_{CC}$ = 3V | | | 5.0 | mA |
| | | Idle 4 MHz, $V_{CC}$ = 3V | | | 2.0 | mA |
| | | Power-down[5], $V_{CC}$ = 3V WDT Enabled | | | 40.0 | µA |
| | | Power-down[5], $V_{CC}$ = 3V WDT Disabled | | | 25.0 | µA |
| | | Power-save[5], $V_{CC}$ = 3V WDT Disabled | | | 35.0 | µA |

## External Data Memory Timing

**Table 45.** External Data Memory Characteristics, 4.0 - 6.0 Volts, No Wait State

| | | | 6 MHz Oscillator | | Variable Oscillator | | |
|---|---|---|---|---|---|---|---|
| | Symbol | Parameter | Min | Max | Min | Max | Unit |
| 0 | $1/t_{CLCL}$ | Oscillator Frequency | | | 0.0 | 6.0 | MHz |
| 1 | $t_{LHLL}$ | ALE Pulse Width | 48.3 | | $0.5\ t_{CLCL}$ - 35.0(1) | | ns |
| 2 | $t_{AVLL}$ | Address Valid A to ALE Low | 43.3 | | $0.5\ t_{CLCL}$ - 40.0(1) | | ns |
| 3a | $t_{LLAX\_ST}$ | Address Hold after ALE Low, ST/STD/STS Instructions | 77.3 | | $0.5\ t_{CLCL}$ - 10.0(2) | | ns |
| 3b | $t_{LLAX\_LD}$ | Address Hold after ALE Low, LD/LDD/LDS Instructions | 15.0 | | 15.0 | | ns |
| 4 | $t_{AVLLC}$ | Address Valid C to ALE Low | 43.3 | | $0.5\ t_{CLCL}$ - 40.0(1) | | ns |
| 5 | $t_{AVRL}$ | Address Valid to RD Low | 136.7 | | $1.0\ t_{CLCL}$ - 30.0 | | ns |
| 6 | $t_{AVWL}$ | Address Valid to WR Low | 215.0 | | $1.5\ t_{CLCL}$ - 35.0(1) | | ns |
| 7 | $t_{LLWL}$ | ALE Low to WR Low | 146.7 | 186.7 | $1.0\ t_{CLCL}$ - 20.0 | $1.0\ t_{CLCL}$ + 20.0 | ns |
| 8 | $t_{LLRL}$ | ALE Low to RD Low | 146.7 | 186.7 | $0.5\ t_{CLCL}$ - 20.0(2) | $0.5\ t_{CLCL}$ + 20.0(2) | ns |
| 9 | $t_{DVRH}$ | Data Setup to RD High | 70.0 | | 70.0 | | ns |
| 10 | $t_{RLDV}$ | Read Low to Data Valid | | 136.7 | | $1.0\ t_{CLCL}$ - 30.0 | ns |
| 11 | $t_{RHDX}$ | Data Hold after RD High | 0.0 | | 0.0 | | ns |
| 12 | $t_{RLRH}$ | RD Pulse Width | 146.7 | | $1.0\ t_{CLCL}$ - 20.0 | | ns |
| 13 | $t_{DVWL}$ | Data Setup to WR Low | 53.3 | | $0.5\ t_{CLCL}$ - 30.0(2) | | ns |
| 14 | $t_{WHDX}$ | Data Hold after WR High | 0.0 | | 0.0 | | ns |
| 15 | $t_{DVWH}$ | Data Valid to WR High | 146.7 | | $1.0\ t_{CLCL}$ - 20.0 | | ns |
| 16 | $t_{WLWH}$ | WR Pulse Width | 63.3 | | $0.5\ t_{CLCL}$ - 20.0(1) | | ns |

**Table 46.** External Data Memory Characteristics, 4.0 - 6.0 Volts, 1 Cycle Wait State

| | | | 6 MHz Oscillator | | Variable Oscillator | | |
|---|---|---|---|---|---|---|---|
| | Symbol | Parameter | Min | Max | Min | Max | Unit |
| 0 | $1/t_{CLCL}$ | Oscillator Frequency | | | 0.0 | 6.0 | MHz |
| 10 | $t_{RLDV}$ | Read Low to Data Valid | | 303.4 | | $2.0\ t_{CLCL}$ - 30.0 | ns |
| 12 | $t_{RLRH}$ | RD Pulse Width | 313.4 | | $2.0\ t_{CLCL}$ - 20.0 | | ns |
| 15 | $t_{DVWH}$ | Data Valid to WR High | 313.4 | | $2.0\ t_{CLCL}$ - 20.0 | | ns |
| 16 | $t_{WLWH}$ | WR Pulse Width | 230.0 | | $1.5\ t_{CLCL}$ - 20.0(2) | | ns |

Notes: 1. This assumes 50% clock duty cycle. The half period is actually the high time of the external clock, XTAL1.
2. This assumes 50% clock duty cycle. The half period is actually the low time of the external clock, XTAL1.

**Figure 98.** I/O Pin Source Current vs. Output Voltage

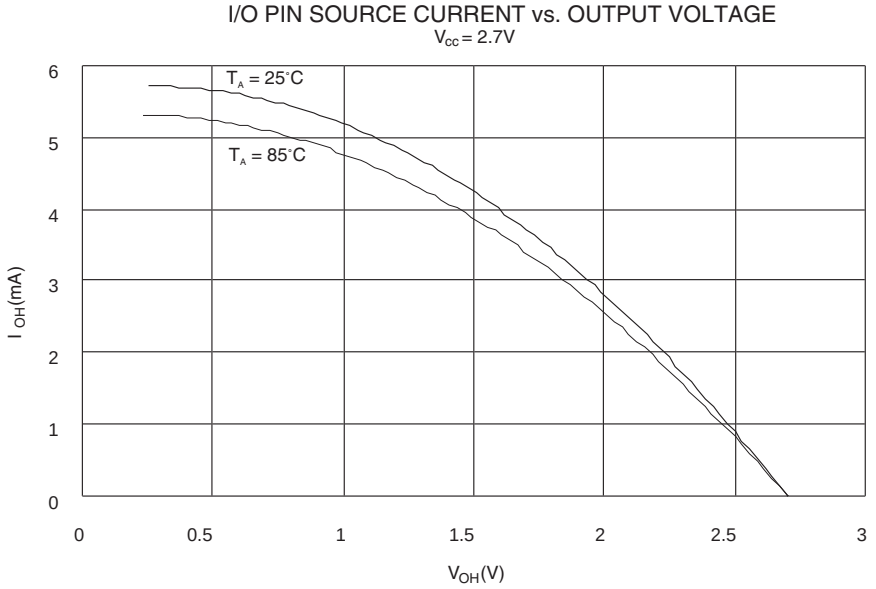



**Figure 99.** I/O Pin Input Threshold Voltage vs. $V_{CC}$