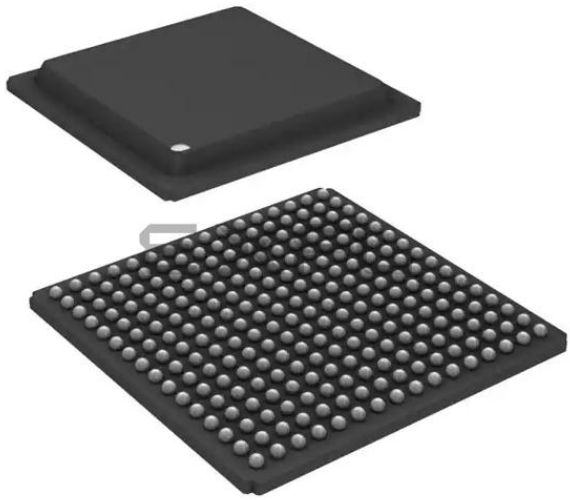

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	166MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc853tvr66a

and incorporates memory management units (MMUs), instruction and data caches. The MPC853T is a subset of this family of devices and is the main focus of this document.

2 Features

The MPC853T is comprised of three modules that each use the 32-bit internal bus: a MPC8xx core, a system integration unit (SIU), and a communications processor module (CPM). The MPC853T block diagram is shown in Figure 1.

The following list summarizes the key MPC853T features:

- Embedded MPC8xx core up to 100 MHz
- Maximum frequency operation of the external bus is 66 MHz
  - The 50-/66-MHz core frequencies support both the 1:1 and 2:1 modes.
  - The 80-/100-MHz core frequencies support 2:1 mode only.
- Single-issue, 32-bit core (compatible with the PowerPC architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch and without conditional execution.
  - 4-Kbyte data cache and 4-Kbyte instruction cache
    - Instruction cache is two-way, set-associative with 128 sets
    - Data cache is two-way, set-associative with 128 sets
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry translation look-aside buffer (TLB), fully associative instruction, and data TLBs
  - MMUs support multiple page sizes of 4 Kbytes, 16 Kbytes, 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank.
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROMs, Flash EPROMs, and other memory devices
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbytes–256 Mbytes)
  - Selectable write protection
  - On-chip bus arbitration logic
- Fast Ethernet Controller (FEC)

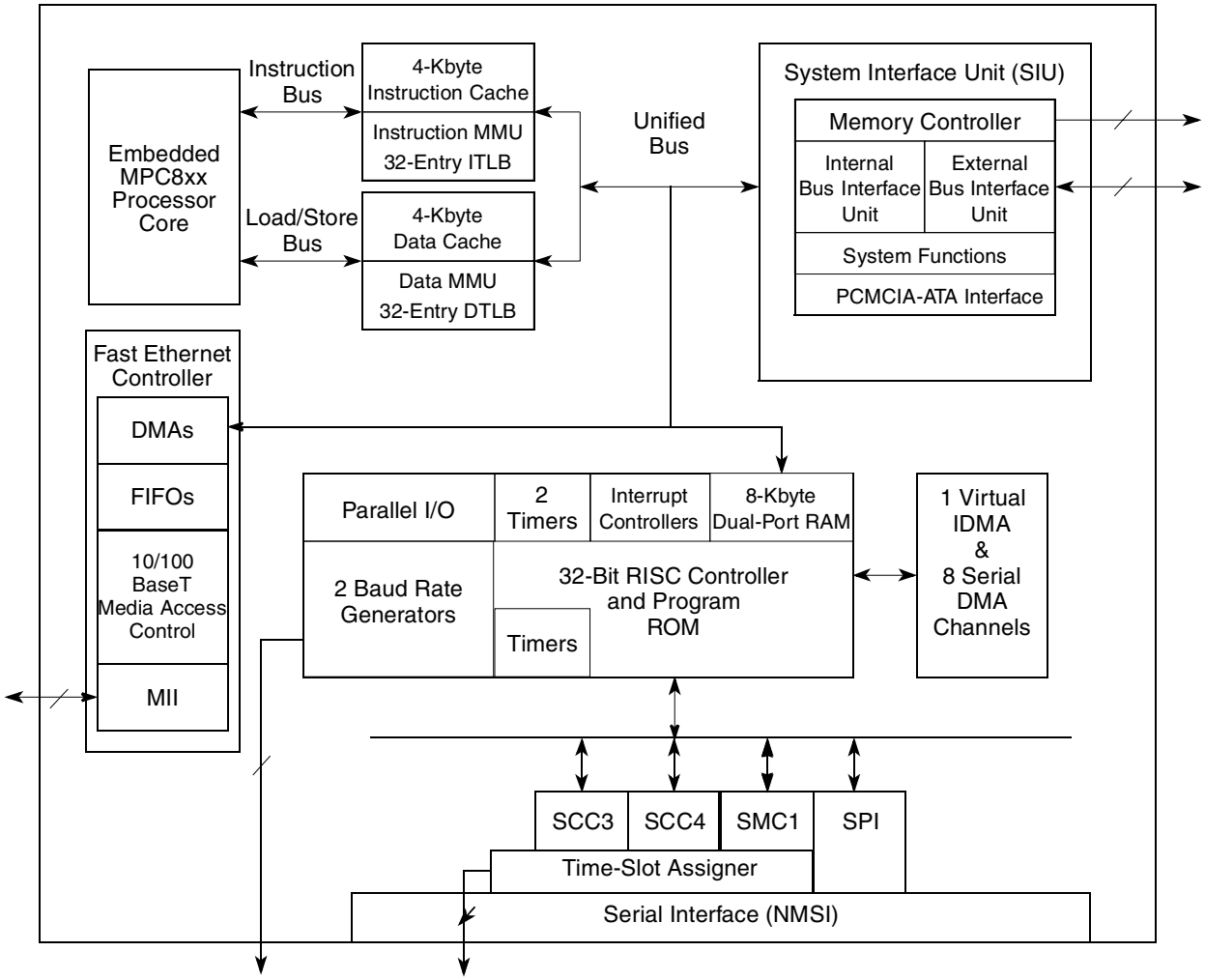

Figure 1. MPC853T Block Diagram

Table 4. Power Dissipation (P_D)

Die Revision	Bus Mode	Frequency (MHz)	Typical [1]	Maximum [2]	Unit
0	1:1	50	110	140	mW
		66	150	180	mW
	2:1	66	140	160	mW
		80	170	200	mW
		100	210	250	mW

1 Typical power dissipation is measured at 1.9 V.

2 Maximum power dissipation at V_{DDL} and V_{DDSYN} is at 1.9 V, and V_{DDH} is at 3.465 V.

NOTE

Values in Table 4 represent V_{DDL}-based power dissipation and do not include I/O power dissipation over V_{DDH}. I/O power dissipation varies widely by application due to buffer current, which depends on external circuitry.

The V_{DDSYN} power dissipation is negligible.

6 DC Characteristics

Table 5 provides the DC electrical characteristics for the MPC853T.

Table 5. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage	V_{DDH}	3.135	3.465	V
	V_{DDL}	1.7	1.9	V
	V_{DDSYN}	1.7	1.9	V
	Difference between V_{DDL} and V_{DDSYN}	—	100	mV
Input high voltage (all inputs except PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15, PD[3:15], TDI, TDO, TCK, $\overline{\text{TRST}}$, TMS, MII_TXEN, MII_MDIO) [1]	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
EXTAL, EXTCLK input high voltage	V_{IHC}	$0.7 \times V_{DDH}$	V_{DDH}	V
Input leakage current, Vin = 5.5 V (except the TMS, $\overline{\text{TRST}}$, DSCK, and DSDI pins) for 5-V tolerant pins [1]	I_{in}	—	100	µA
Input leakage current, Vin = V_{DDH} (except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI)	I_{In}	—	10	µA
Input leakage current, Vin = 0 V (except the TMS, $\overline{\text{TRST}}$, DSCK, and DSDI)	I_{In}	—	10	µA
Input capacitance [2]	C_{in}	—	20	pF

Table 5. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Output high voltage, IOH = –2.0 mA, V_{DDH} = 3.0 V (except XTAL and open-drain pins)	V_{OH}	2.4	—	V
Output low voltage IOL = 2.0 mA (CLKOUT) IOL = 3.2 mA [3] IOL = 5.3 mA [4] IOL = 7.0 mA (Txd1/pa14, txd2/pa12) IOL = 8.9 mA ($\overline{TS}$, $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{HRESET}$, $\overline{SRESET}$)	V_{OL}	—	0.5	V

1 The PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15, PD[3:15], TDI, TDO, TCK, $\overline{TRST}$, TMS, MII_TXEN, and MII_MDIO are 5-V tolerant pins.

2 Input capacitance is periodically sampled.

3 A(0:31), TSIZ0/$\overline{REG}$, TSIZ1, D(0:31), DP(0:3)/$\overline{IRQ}$(3:6), RD/$\overline{WR}$, $\overline{BURST}$, $\overline{RSV}$/$\overline{IRQ2}$, IWP(0:1)/VFLS(0:1), RXD3/PA11, TXD3/PA10, RXD4/PA9, TXD4/PA8, TIN3/BRGO3/CLK5/PA3, BRGCLK2/$\overline{TOUT3}$/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, $\overline{TOUT4}$/CLK8/PA0, $\overline{SPISEL}$/PB31, SPICLK/PB30, SPIMOSI/PB29, BRGO4/SPIMISO/PB28, SMTXD1/PB25, SMRXD1/PB24, BRGO3/PB15, $\overline{RTS1}$/$\overline{DREQ0}$/PC15, $\overline{RTS3}$/PC13, $\overline{RTS4}$/PC12, $\overline{CTS3}$/PC7, $\overline{CD3}$/PC6, $\overline{CTS4}$/$\overline{SDACK1}$/PC5, $\overline{CD4}$/PC4, MII-RXD3/PD15, MII-RXD2/PD14, MII-RXD1/PD13, MII-MDC/PD12, MII-TXERR/RXD3/PD11, MII-RX0/TXD3/PD10, MII-TXD0/RXD4/PD9, MII-RXCLK/TXD4/PD8, MII-TXD3/PD5, MII-RXDV/$\overline{RTS4}$/PD6, MII-RXERR/$\overline{RTS3}$/PD7, MII-TXD2/REJECT3/PD4, MII-TXD1/REJECT4/PD3, MII_CRS, MII_MDIO, MII_TXEN, MII_COL

4 $\overline{BDIP}$/$\overline{GPL\_B}$(5), $\overline{BR}$, $\overline{BG}$, FRZ/$\overline{IRQ6}$, $\overline{CS}$(0:5), $\overline{CS}$(6), $\overline{CS}$(7), $\overline{WE0}$/BS_B0/$\overline{IORD}$, $\overline{WE1}$/BS_B1/$\overline{IOWR}$, $\overline{WE2}$/BS_B2/$\overline{PCOE}$, $\overline{WE3}$/ BS_B3/$\overline{PCWE}$, $\overline{BS\_A}$(0:3), $\overline{GPL\_A0}$/$\overline{GPL\_B0}$, $\overline{OE}$/$\overline{GPL\_A1}$/$\overline{GPL\_B1}$, $\overline{GPL\_A}$(2:3)/$\overline{GPL\_B}$(2:3)/$\overline{CS}$(2:3), UPWAITA/$\overline{GPL\_A4}$, $\overline{GPL\_A5}$, ALE_A, $\overline{CE}$1_A, $\overline{CE}$2_A, DSCK, OP(0:1), OP2/MODCK1/$\overline{STS}$, OP3/MODCK2/DSDO, BADDR(28:30)

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DDL} \times I_{DDL}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

NOTE

The V_{DDSYN} power dissipation is negligible.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature ºC

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (ºC/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages, and especially PBGA packages, is strongly dependent on the board temperature. If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)
T_B = board temperature ºC
P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

Table 8. Frequency Ranges for Standard Part Frequencies (2:1 Bus Mode)

Part Frequency	50 MHz		66 MHz		80 MHz		100 MHz	
	Min	Max	Min	Max	Min	Max	Min	Max
Core Frequency	40	50	40	66.67	40	80	40	100
Bus Frequency 2:1	20	25	20	33.33	20	40	20	50

Table 9 provides the bus operation timing for the MPC853T at 33, 40, 50, and 66 MHz.

The timing for the MPC853T bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. CLKOUT assumes a 100-pF load maximum delay.

Table 9. Bus Operation Timings

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	Bus period (CLKOUT), see Table 7	—	—	—	—	—	—	—	—	ns
B1a	EXTCLK to CLKOUT phase skew - If CLKOUT is an integer multiple of EXTCLK, then the rising edge of EXTCLK is aligned with the rising edge of CLKOUT. For a non-integer multiple of EXTCLK, this synchronization is lost, and the rising edges of EXTCLK and CLKOUT have a continuously varying phase skew.	–2	+2	–2	+2	–2	+2	–2	+2	ns
B1b	CLKOUT frequency jitter peak-to-peak	—	1	—	1	—	1	—	1	ns
B1c	Frequency jitter on EXTCLK [1]	—	0.50	—	0.50	—	0.50	—	0.50	%
B1d	CLKOUT phase jitter peak-to-peak for OSCLK ≥ 15 MHz	—	4	—	4	—	4	—	4	ns
	CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz	—	5	—	5	—	5	—	5	ns
B2	CLKOUT pulse width low (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns
B3	CLKOUT pulse width high (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns
B4	CLKOUT rise time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B5	CLKOUT fall time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B7a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B7b	CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), $\overline{STS}$ output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30) RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) valid (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B8a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR valid (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B8b	CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{STS}$ valid [3] (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B9	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3), TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, PTR High-Z (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B11	CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion (MAX = 0.25 × B1 + 6.0)	7.60	13.60	6.30	12.30	5.00	11.00	3.80	9.80	ns
B11a	CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.30 [2])	2.50	9.30	2.50	9.30	2.50	9.30	2.50	9.80	ns
B12	CLKOUT to $\overline{TS}$, $\overline{BB}$ negation (MAX = 0.25 × B1 + 4.8)	7.60	12.30	6.30	11.00	5.00	9.80	3.80	8.50	ns
B12a	CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B13	CLKOUT to $\overline{TS}$, $\overline{BB}$ High-Z (MIN = 0.25 × B1)	7.60	21.60	6.30	20.30	5.00	19.00	3.80	14.00	ns
B13a	CLKOUT to $\overline{TA}$, $\overline{BI}$ High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 × B1 + 2.5)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to $\overline{TEA}$ assertion (MAX = 0.00 × B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B15	CLKOUT to $\overline{TEA}$ High-Z (MIN = 0.00 × B1 + 2.50)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	$\overline{TA}$, $\overline{BI}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B16a	$\overline{TEA}$, $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 4.5)	4.50	—	4.50	—	4.50	—	4.50	—	ns
B16b	$\overline{BB}$, $\overline{BG}$, $\overline{BR}$, valid to CLKOUT (setup time) [3] (4MIN = 0.00 × B1 + 0.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B37	UPWAIT valid to CLKOUT falling edge [9] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid [9] (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge [10] (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

1 If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) the maximum allowed jitter on EXTAL can be up to 2%.

2 For part speeds above 50 MHz, use 9.80 ns for B11a.

3 The timing required for $\overline{BR}$ input is relevant when the MPC853T is selected to work with the internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC853T is selected to work with the external bus arbiter.

4 For part speeds above 50 MHz, use 2 ns for B17.

5 The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

6 For part speeds above 50 MHz, use 2 ns for B19.

7 The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.

8 The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

9 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 18.

10 The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 21.

Figure 5 provides the timing for the synchronous output signals.

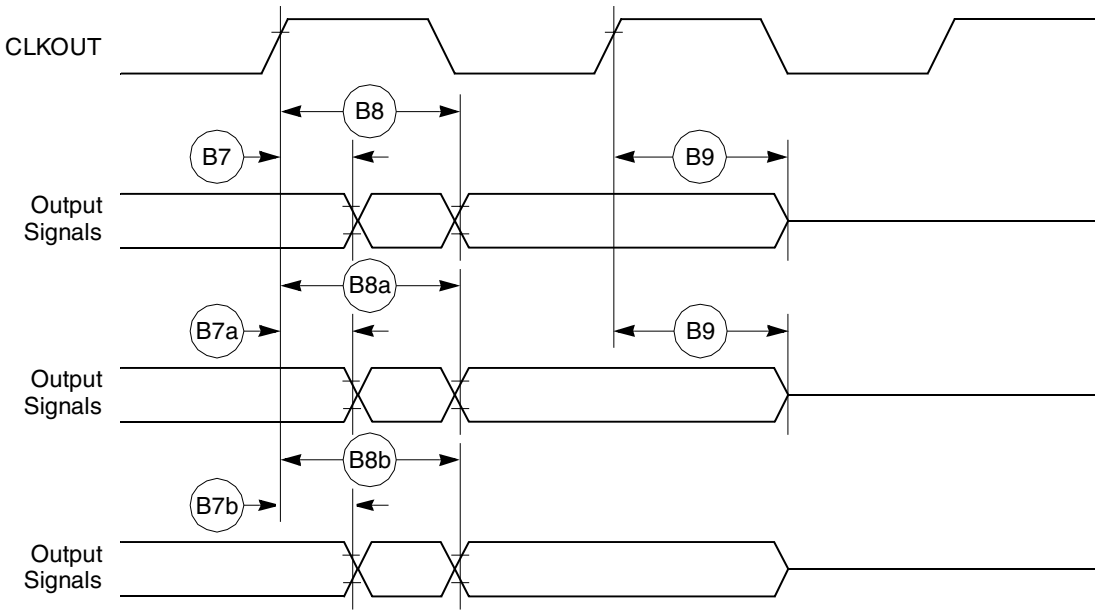

Figure 5. Synchronous Output Signals Timing

Figure 6 provides the timing for the synchronous active pull-up and open-drain output signals.

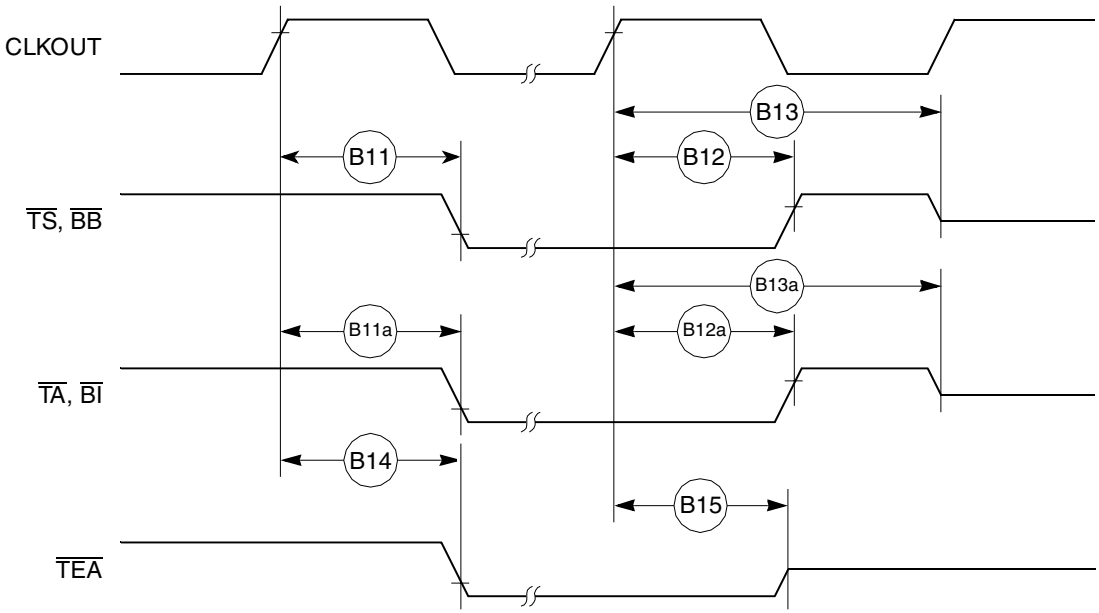

Figure 6. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

Figure 7 provides the timing for the synchronous input signals.

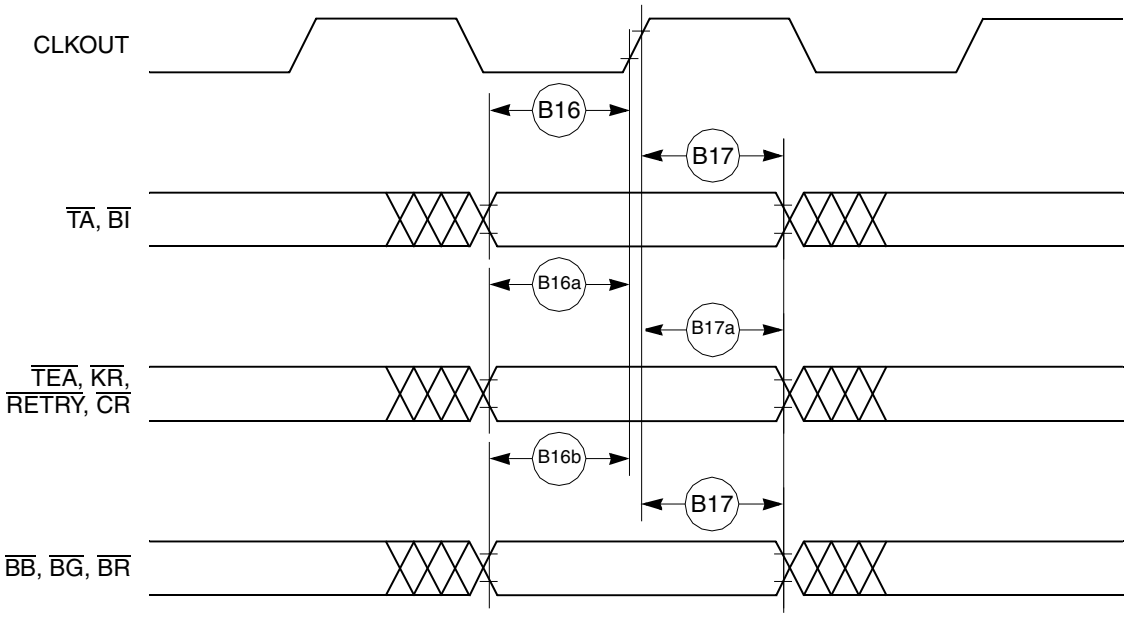

Figure 7. Synchronous Input Signals Timing

Figure 8 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

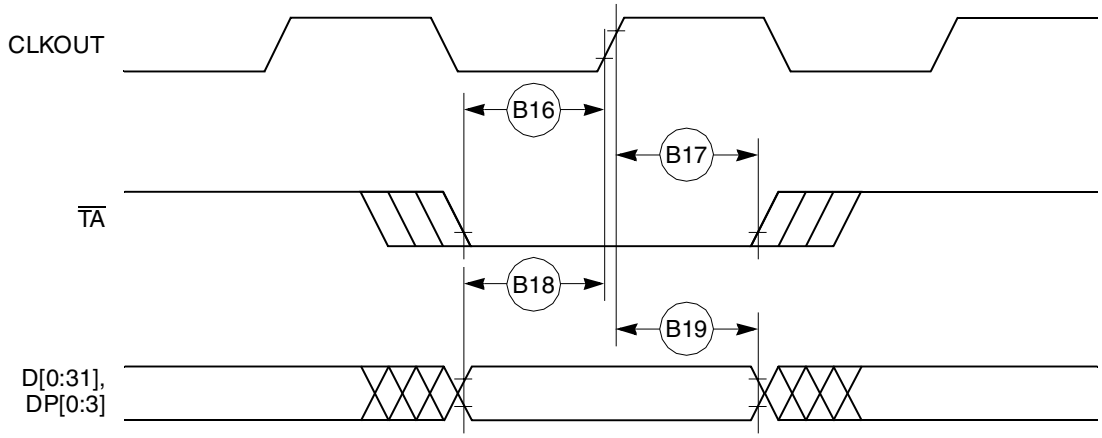

Figure 8. Input Data Timing in Normal Case

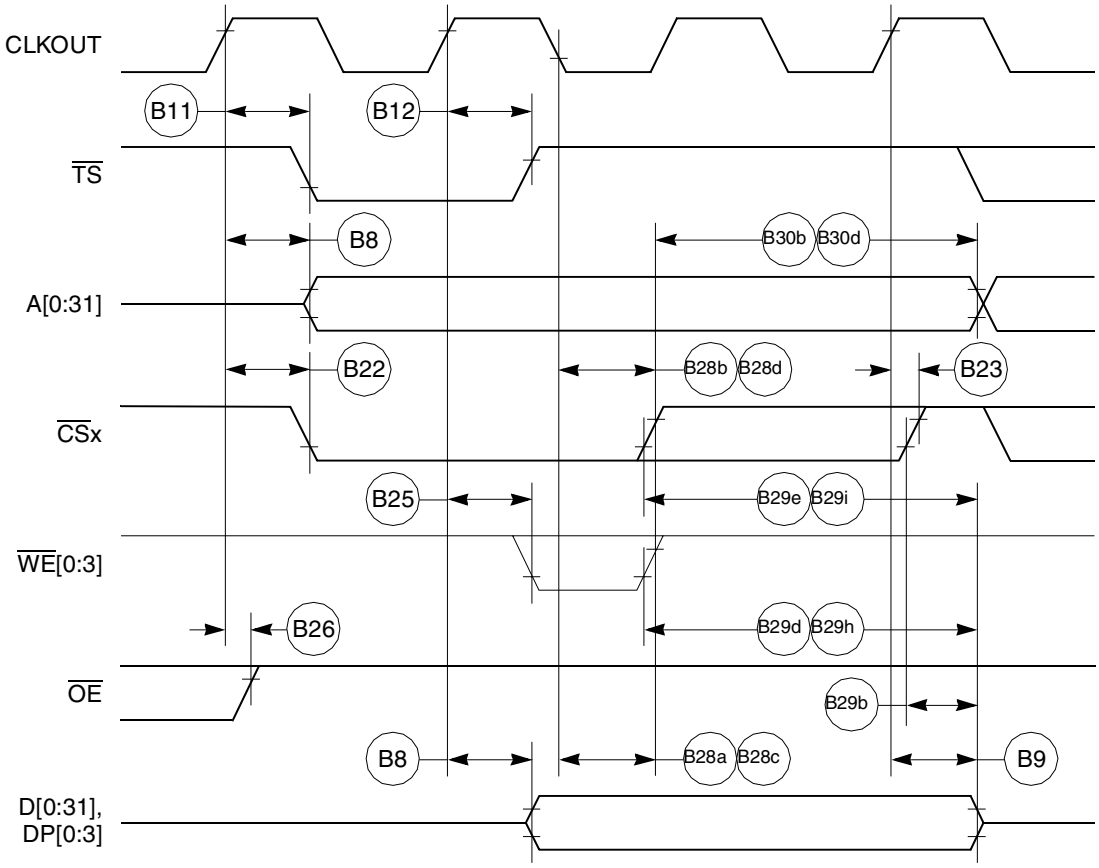

Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

Figure 32 shows the reset timing for the data bus configuration.

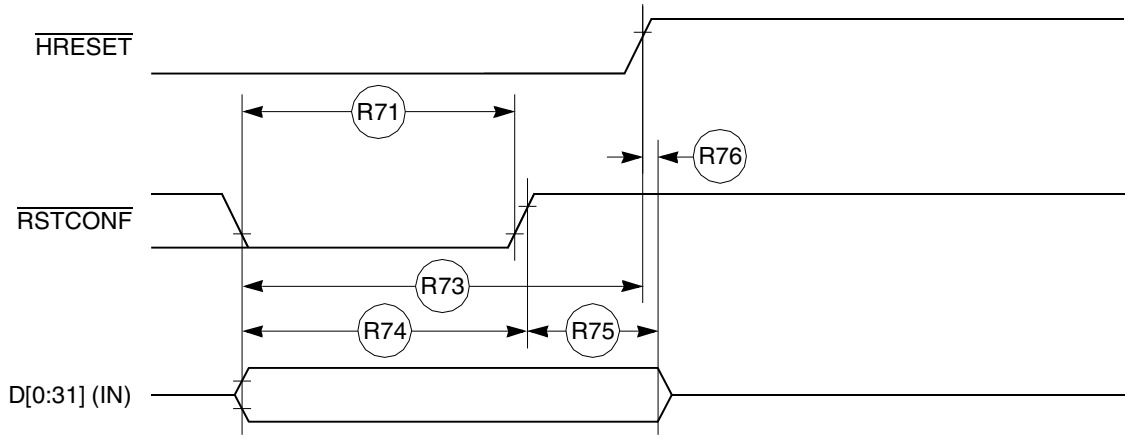

Figure 32. Reset Timing—Configuration from Data Bus

Figure 33 provides the reset timing for the data bus weak drive during configuration.

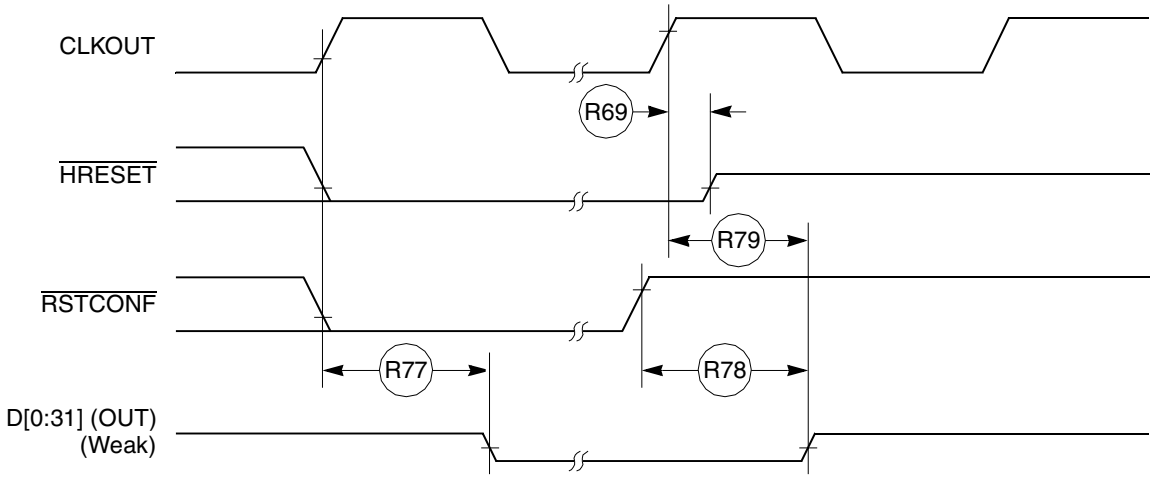

Figure 33. Reset Timing—Data Bus Weak Drive During Configuration

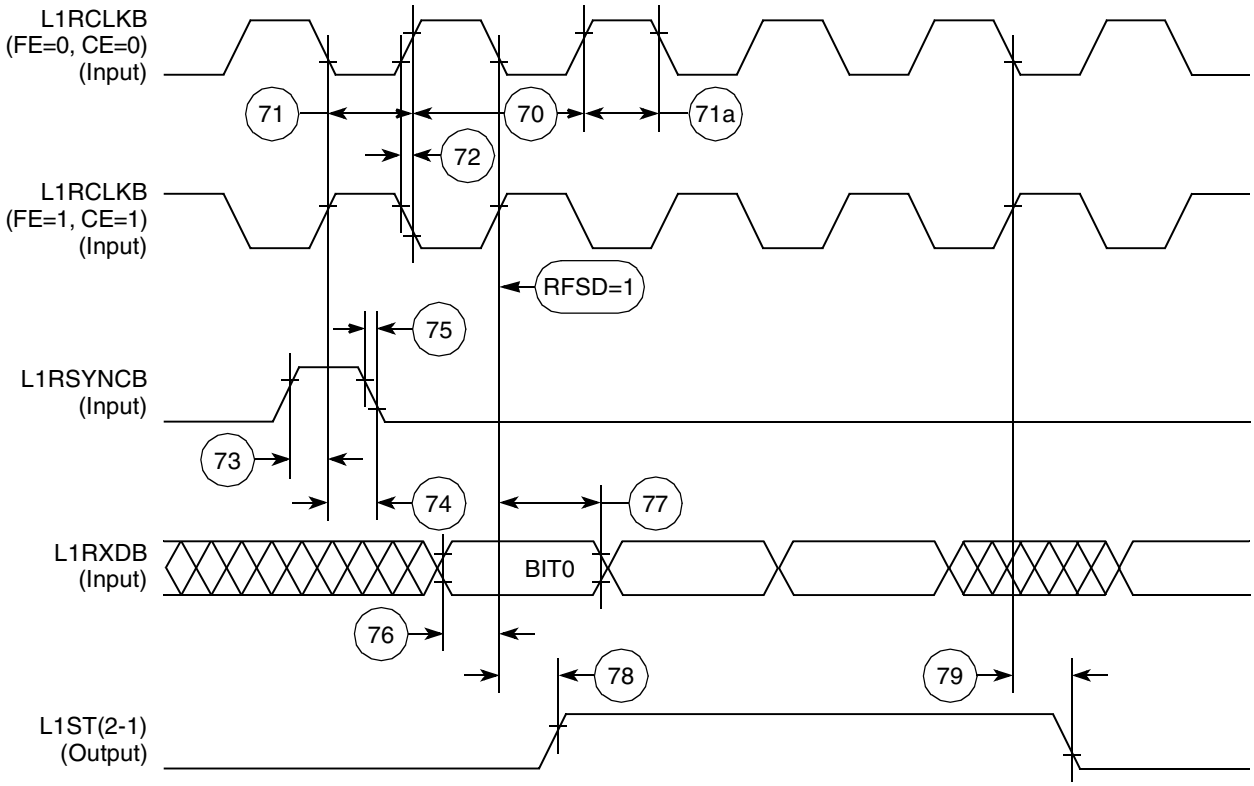

Figure 46. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

Figure 51 through Figure 53 show the NMSI timings.

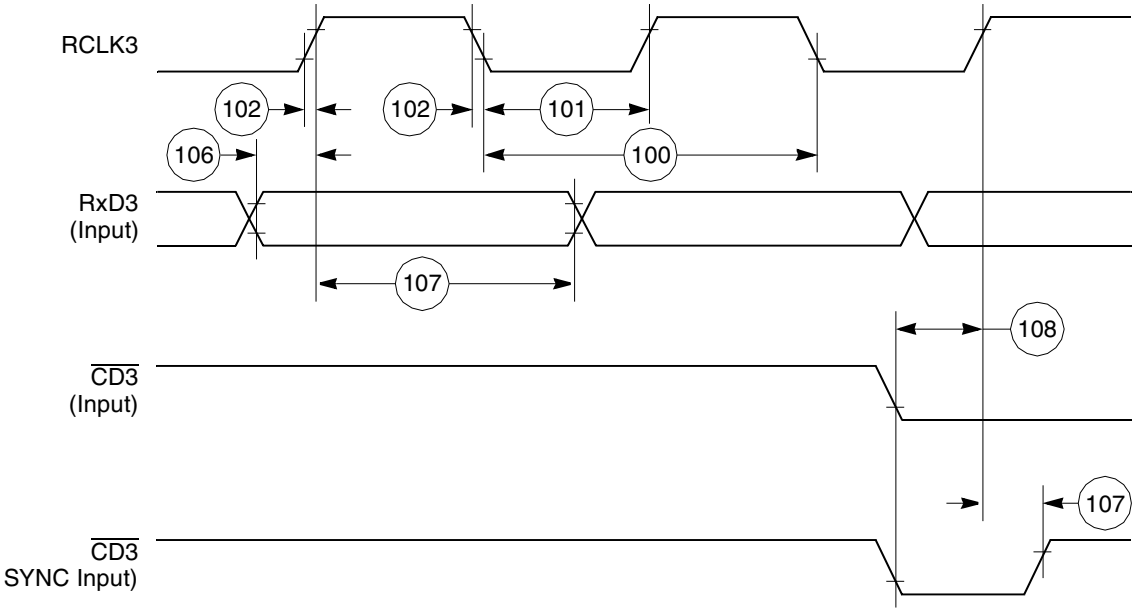

Figure 51. SCC NMSI Receive Timing Diagram

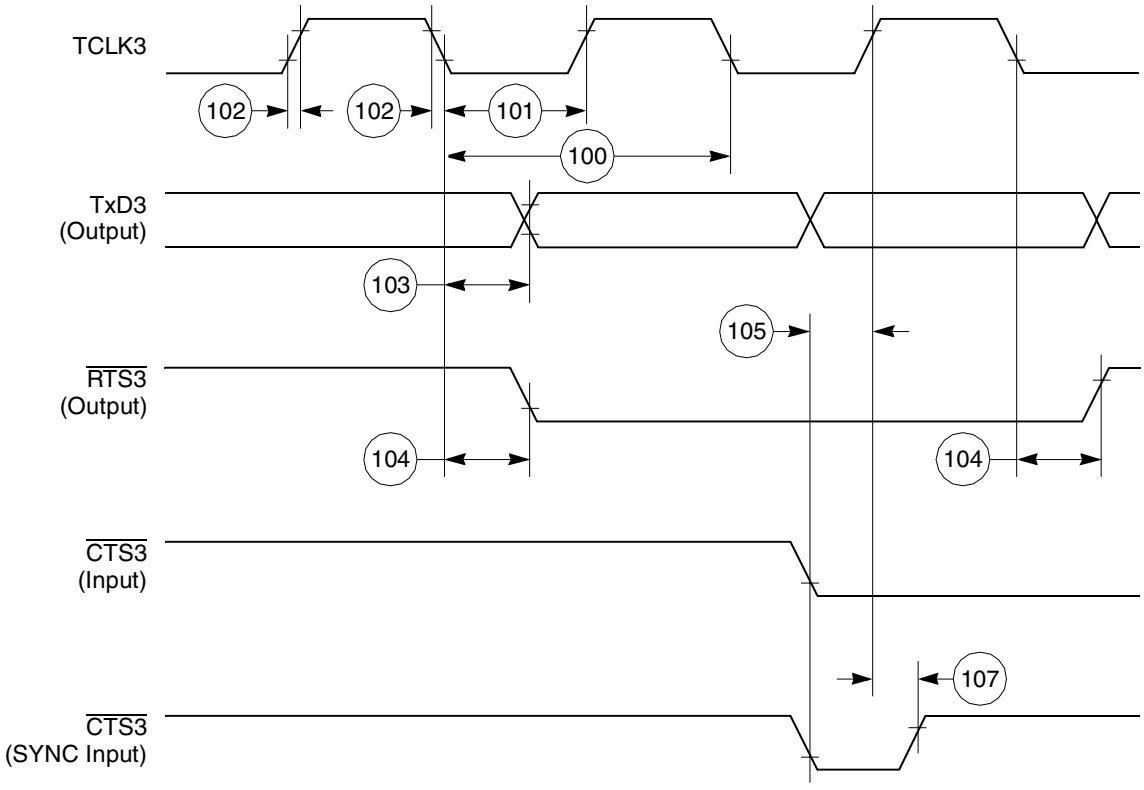

Figure 52. SCC NMSI Transmit Timing Diagram

15 Mechanical Data and Ordering Information

Table 30 identifies the packages and operating frequencies orderable for the MPC853T.

Table 30. MPC853T Package/Frequency Orderable

Package Type	Temperature (Tj)	Frequency (MHz)	Order Number
Plastic ball grid array (VR and ZT suffix)	0°C to 95°C	50	MPC853TVR50 MPC853TZT50
		66	MPC853TVR66 MPC853TZT66
		80	MPC853TVR80 MPC853TZT80
		100	MPC853TVR100 MPC853TZT100
Plastic ball grid array (CVR suffix)	–40°C to 100°C	66	TBD

15.1 Pin Assignments

The following sections give the pinout and pin listing for the JEDEC Compliant and the non-JEDEC versions of the 16 x 16 PBGA package.

15.1.1 The JEDEC Compliant Pinout

Figure 67 shows the JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *MPC866 PowerQUICC Family User's Manual*.

NOTE: This is the top view of the device.

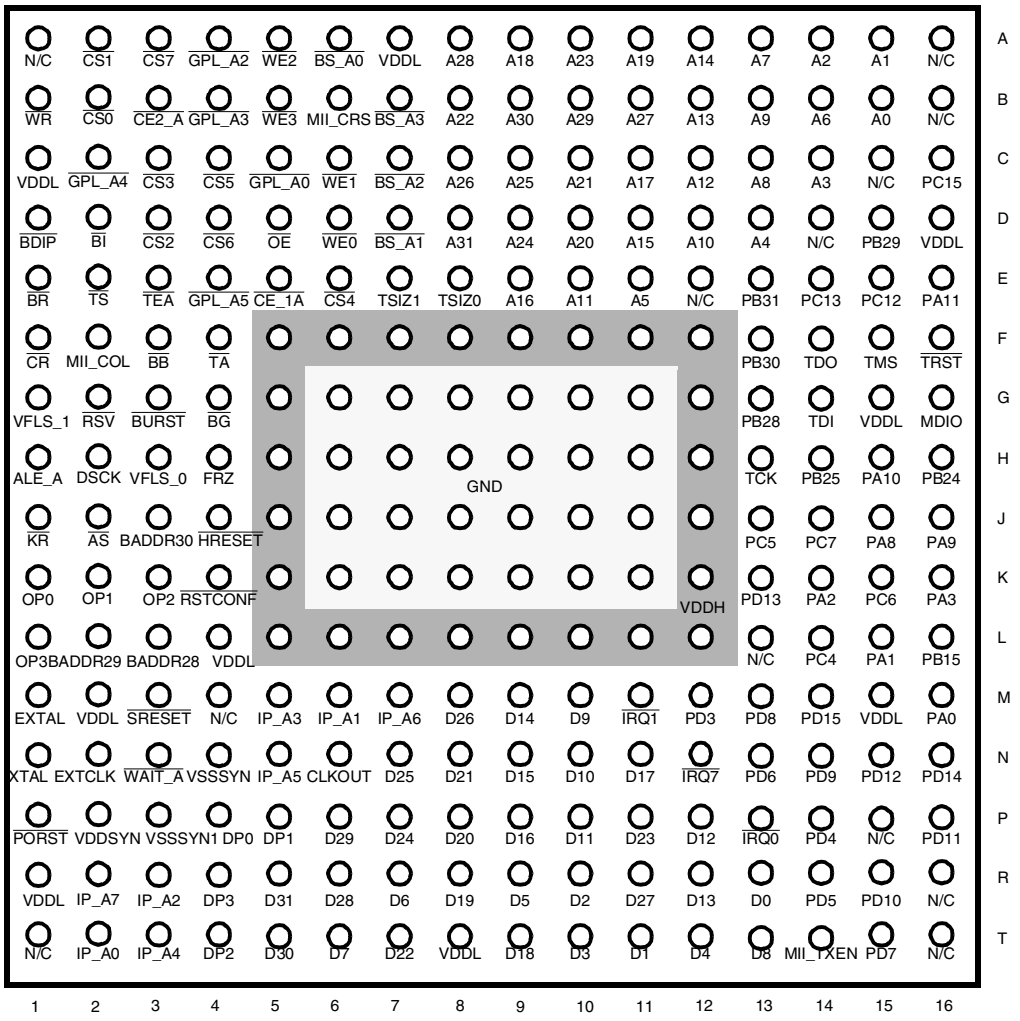

Figure 67. Pinout of the PBGA Package - JEDEC Standard

Table 31 contains a list of the MPC853T input and output signals and shows multiplexing and pin assignments.

Table 31. Pin Assignments - JEDEC Standard

Name	Pin Number	Type
A[0:31]	B15, A15, A14, C14, D13, E11, B14, A13, C13, B13, D12, E10, C12, B12, A12, D11, E9, C11, A9, A11, D10, C10, B8, A10, D9, C9, C8, B11, A8, B10, B9, D8	Bidirectional Three-state (3.3V only)
TSIZ0 REG	E8	Bidirectional Three-state (3.3V only)
TSIZ1	E7	Bidirectional Three-state (3.3V only)
RD/WR	B1	Bidirectional Three-state (3.3V only)

Table 31. Pin Assignments - JEDEC Standard (continued)

Name	Pin Number	Type
BURST	G3	Bidirectional Three-state (3.3V only)
BDIP GPL_B5	D1	Output
TS	E2	Bidirectional Active Pull-up (3.3V only)
TA	F4	Bidirectional Active Pull-up (3.3V only)
TEA	E3	Open-drain
BI	D2	Bidirectional Active Pull-up (3.3V only)
IRQ2 RSV	G2	Bidirectional Three-state (3.3V only)
IRQ4 KR RETRY SPKROUT	J1	Bidirectional Three-state (3.3V only)
CR IRQ3	F1	Input (3.3V only)
D[0:31]	R13, T11, R10, T10, T12, R9, R7, T6, T13, M10, N10, P10, P12, R12, M9, N9, P9, N11, T9, R8, P8, N8, T7, P11, P7, N7, M8, R11, R6, P6, T5, R5	Bidirectional Three-state (3.3V only)
DP0 IRQ3	P4	Bidirectional Three-state (3.3V only)
DP1 IRQ4	P5	Bidirectional Three-state (3.3V only)
DP2 IRQ5	T4	Bidirectional Three-state (3.3V only)
DP3 IRQ6	R4	Bidirectional Three-state (3.3V only)
BR	E1	Bidirectional (3.3V only)
BG	G4	Bidirectional (3.3V only)
BB	F3	Bidirectional Active Pull-up (3.3V only)
FRZ IRQ6	H4	Bidirectional (3.3V only)
IRQ0	P13	Input (3.3V only)
IRQ1	M11	Input (3.3V only)
M_TX_CLK IRQ7	N12	Input (3.3V only)

Table 31. Pin Assignments - JEDEC Standard (continued)

Name	Pin Number	Type
CS[0:5]	B2, A2, D3, C3, E6, C4	Output
CS6	D4	Output
CS7	A3	Output
WE0 BS_B0 IORD	D6	Output
WE1 BS_B1 IOWR	C6	Output
WE2 BS_B2 PCOE	A5	Output
WE3 BS_B3 PCWE	B5	Output
BS_A[0:3]	A6, D7, C7, B7	Output
GPL_A0 GPL_B0	C5	Output
OE GPL_A1 GPL_B1	D5	Output
GPL_A[2:3] GPL_B[2:3] CS[2–3]	A4, B4	Output
UPWAITA GPL_A4	C2	Bidirectional (3.3V only)
GPL_A5	E4	Output
PORESET	P1	Input (3.3V only)
RSTCONF	K4	Input (3.3V only)
HRESET	J4	Open-drain
SRESET	M3	Open-drain
XTAL	N1	Analog Output
EXTAL	M1	Analog Input (1.8V only)
CLKOUT	N6	Output
EXTCLK	N2	Input (1.8V only)
ALE_A	H1	Output
CE1_A	E5	Output
CE2_A	B3	Output

Table 31. Pin Assignments - JEDEC Standard (continued)

Name	Pin Number	Type
$\overline{\text{WAIT\_A}}$	N3	Input (3.3V only)
IP_A0	T2	Input (3.3V only)
IP_A1	M6	Input (3.3V only)
IP_A2 $\overline{\text{IOIS16\_A}}$	R3	Input (3.3V only)
IP_A3	M5	Input (3.3V only)
IP_A4	T3	Input (3.3V only)
IP_A5	N5	Input (3.3V only)
IP_A6	M7	Input (3.3V only)
IP_A7	R2	Input (3.3V only)
DSCK	H2	Bidirectional Three-state (3.3V only)
IWP[0:1] VFLS[0:1]	H3, G1	Bidirectional (3.3V only)
OP0	K1	Bidirectional (3.3V only)
OP1	K2	Output
OP2 MODCK1 $\overline{\text{STS}}$	K3	Bidirectional (3.3V only)
OP3 MODCK2 DSDO	L1	Bidirectional (3.3V only)
BADDR[28:29]	L3, L2	Output
BADDR30 $\overline{\text{REG}}$	J3	Output
$\overline{\text{AS}}$	J2	Input (3.3V only)
PA11 RXD3 L1TXDB	E16	Bidirectional (Optional: Open-drain) (5V tolerant)
PA10 TXD3 L1RXDB	H15	Bidirectional (5V tolerant)
PA9 RXD4	J16	Bidirectional (Optional: Open-drain) (5V tolerant)
PA8 TXD4	J15	Bidirectional (5V tolerant)

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