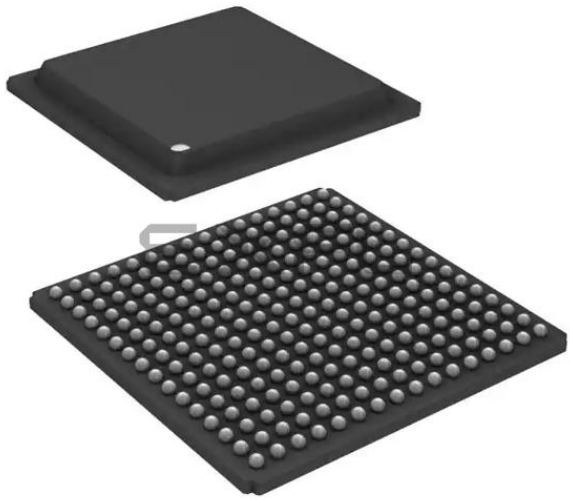

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	100MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc853tzt100a

Table 4. Power Dissipation (P_D)

Die Revision	Bus Mode	Frequency (MHz)	Typical [1]	Maximum [2]	Unit
0	1:1	50	110	140	mW
		66	150	180	mW
	2:1	66	140	160	mW
		80	170	200	mW
		100	210	250	mW

1 Typical power dissipation is measured at 1.9 V.

2 Maximum power dissipation at V_{DDL} and V_{DDSYN} is at 1.9 V, and V_{DDH} is at 3.465 V.

NOTE

Values in Table 4 represent V_{DDL}-based power dissipation and do not include I/O power dissipation over V_{DDH}. I/O power dissipation varies widely by application due to buffer current, which depends on external circuitry.

The V_{DDSYN} power dissipation is negligible.

6 DC Characteristics

Table 5 provides the DC electrical characteristics for the MPC853T.

Table 5. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage	V_{DDH}	3.135	3.465	V
	V_{DDL}	1.7	1.9	V
	V_{DDSYN}	1.7	1.9	V
	Difference between V_{DDL} and V_{DDSYN}	—	100	mV
Input high voltage (all inputs except PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15, PD[3:15], TDI, TDO, TCK, $\overline{\text{TRST}}$, TMS, MII_TXEN, MII_MDIO) [1]	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
EXTAL, EXTCLK input high voltage	V_{IHC}	$0.7 \times V_{DDH}$	V_{DDH}	V
Input leakage current, Vin = 5.5 V (except the TMS, $\overline{\text{TRST}}$, DSCK, and DSDI pins) for 5-V tolerant pins [1]	I_{in}	—	100	µA
Input leakage current, Vin = V_{DDH} (except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI)	I_{In}	—	10	µA
Input leakage current, Vin = 0 V (except the TMS, $\overline{\text{TRST}}$, DSCK, and DSDI)	I_{In}	—	10	µA
Input capacitance [2]	C_{in}	—	20	pF

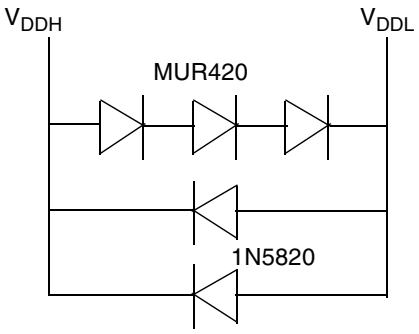

Figure 2. Example Voltage Sequencing Circuit

9 Mandatory Reset Configurations

The MPC853T requires a mandatory configuration during reset.

If hardware reset configuration word (HRCW) is enabled, the HRCW[DBGC] value needs to be set to binary X1 in HRCW, and the SIUMCR[DBGC] should be programmed with the same value in the boot code after reset. This can be done by asserting the $\overline{\text{RSTCONF}}$ during $\overline{\text{HRESET}}$ assertion.

If HRCW is disabled, the SIUMCR[DBGC] should be programmed with binary X1 in the boot code after reset by negating the $\overline{\text{RSTCONF}}$ during the $\overline{\text{HRESET}}$ assertion.

The MBMR[GPLB4DIS], PAPAR, PADIR, PBPAR, PBDIR, PCPAR, and PCDIR registers need to be configured with the mandatory value in Table 6 in the boot code after the reset is negated.

Table 6. Mandatory Reset Configuration of MPC853T

Register/Configuration	Field	Value (binary)
HRCW (Hardware reset configuration word)	HRCW[DBGC]	0bx1
SIUMCR (SIU module configuration register)	SIUMCR[DBGC]	0bx1
MBMR (Machine B mode register)	MBMR[GPLB4DIS}	0
PAPAR (Port A pin assignment register)	PAPAR[4:7] PAPAR[12:15]	0
PADIR (Port A data direction register)	PADIR[4:7] PADIR[12:15]	1
PBPAR (Port B pin assignment register)	PBPAR[14] PBPAR[16:23] PBPAR[26:27]	0
PBDIR (Port B Data direction register)	PBDIR[14] PBDIR[16:23] PBDIR[26:27]	1

Table 6. Mandatory Reset Configuration of MPC853T (continued)

Register/Configuration	Field	Value (binary)
PCPAR (Port C pin assignment register)	PCPAR[8:11] PCDIR[14]	0
PCDIR (Port C data direction register)	PCDIR[8:11] PCDIR[14]	1

10 Layout Practices

Each V_{DD} pin on the MPC853T should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1-µF bypass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized, and additional appropriate decoupling capacitors should be used if required. Capacitor leads and associated printed circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as V_{DD} and GND planes should be used.

All output pins on the MPC853T have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads, as well as parasitic capacitances caused by the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{DD} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, please refer to Section 14.4.3, "Clock Synthesizer Power (V_{DDSYN}, V_{SSSYN}, V_{SSSYN1})" in the *MPC866 PowerQUICC Family User's Manual*.

11 Bus Signal Timing

The maximum bus speed supported by the MPC853T is 66 MHz. Table 7 shows the frequency ranges for standard part frequencies in 1:1 bus mode.

Table 7. Frequency Ranges for Standard Part Frequencies (1:1 Bus Mode)

Part Frequency	50 MHz		66 MHz	
	Min	Max	Min	Max
Core Frequency	40	50	40	66.67
Bus Frequency	40	50	40	66.67

Table 8 shows the frequency ranges for standard part frequencies in 2:1 bus mode.

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B17	CLKOUT to $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ valid (hold time) (MIN = 0.00 × B1 + 1.00 [4])	1.00	—	1.00	—	1.00	—	2.00	—	ns
B17a	CLKOUT to $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) [5] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) [5] (MIN = 0.00 × B1 + 1.00 [6])	1.00	—	1.00	—	1.00	—	2.00	—	ns
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) [7](MIN = 0.00 × B1 + 4.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold Time) [7] (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22a	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MAX = 0.00 × B1 + 8.00)	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22c	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	16.00	7.00	14.10	5.20	12.30	ns
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 (MAX = 0.00 × B1 + 8.00)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11 TRLX = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3)/BS_B[0:3] asserted (MAX = 0.00 × B1 + 9.00)	—	9.00		9.00		9.00		9.00	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B37	UPWAIT valid to CLKOUT falling edge [9] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid [9] (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge [10] (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

1 If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) the maximum allowed jitter on EXTAL can be up to 2%.

2 For part speeds above 50 MHz, use 9.80 ns for B11a.

3 The timing required for $\overline{BR}$ input is relevant when the MPC853T is selected to work with the internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC853T is selected to work with the external bus arbiter.

4 For part speeds above 50 MHz, use 2 ns for B17.

5 The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

6 For part speeds above 50 MHz, use 2 ns for B19.

7 The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.

8 The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

9 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 18.

10 The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 21.

Figure 5 provides the timing for the synchronous output signals.

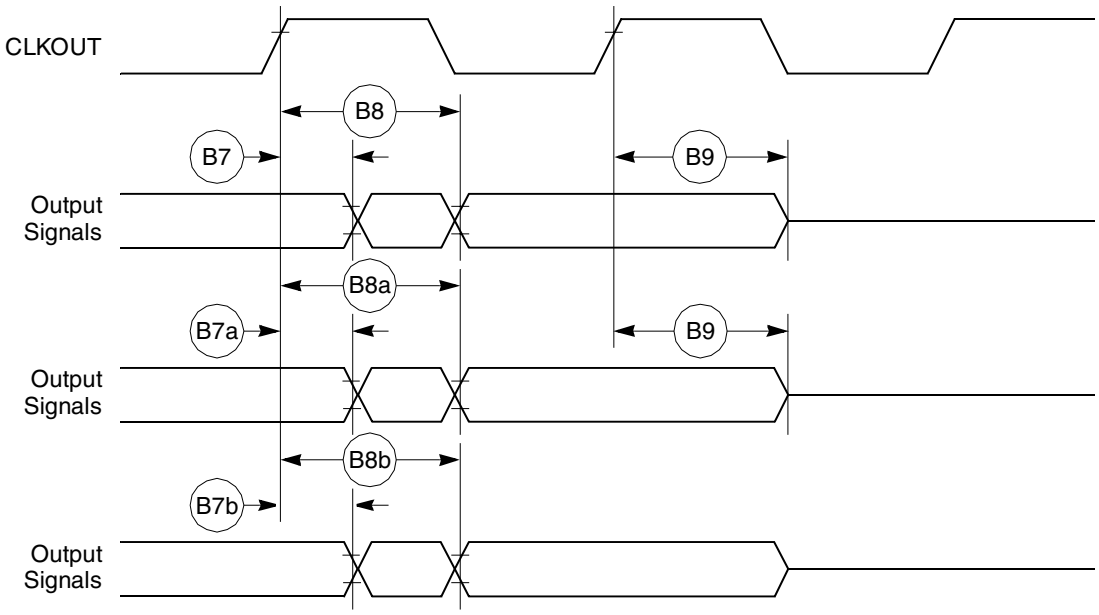

Figure 5. Synchronous Output Signals Timing

Figure 6 provides the timing for the synchronous active pull-up and open-drain output signals.

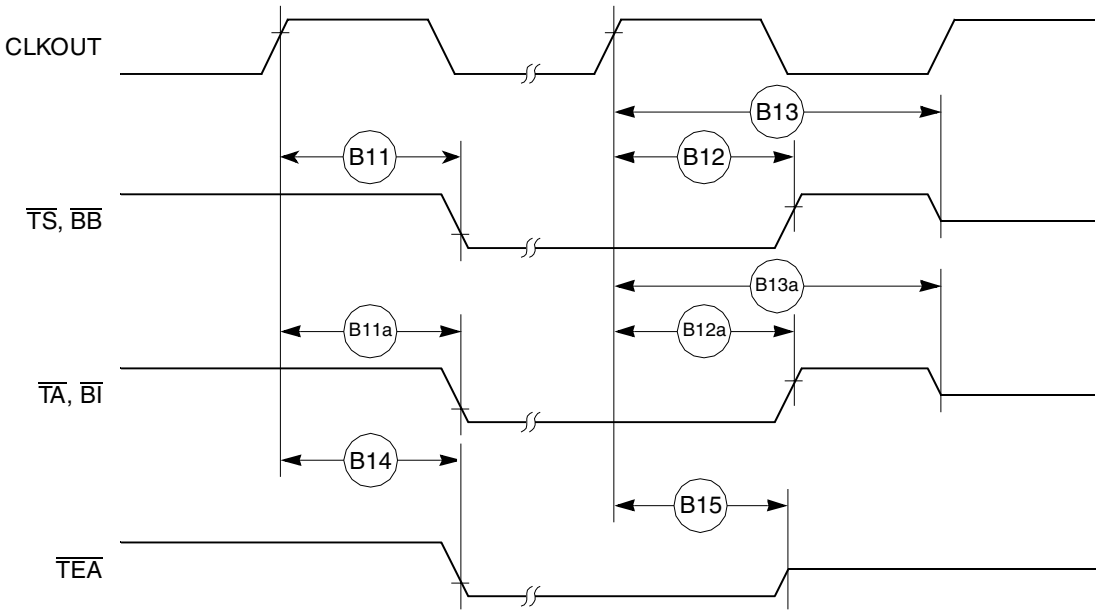

Figure 6. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

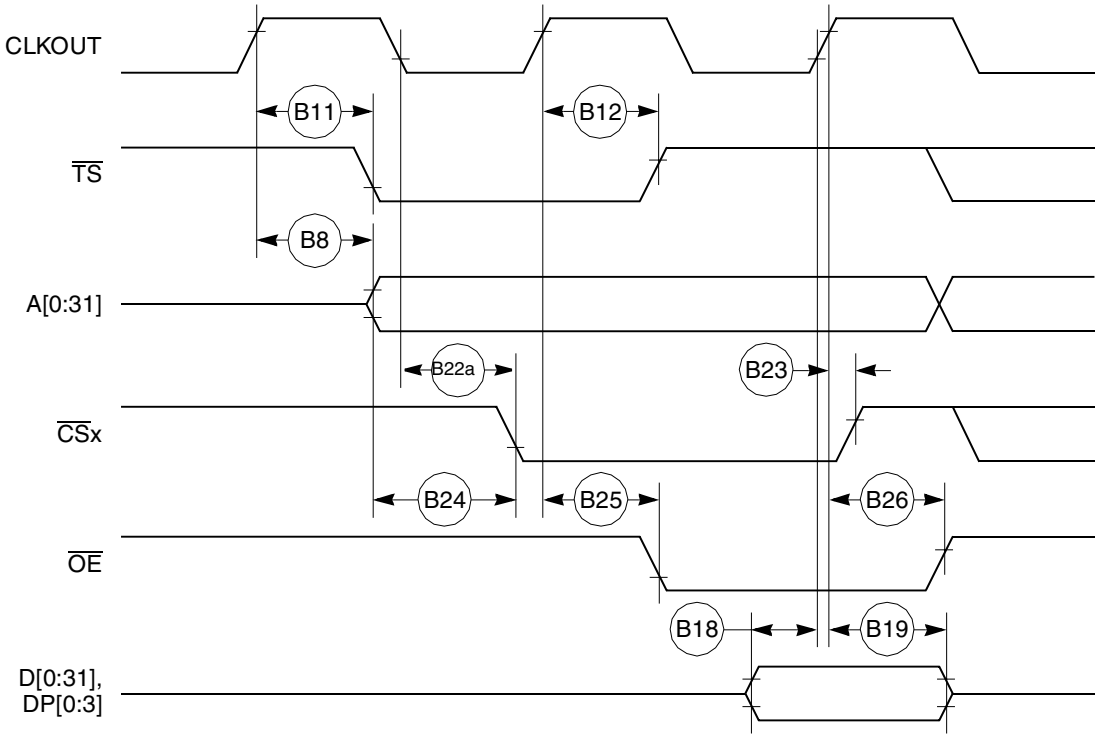

Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

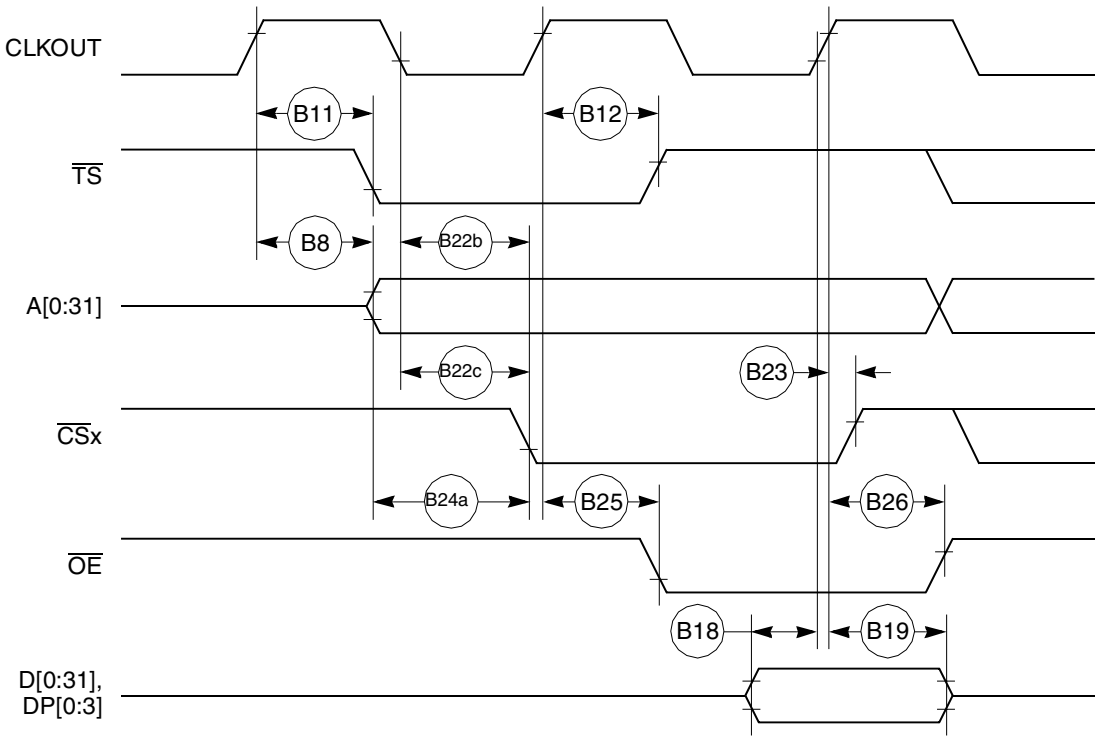

Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

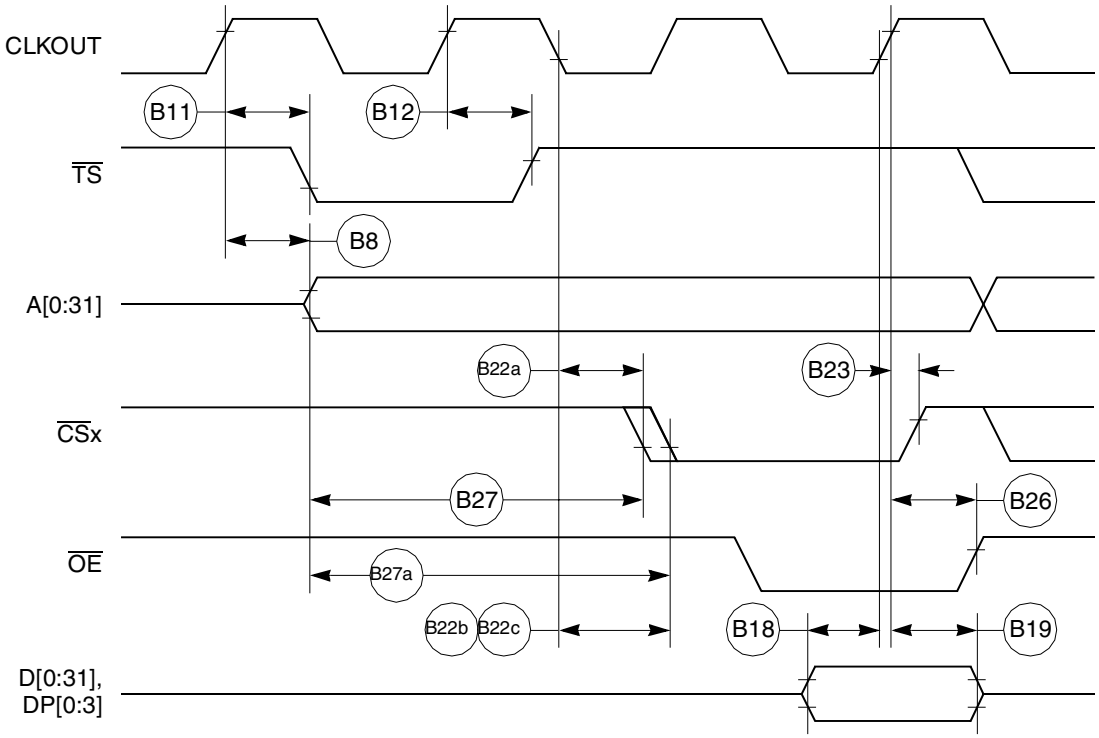

Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10, ACS = 11)

Figure 14 through Figure 16 provide the timing for the external bus write controlled by various GPCM factors.

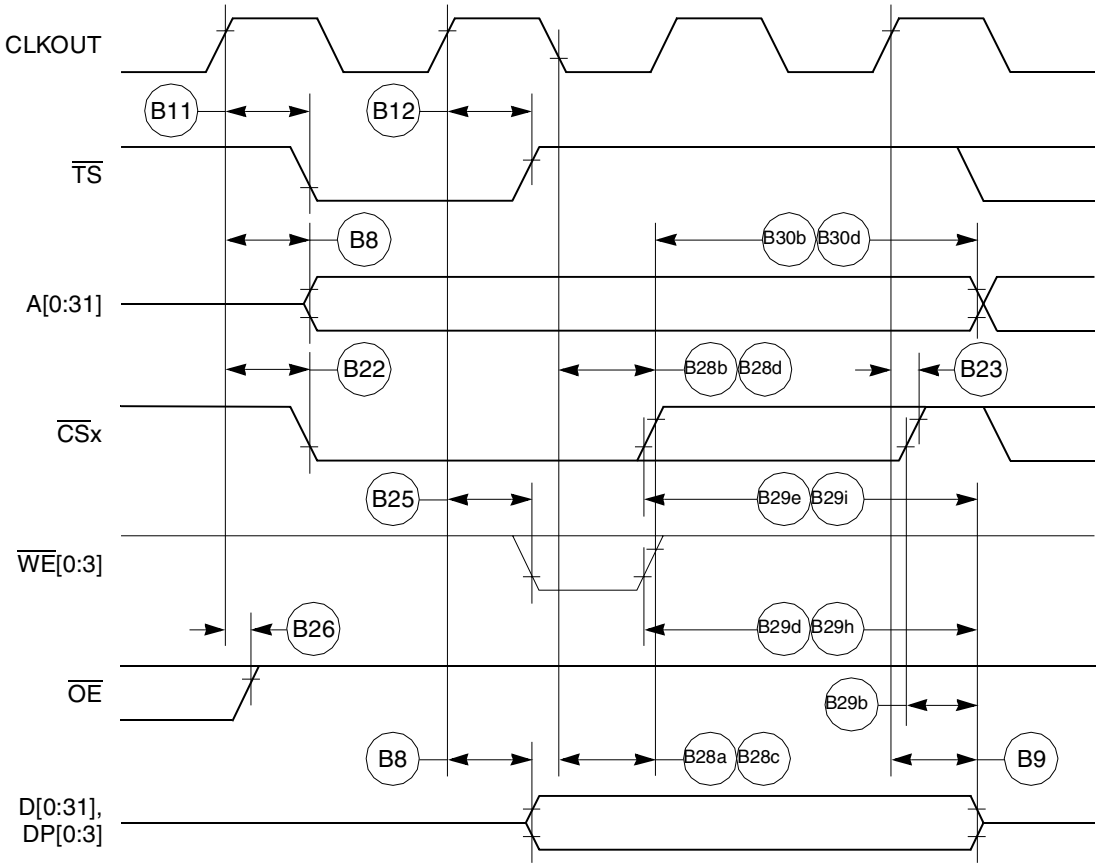

Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

Figure 17 provides the timing for the external bus controlled by the UPM.

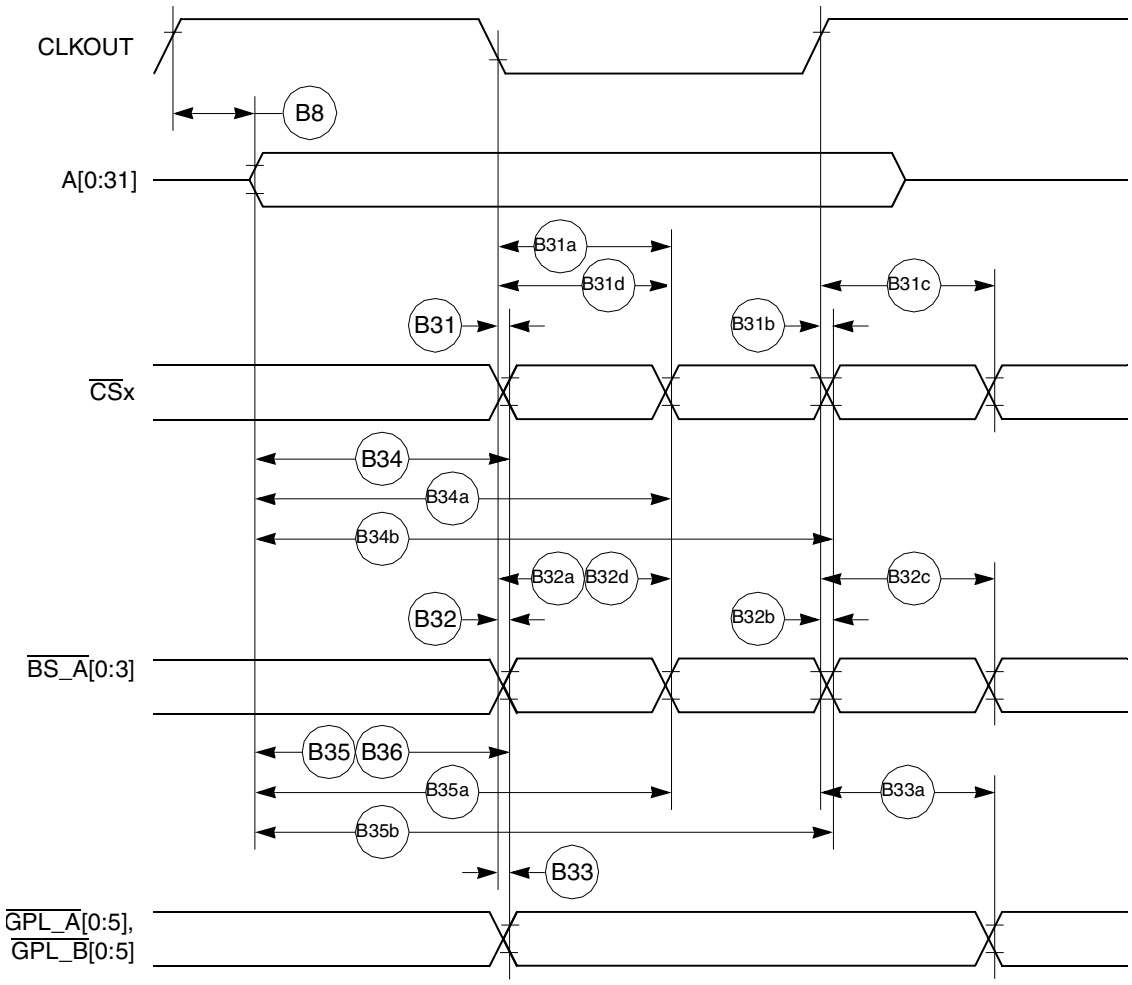

Figure 17. External Bus Timing (UPM-Controlled Signals)

Figure 18 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

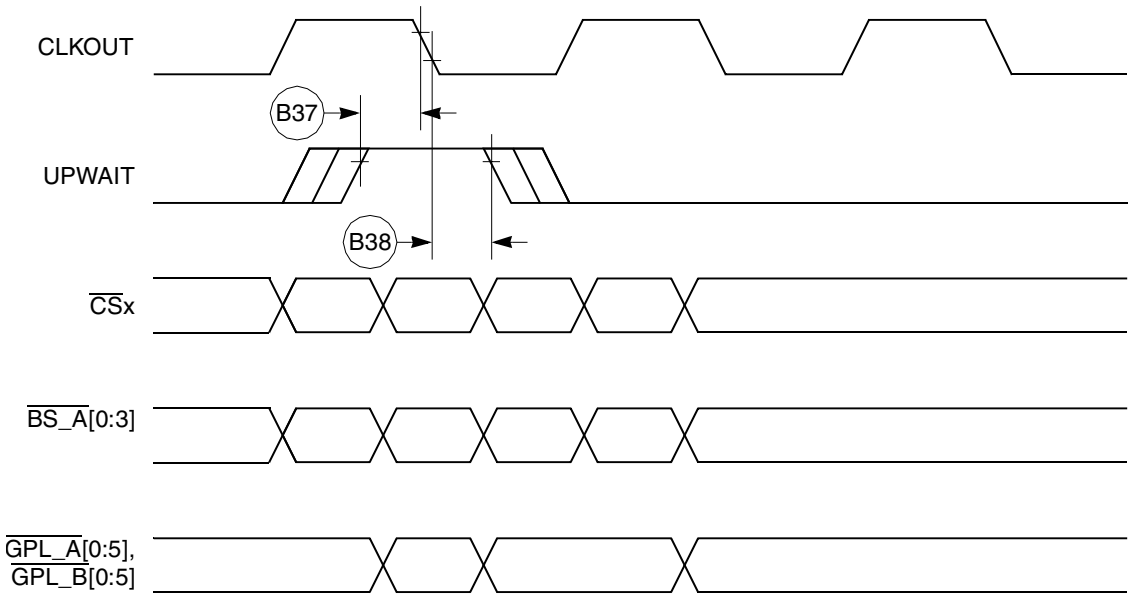

Figure 18. Asynchronous UPWAIT Asserted Detection in UPM-Handled Cycles Timing

Figure 19 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

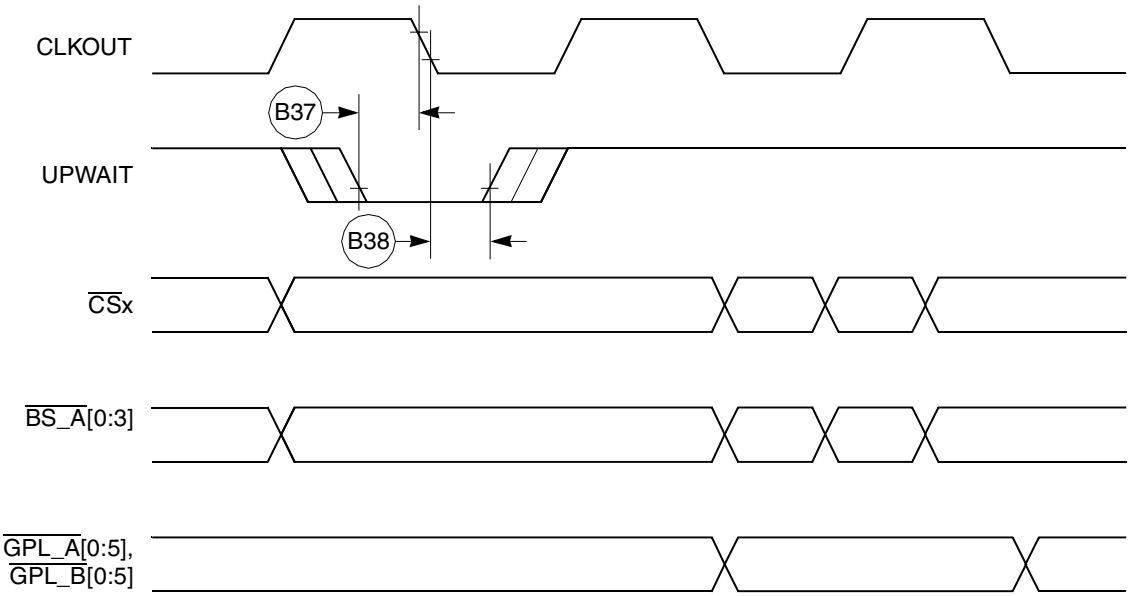

Figure 19. Asynchronous UPWAIT Negated Detection in UPM-Handled Cycles Timing

Figure 32 shows the reset timing for the data bus configuration.

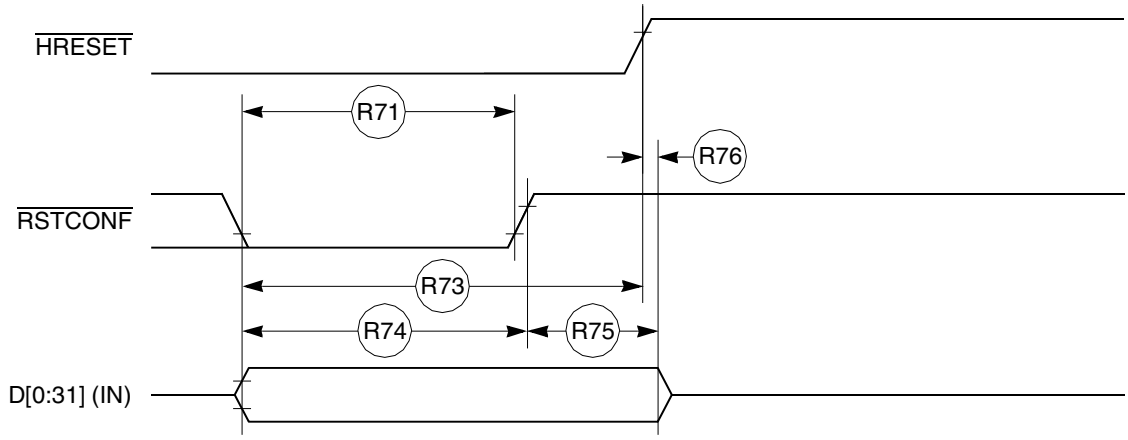

Figure 32. Reset Timing—Configuration from Data Bus

Figure 33 provides the reset timing for the data bus weak drive during configuration.

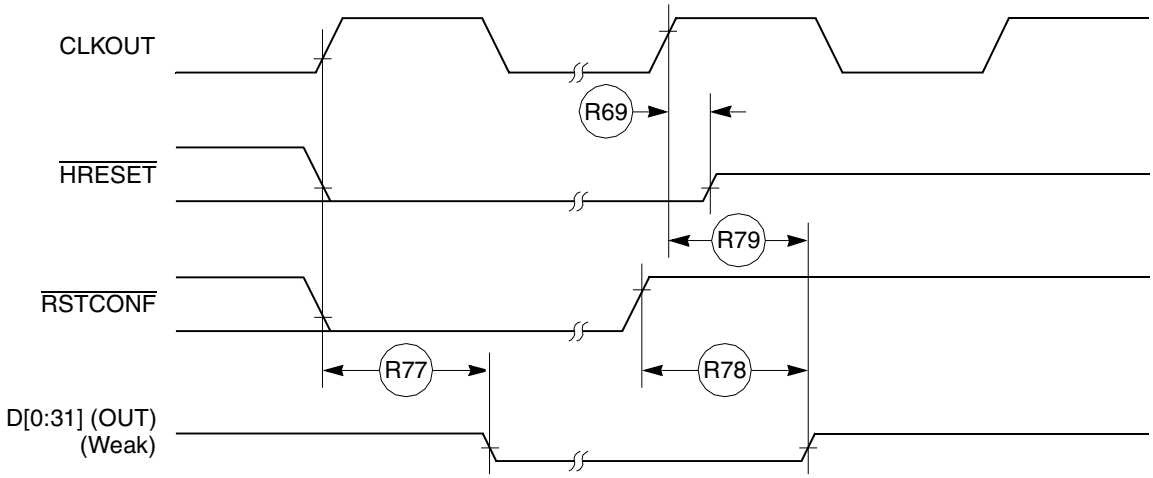

Figure 33. Reset Timing—Data Bus Weak Drive During Configuration

Figure 34 provides the reset timing for the debug port configuration.

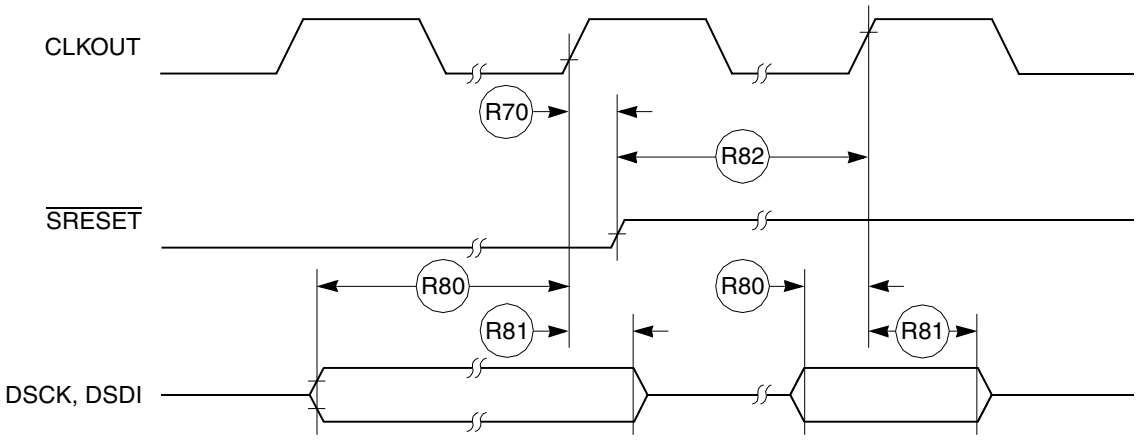

Figure 34. Reset Timing—Debug Port Configuration

12 IEEE 1149.1 Electrical Specifications

Table 15 provides the JTAG timings for the MPC853T shown in Figure 35 to Figure 38.

Table 15. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

Figure 51 through Figure 53 show the NMSI timings.

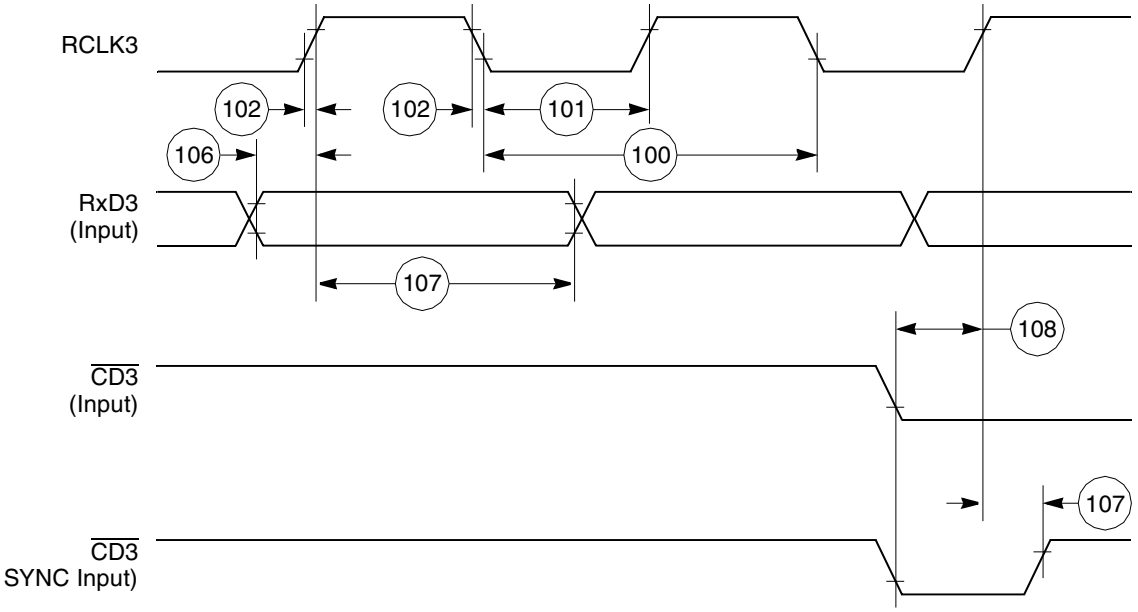

Figure 51. SCC NMSI Receive Timing Diagram

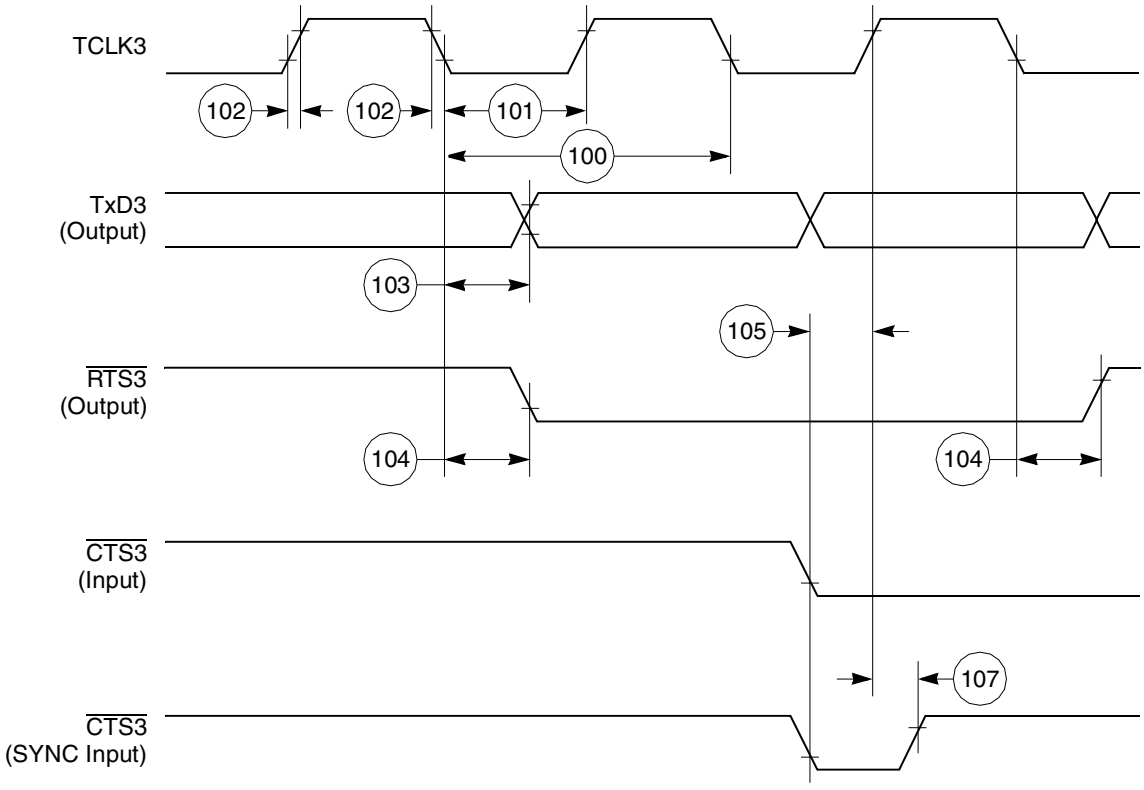

Figure 52. SCC NMSI Transmit Timing Diagram

15 Mechanical Data and Ordering Information

Table 30 identifies the packages and operating frequencies orderable for the MPC853T.

Table 30. MPC853T Package/Frequency Orderable

Package Type	Temperature (Tj)	Frequency (MHz)	Order Number
Plastic ball grid array (VR and ZT suffix)	0°C to 95°C	50	MPC853TVR50 MPC853TZT50
		66	MPC853TVR66 MPC853TZT66
		80	MPC853TVR80 MPC853TZT80
		100	MPC853TVR100 MPC853TZT100
Plastic ball grid array (CVR suffix)	–40°C to 100°C	66	TBD

15.1 Pin Assignments

The following sections give the pinout and pin listing for the JEDEC Compliant and the non-JEDEC versions of the 16 x 16 PBGA package.

15.1.1 The JEDEC Compliant Pinout

Figure 67 shows the JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *MPC866 PowerQUICC Family User's Manual*.

Table 31. Pin Assignments - JEDEC Standard (continued)

Name	Pin Number	Type
BURST	G3	Bidirectional Three-state (3.3V only)
BDIP GPL_B5	D1	Output
TS	E2	Bidirectional Active Pull-up (3.3V only)
TA	F4	Bidirectional Active Pull-up (3.3V only)
TEA	E3	Open-drain
BI	D2	Bidirectional Active Pull-up (3.3V only)
IRQ2 RSV	G2	Bidirectional Three-state (3.3V only)
IRQ4 KR RETRY SPKROUT	J1	Bidirectional Three-state (3.3V only)
CR IRQ3	F1	Input (3.3V only)
D[0:31]	R13, T11, R10, T10, T12, R9, R7, T6, T13, M10, N10, P10, P12, R12, M9, N9, P9, N11, T9, R8, P8, N8, T7, P11, P7, N7, M8, R11, R6, P6, T5, R5	Bidirectional Three-state (3.3V only)
DP0 IRQ3	P4	Bidirectional Three-state (3.3V only)
DP1 IRQ4	P5	Bidirectional Three-state (3.3V only)
DP2 IRQ5	T4	Bidirectional Three-state (3.3V only)
DP3 IRQ6	R4	Bidirectional Three-state (3.3V only)
BR	E1	Bidirectional (3.3V only)
BG	G4	Bidirectional (3.3V only)
BB	F3	Bidirectional Active Pull-up (3.3V only)
FRZ IRQ6	H4	Bidirectional (3.3V only)
IRQ0	P13	Input (3.3V only)
IRQ1	M11	Input (3.3V only)
M_TX_CLK IRQ7	N12	Input (3.3V only)

Table 31. Pin Assignments - JEDEC Standard (continued)

Name	Pin Number	Type
PD5 MII-TXD3	R14	Bidirectional (5V tolerant)
PD4 MII-TXD2	P14	Bidirectional (5V tolerant)
PD3 MII-TXD1	M12	Bidirectional (5V tolerant)
TMS	F15	Input (5V tolerant)
TDI DSDI	G14	Input (5V tolerant)
TCK DSCK	H13	Input (5V tolerant)
$\overline{\text{TRST}}$	F16	Input (5V tolerant)
TDO DSDO	F14	Output (5V tolerant)
MII_CRS	B6	Input
MII_MDIO	G16	Bidirectional (5V tolerant)
MII_TXEN	T14	Output (5V tolerant)
MII_COL	F2	Input
V_{SSSYN}	N4	PLL analog GND
V_{SSSYN1}	P3	PLL analog GND
V_{DDSYN}	P2	PLL analog V_{DD}
GND	G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11	Power
VDDL	A7, C1, D16, G15, L4, M2, R1, M15, T8	Power
VDDH	F5, F6, F7, F8, F9, F10, F11, F12, G5, G12, H5, H12, J5, J12, K5, K12, L5, L6, L7, L8, L9, L10, L11, L12	Power
N/C	A1, A16, B16, C15, D14, E12, L13, M4, P15, R16, T1, T16	No-connect

15.1.2 The Non-JEDEC Pinout

Figure 68 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *MPC866 PowerQUICC Family User's Manual*.

Table 32. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
IRQ0	R14	Input (3.3 V only)
IRQ1	N12	Input (3.3 V only)
IRQ7 M_TX_CLK	P13	Input (3.3 V only)
CS[0:5]	C3, B3, E4, D4, F7, D5	Output
CS6	E5	Output
CS7	B4	Output
WE0 BS_B0 IORD	E7	Output
WE1 BS_B1 IOWR	D7	Output
WE2 BS_B2 PCOE	B6	Output
WE3 BS_B3 PCWE	C6	Output
BS_A[0:3]	B7, E8, D8, C8	Output
GPL_A0 GPL_B0	D6	Output
OE GPL_A1 GPL_B1	E6	Output
GPL_A[2:3] GPL_B[2:3] CS[2–3]	B5, C5	Output
UPWAITA GPL_A4	D3	Bidirectional (3.3 V only)
GPL_A5	F5	Output
PORESET	R2	Input (3.3 V only)
RSTCONF	L5	Input (3.3 V only)
HRESET	K5	Open drain
SRESET	N4	Open drain
XTAL	P2	Analog output
EXTAL	N2	Analog Input (3.3 V only)

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