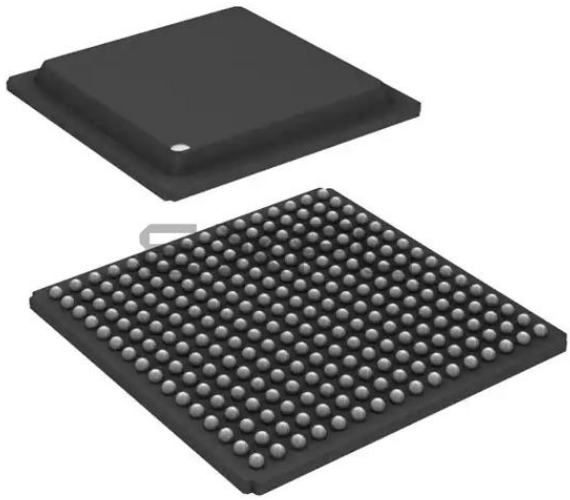

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	166MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc853tzt66a

- SPI (serial peripheral interface)
  - Supports master and slave modes
  - Supports multiple-master operation on the same bus
- The MPC853T has a time-slot assigner (TSA) that supports one TDM bus (TDMb)
  - Allows SCCs and SMC to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame synchronization, and clocking
  - Allows dynamic changes
  - Can be internally connected to three serial channels (two SCCs and one SMC)
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant
  - Supports one independent PCMCIA socket, 8 memory or I/O windows
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a break point internally
- Normal high and normal low power modes to conserve power
- 1.8-V core and 3.3-V I/O operation with 5-V TTL compatibility. Refer to Table 5 for a listing of the 5-V tolerant pins.

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC853T. Table 1 provides the maximum ratings and the operating temperatures.

Table 1. Maximum Tolerated Ratings

Rating	Symbol	Value	Unit
Supply voltage [1]	V_{DDL} (core voltage)	–0.3 to 3.4	V
	V_{DDH} (I/O voltage)	–0.3 to 4	V
	V_{DDSYN}	–0.3 to 3.4	V
	Difference between V_{DDL} and V_{DDSYN}	100	mV
Input voltage [2]	V_{in}	GND–0.3 to V_{DDH}	V
Storage temperature range	T_{stg}	–55 to +150	°C

1 The power supply of the device must start its ramp from 0.0 V.

2 Functional operating conditions are provided with the DC electrical specifications in Table 5. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than V_{DDH}. This restriction applies to power up and normal operation (that is, if the MPC853T is unpowered, a voltage greater than 2.5 V must not be applied to its inputs).

Table 2. Operating Temperatures

Rating	Symbol	Value	Unit
Temperature [1] (standard)	$T_{A(min)}$	0	°C
	$T_{j(max)}$	95	°C
Temperature (extended)	$T_{A(min)}$	–40	°C
	$T_{j(max)}$	100	°C

1 Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_j.

This device contains circuitry protecting against damage caused by high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND, V_{DDL}, or V_{DDH}).

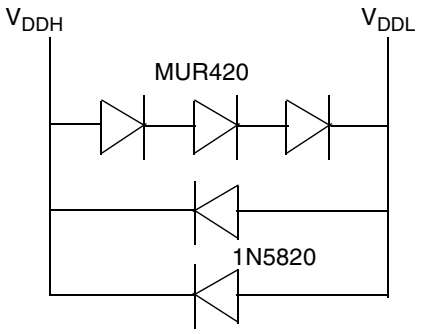

Figure 2. Example Voltage Sequencing Circuit

9 Mandatory Reset Configurations

The MPC853T requires a mandatory configuration during reset.

If hardware reset configuration word (HRCW) is enabled, the HRCW[DBGC] value needs to be set to binary X1 in HRCW, and the SIUMCR[DBGC] should be programmed with the same value in the boot code after reset. This can be done by asserting the $\overline{\text{RSTCONF}}$ during $\overline{\text{HRESET}}$ assertion.

If HRCW is disabled, the SIUMCR[DBGC] should be programmed with binary X1 in the boot code after reset by negating the $\overline{\text{RSTCONF}}$ during the $\overline{\text{HRESET}}$ assertion.

The MBMR[GPLB4DIS], PAPAR, PADIR, PBPAR, PBDIR, PCPAR, and PCDIR registers need to be configured with the mandatory value in Table 6 in the boot code after the reset is negated.

Table 6. Mandatory Reset Configuration of MPC853T

Register/Configuration	Field	Value (binary)
HRCW (Hardware reset configuration word)	HRCW[DBGC]	0bx1
SIUMCR (SIU module configuration register)	SIUMCR[DBGC]	0bx1
MBMR (Machine B mode register)	MBMR[GPLB4DIS}	0
PAPAR (Port A pin assignment register)	PAPAR[4:7] PAPAR[12:15]	0
PADIR (Port A data direction register)	PADIR[4:7] PADIR[12:15]	1
PBPAR (Port B pin assignment register)	PBPAR[14] PBPAR[16:23] PBPAR[26:27]	0
PBDIR (Port B Data direction register)	PBDIR[14] PBDIR[16:23] PBDIR[26:27]	1

Table 6. Mandatory Reset Configuration of MPC853T (continued)

Register/Configuration	Field	Value (binary)
PCPAR (Port C pin assignment register)	PCPAR[8:11] PCDIR[14]	0
PCDIR (Port C data direction register)	PCDIR[8:11] PCDIR[14]	1

10 Layout Practices

Each V_{DD} pin on the MPC853T should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1-µF bypass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized, and additional appropriate decoupling capacitors should be used if required. Capacitor leads and associated printed circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as V_{DD} and GND planes should be used.

All output pins on the MPC853T have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads, as well as parasitic capacitances caused by the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{DD} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, please refer to Section 14.4.3, "Clock Synthesizer Power (V_{DDSYN}, V_{SSSYN}, V_{SSSYN1})" in the *MPC866 PowerQUICC Family User's Manual*.

11 Bus Signal Timing

The maximum bus speed supported by the MPC853T is 66 MHz. Table 7 shows the frequency ranges for standard part frequencies in 1:1 bus mode.

Table 7. Frequency Ranges for Standard Part Frequencies (1:1 Bus Mode)

Part Frequency	50 MHz		66 MHz	
	Min	Max	Min	Max
Core Frequency	40	50	40	66.67
Bus Frequency	40	50	40	66.67

Table 8 shows the frequency ranges for standard part frequencies in 2:1 bus mode.

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B26	CLKOUT rising edge to $\overline{OE}$ negated (MAX = 0.00 × B1 + 9.00)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 × B1 – 2.00)	35.90	—	29.30	—	23.00	—	16.90	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B28	CLKOUT rising edge to $\overline{WE}$(0:3)/BS_B[0:3] negated GPCM write access CSNT = 0 (MAX = 0.00 × B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$(0:3)/BS_B[0:3] negated GPCM write access TRLX = 0,1 CSNT = 1, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	—	14.30	—	13.00	—	11.80	—	10.50	ns
B28c	CLKOUT falling edge to $\overline{WE}$(0:3)/BS_B[0:3] negated GPCM write access TRLX = 0,1 CSNT = 1 write access TRLX = 0,1 CSNT = 1, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	—	18.00	—	18.00	—	14.30	—	12.30	ns
B29	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B29a	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B29b	$\overline{CS}$ negated to D(0:31), DP(0:3), High-Z GPCM write access, ACS = 00, TRLX = 0,1 & CSNT = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns

Figure 5 provides the timing for the synchronous output signals.

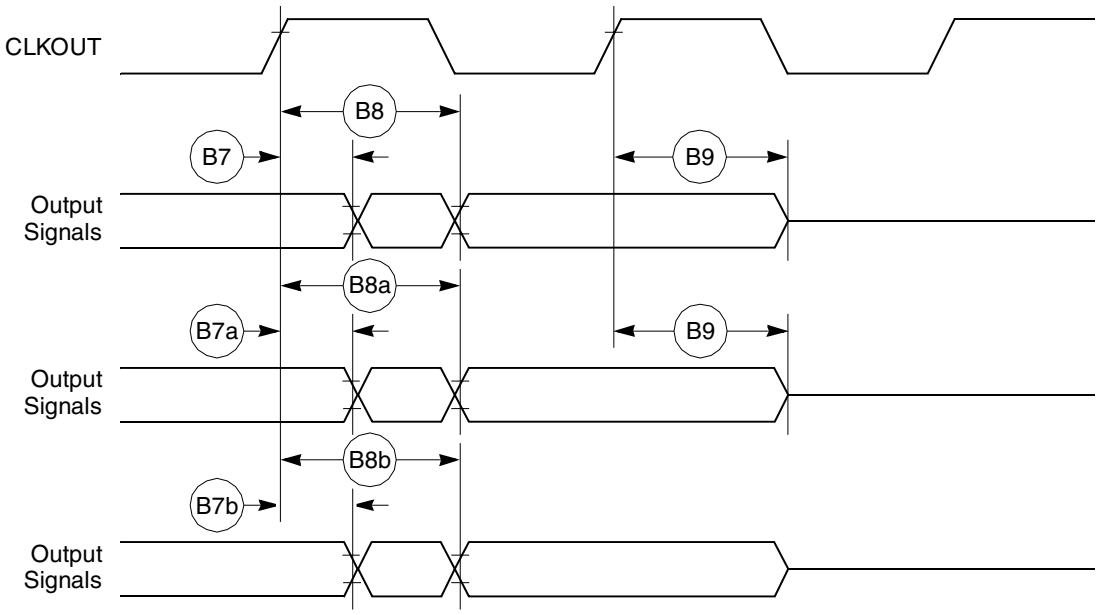

Figure 5. Synchronous Output Signals Timing

Figure 6 provides the timing for the synchronous active pull-up and open-drain output signals.

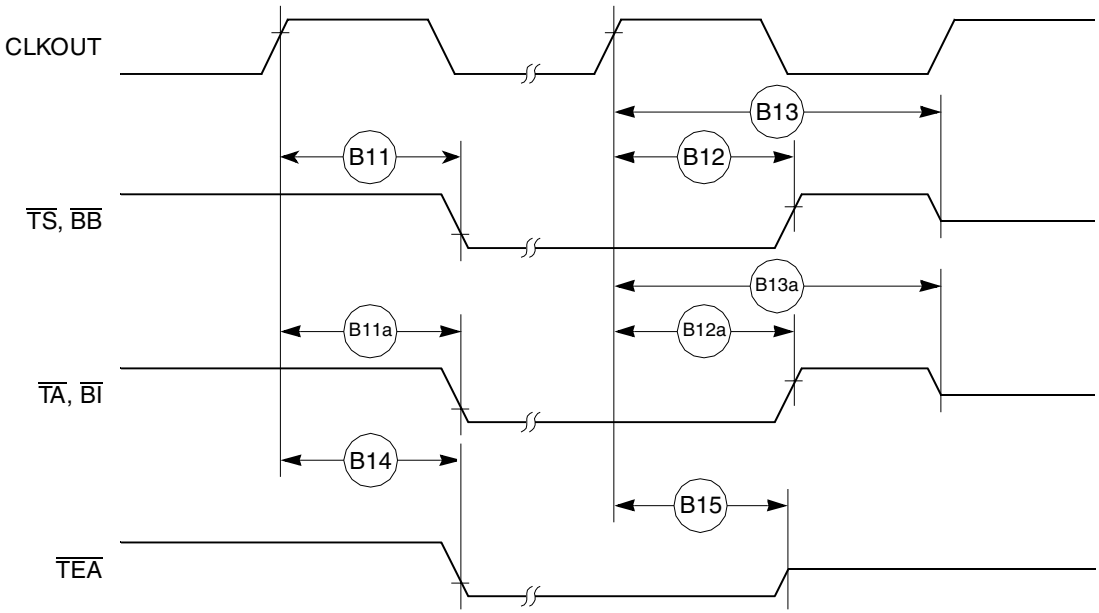

Figure 6. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

Figure 9 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

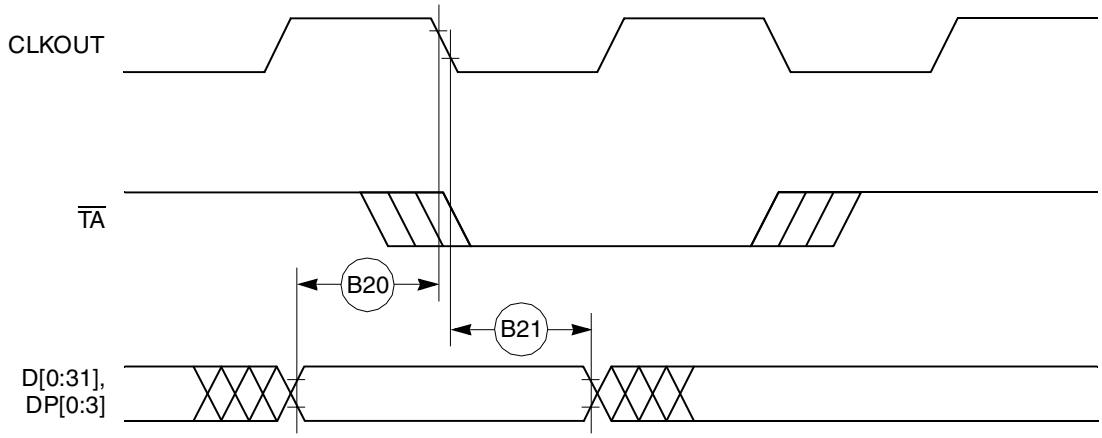

Figure 9. Input Data Timing When Controlled by the UPM in the Memory Controller and DLT3 = 1

Figure 10 through Figure 13 provide the timing for the external bus read controlled by various GPCM factors.

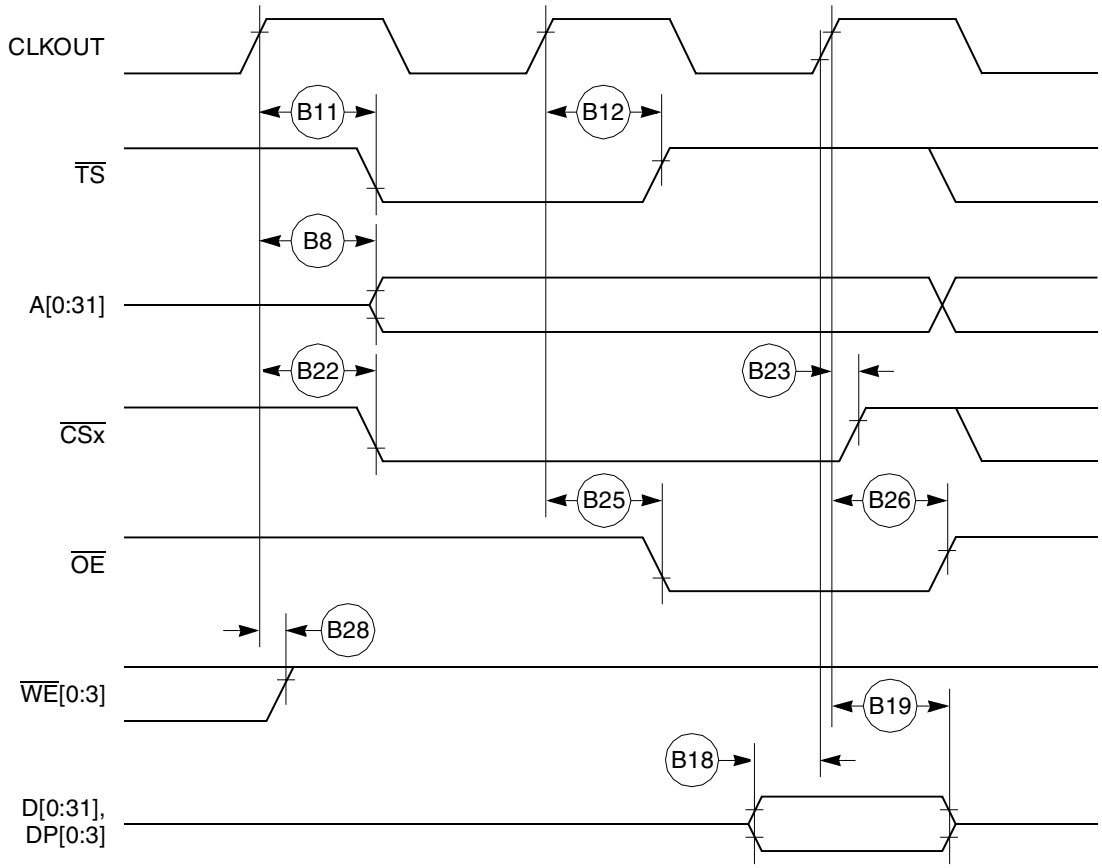

Figure 10. External Bus Read Timing (GPCM Controlled—ACS = 00)

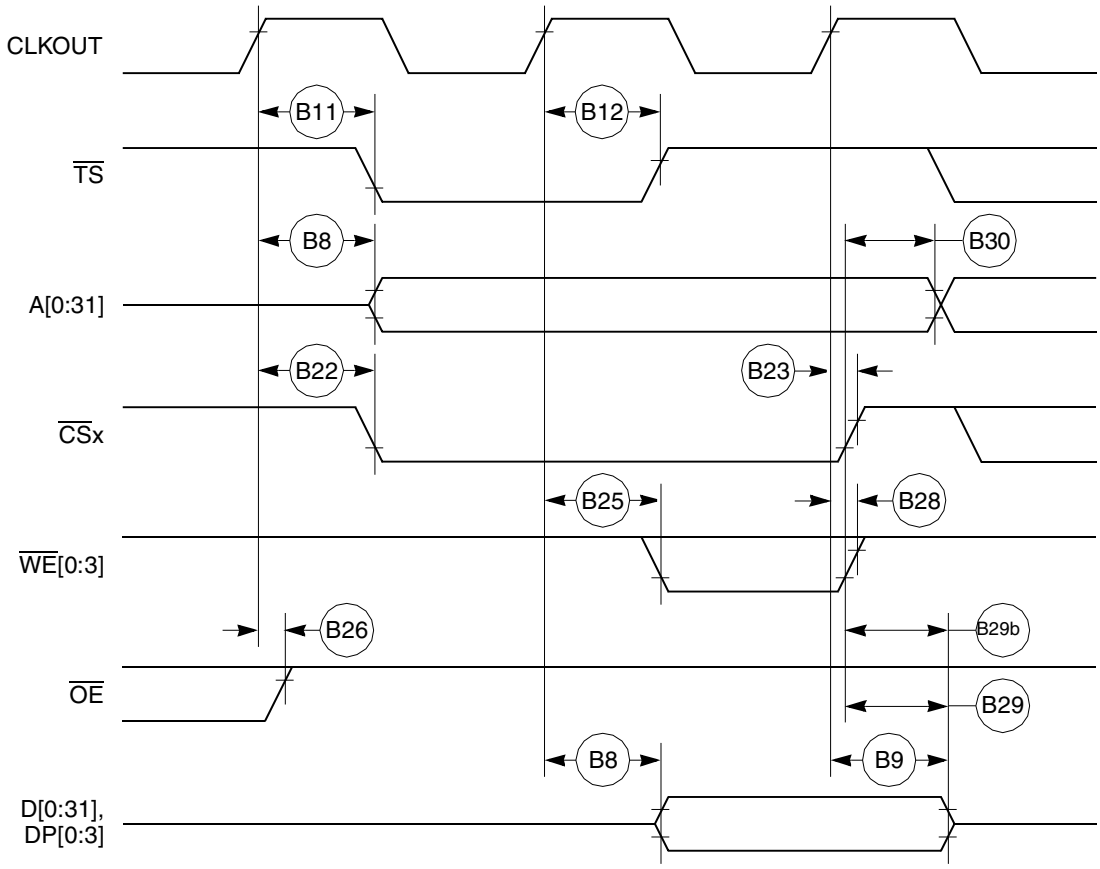

Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 0)

Table 11 shows the PCMCIA timing for the MPC853T.

Table 11. PCMCIA Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
J82	A(0:31), $\overline{\text{REG}}$ valid to PCMCIA strobe asserted [1] (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
J83	A(0:31), $\overline{\text{REG}}$ valid to ALE negation[1] (MIN = 1.00 × B1 – 2.00)	28.30	—	23.00	—	18.00	—	13.20	—	ns
J84	CLKOUT to $\overline{\text{REG}}$ valid (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
J85	CLKOUT to $\overline{\text{REG}}$ invalid (MIN = 0.25 × B1 + 1.00)	8.60	—	7.30	—	6.00	—	4.80	—	ns
J86	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
J87	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
J88	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time (MAX = 0.00 × B1 + 11.00)	—	11.00	—	11.00	—	11.00	—	11.00	ns
J89	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time (MAX = 0.00 × B1 + 11.00)	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
J90	CLKOUT to ALE assert time (MAX = 0.25 × B1 + 6.30)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
J91	CLKOUT to ALE negate time (MAX = 0.25 × B1 + 8.00)	—	15.60	—	14.30	—	13.00	—	11.80	ns
J92	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid[1] (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
J93	$\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge[1] (MIN = 0.00 × B1 + 8.00)	8.00	—	8.00	—	8.00	—	8.00	—	ns
J94	CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid[1] (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns

1 PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the $\overline{\text{WAITA}}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAITA}}$ assertion will be effective only if it is detected two cycles before the PSL timer expiration. See the Chapter 16, “PCMCIA Interface,” in the *MPC866 PowerQUICC Family User’s Manual*.

Figure 26 provides the PCMCIA access cycle timing for the external bus write.

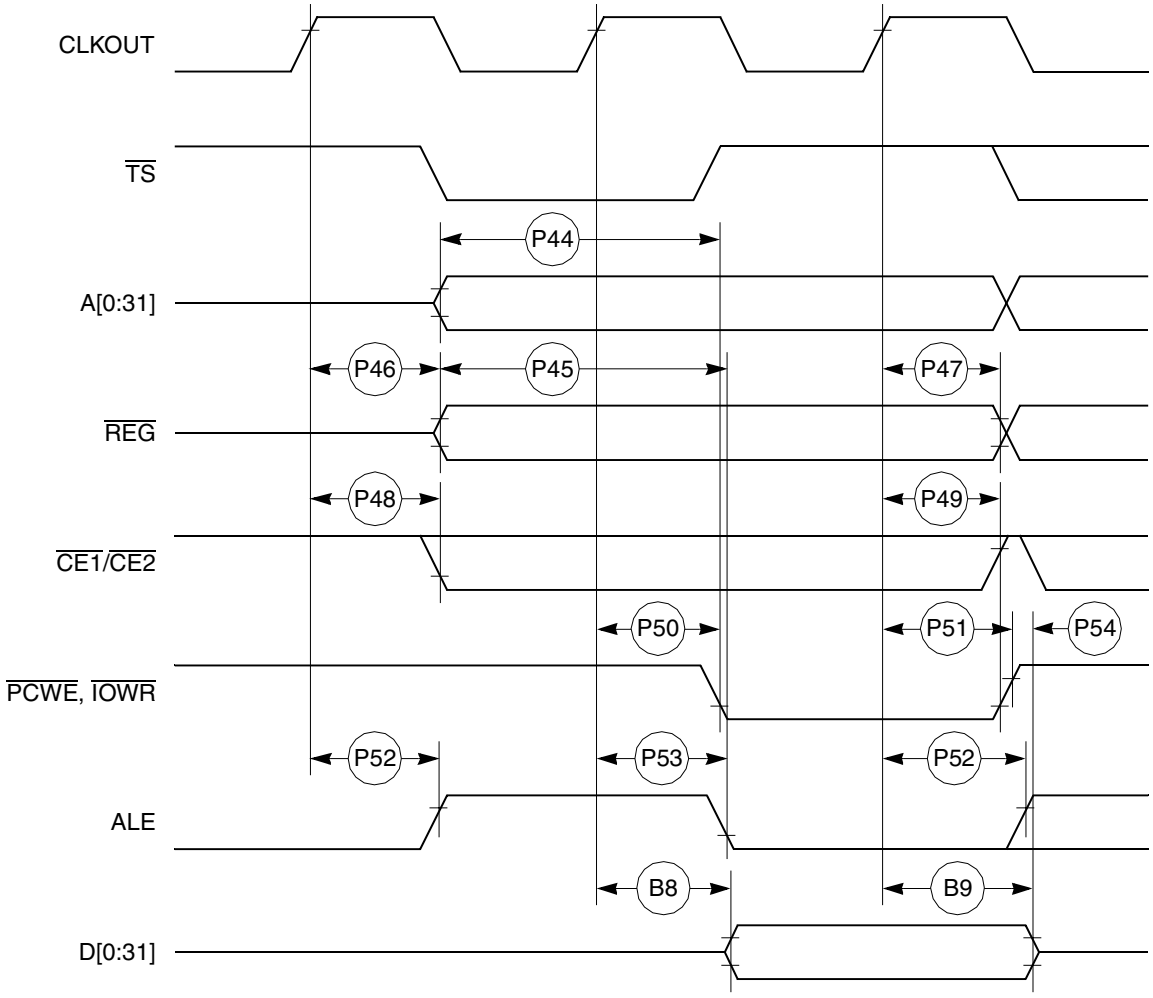

Figure 26. PCMCIA Access Cycles Timing External Bus Write

Figure 27 provides the PCMCIA WAIT signals detection timing.

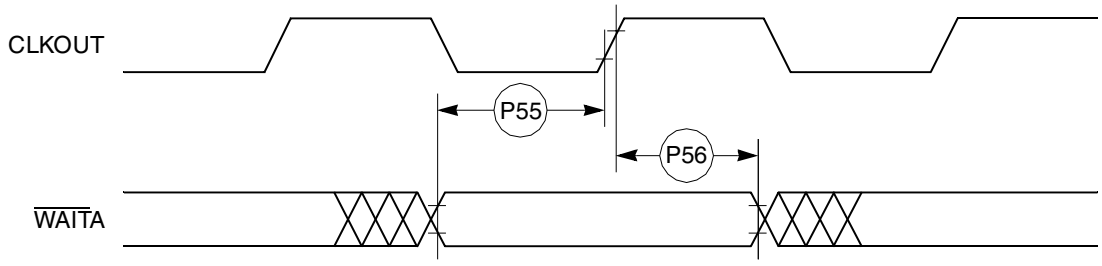

Figure 27. PCMCIA WAIT Signals Detection Timing

Figure 32 shows the reset timing for the data bus configuration.

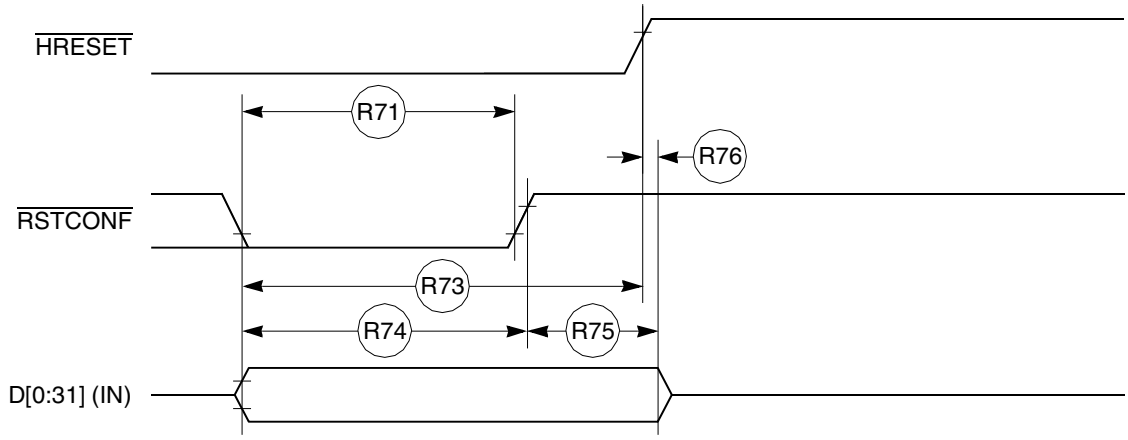

Figure 32. Reset Timing—Configuration from Data Bus

Figure 33 provides the reset timing for the data bus weak drive during configuration.

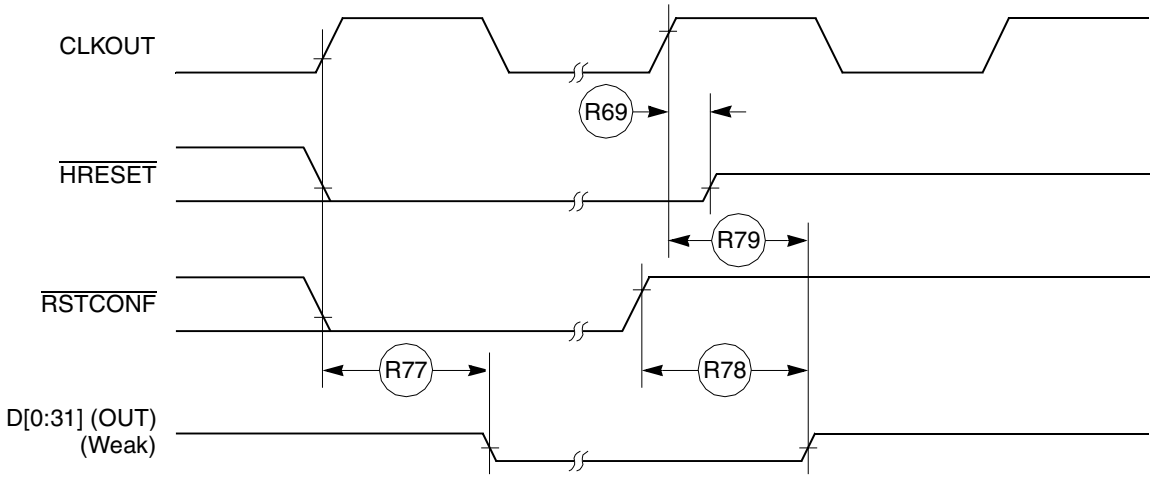

Figure 33. Reset Timing—Data Bus Weak Drive During Configuration

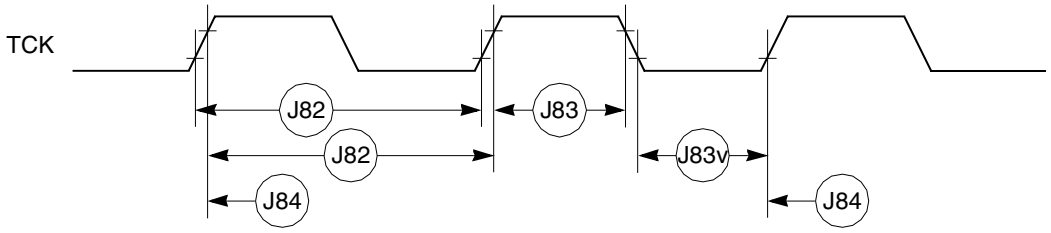

Figure 35. JTAG Test Clock Input Timing

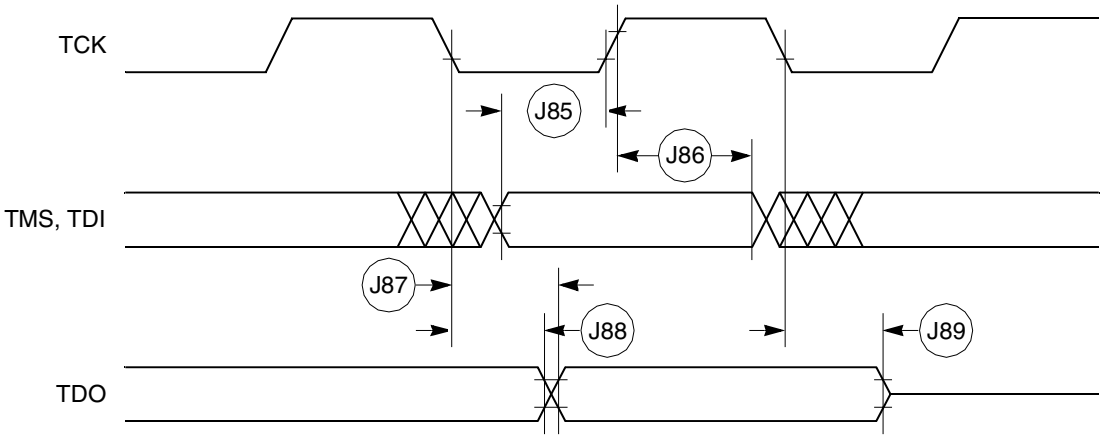

Figure 36. JTAG Test Access Port Timing Diagram

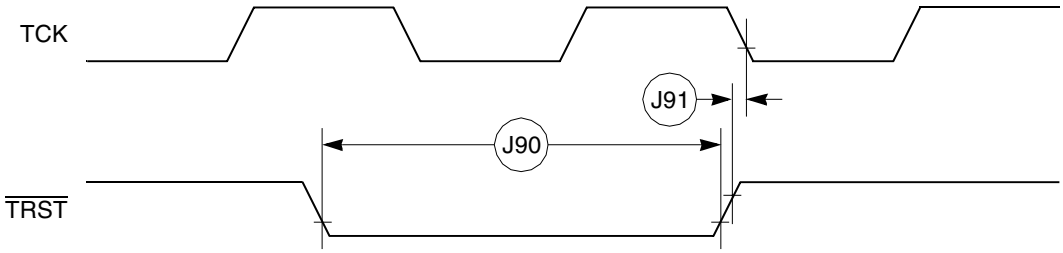

Figure 37. JTAG $\overline{\text{TRST}}$ Timing Diagram

Table 20. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
75	L1RSYNCB, L1TSYNCB rise/fall time	—	15.00	ns
76	L1RXDB valid to L1CLKB edge (L1RXDB setup time)	17.00	—	ns
77	L1CLKB edge to L1RXDB invalid (L1RXDB hold time)	13.00	—	ns
78	L1CLKB edge to L1ST1 and L1ST2 valid [4]	10.00	45.00	ns
78A	L1SYNCB valid to L1ST1 and L1ST2 valid	10.00	45.00	ns
79	L1CLKB edge to L1ST1 and L1ST2 invalid	10.00	45.00	ns
80	L1CLKB edge to L1TXDB valid	10.00	55.00	ns
80A	L1TSYNCB valid to L1TXDB valid [4]	10.00	55.00	ns
81	L1CLKB edge to L1TXDB high impedance	0.00	42.00	ns
82	L1RCLKB, L1TCLKB frequency (DSC =1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLKB, L1TCLKB width low (DSC =1)	P + 10	—	ns
83a	L1RCLKB, L1TCLKB width high (DSC = 1)[3]	P + 10	—	ns
84	L1CLKB edge to L1CLKOB valid (DSC = 1)	—	30.00	ns
85	$\overline{\text{L1RQB}}$ valid before falling edge of L1TSYNCB[4]	1.00	—	L1TCLK
86	L1GRB setup time[2]	42.00	—	ns
87	L1GRB hold time	42.00	—	ns
88	L1CLKB edge to L1SYNCB valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

1 The ratio SyncCLK/L1RCLKB must be greater than 2.5/1.

2 These specs are valid for IDL mode only.

3 Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.

4 These strobes and TxD on the first bit of the frame become valid after L1CLKB edge or L1SYNCB, whichever comes later.

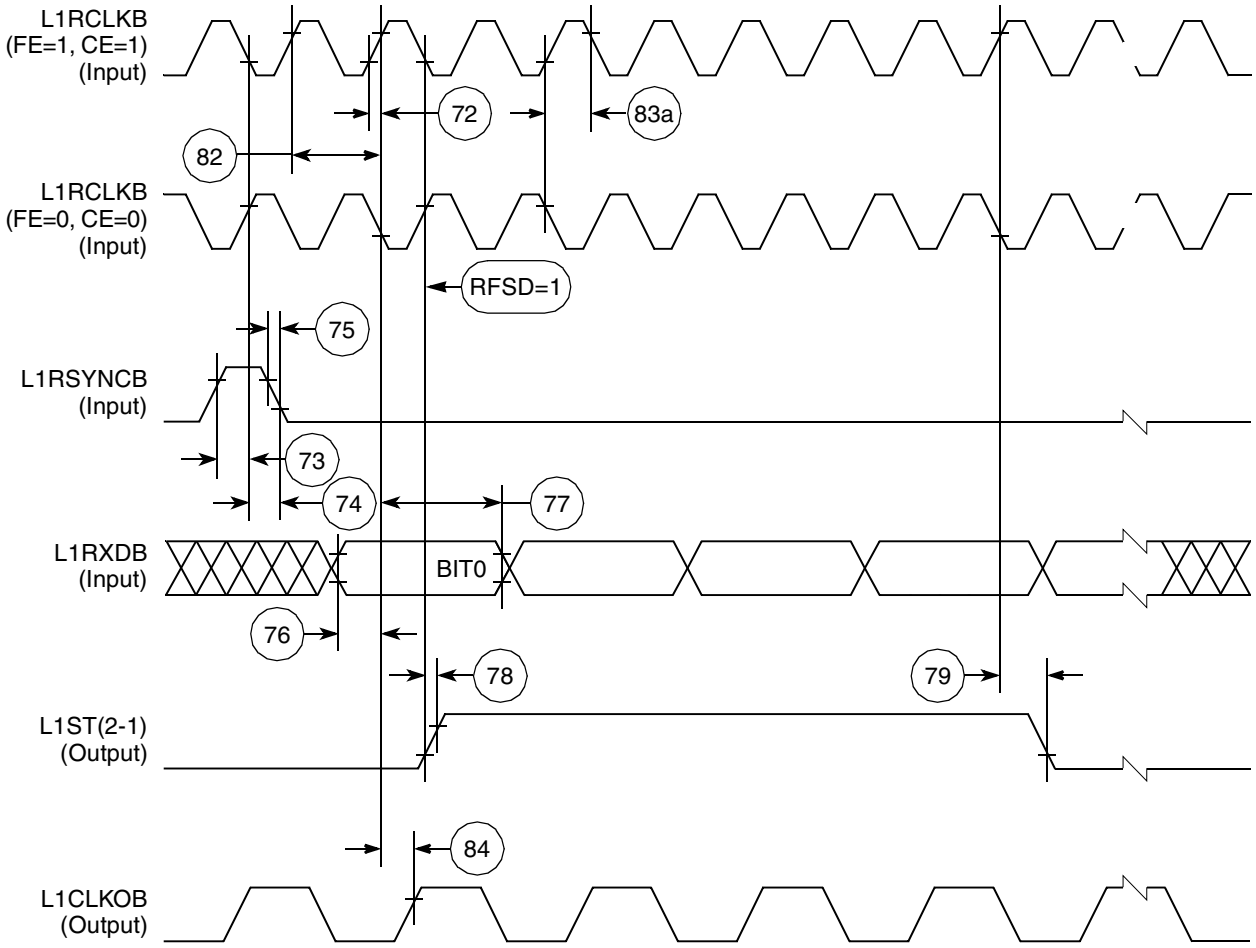

Figure 47. SI Receive Timing with Double-Speed Clocking (DSC = 1)

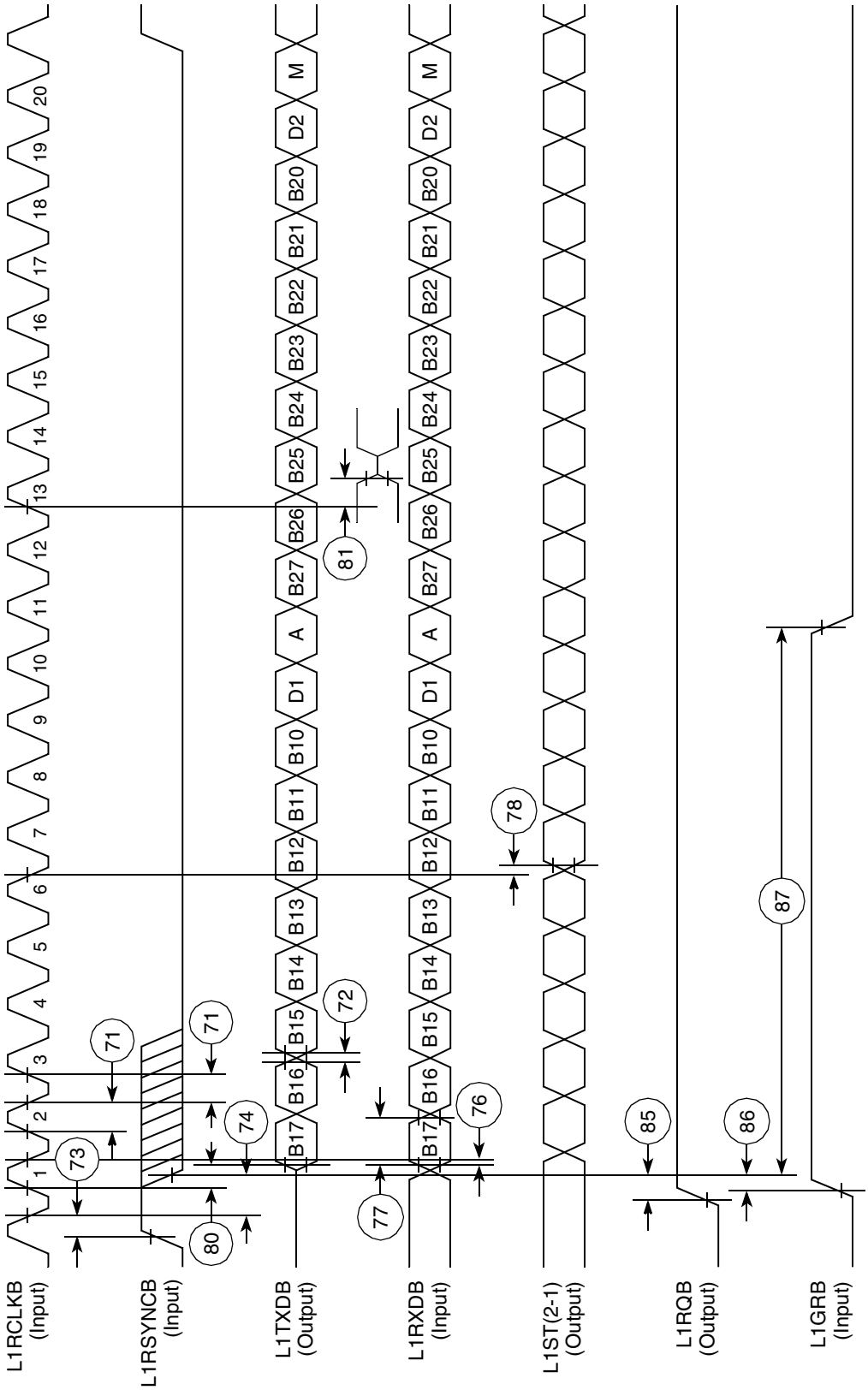

Figure 50. IDL Timing

13.6 SCC in NMSI Mode Electrical Specifications

Table 21 provides the NMSI external clock timing.

Table 21. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK3 and TCLK3 width high [1]	1/SYNCCLK	—	ns
101	RCLK3 and TCLK3 width low	1/SYNCCLK +5	—	ns
102	RCLK3 and TCLK3 rise/fall time	—	15.00	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS3}}$ active/inactive delay (from TCLK3 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS3}}$ setup time to TCLK3 rising edge	5.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	5.00	—	ns
107	RXD3 hold time from RCLK3 rising edge [2]	5.00	—	ns
108	$\overline{\text{CD3}}$ setup Time to RCLK3 rising edge	5.00	—	ns

1 The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater than or equal to 2.25/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Table 22 provides the NMSI internal clock timing.

Table 22. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK3 and TCLK3 frequency [1]	0.00	SYNCCLK/3	MHz
102	RCLK3 and TCLK3 rise/fall time	—	—	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS3}}$ active/inactive delay (from TCLK3 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS3}}$ setup time to TCLK3 rising edge	40.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	40.00	—	ns
107	RXD3 hold time from RCLK3 rising edge [2]	0.00	—	ns
108	$\overline{\text{CD3}}$ setup time to RCLK3 rising edge	40.00	—	ns

1 The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater than or equal to 3/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Table 23. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLK3 rising edge)	10	50	ns
135	$\overline{\text{RSTRT}}$ active delay (from TCLK3 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK3 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted [2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated [2]	—	20	ns

1 The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater than or equal to 2/1.

2 $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

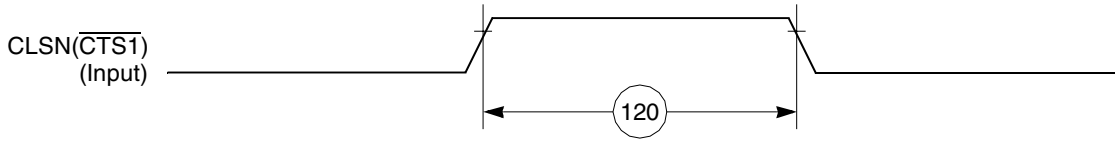

Figure 54. Ethernet Collision Timing Diagram

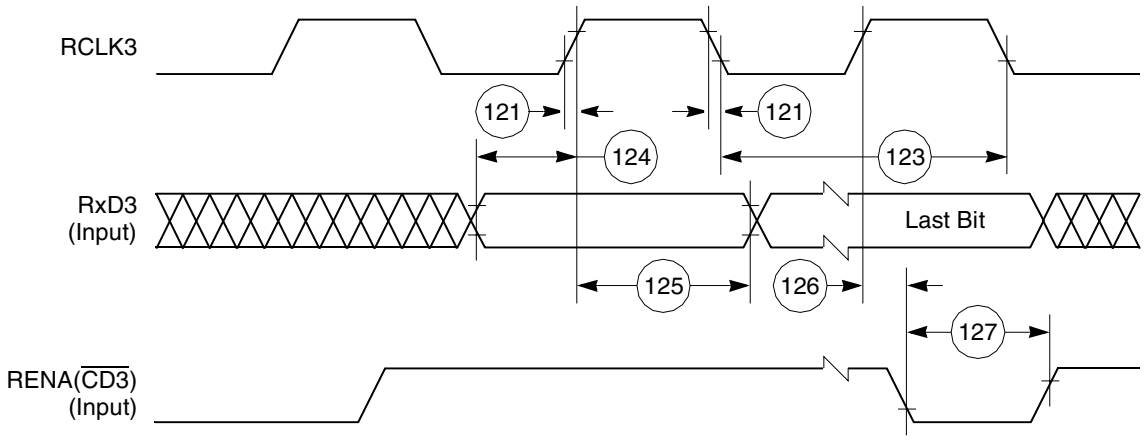

Figure 55. Ethernet Receive Timing Diagram

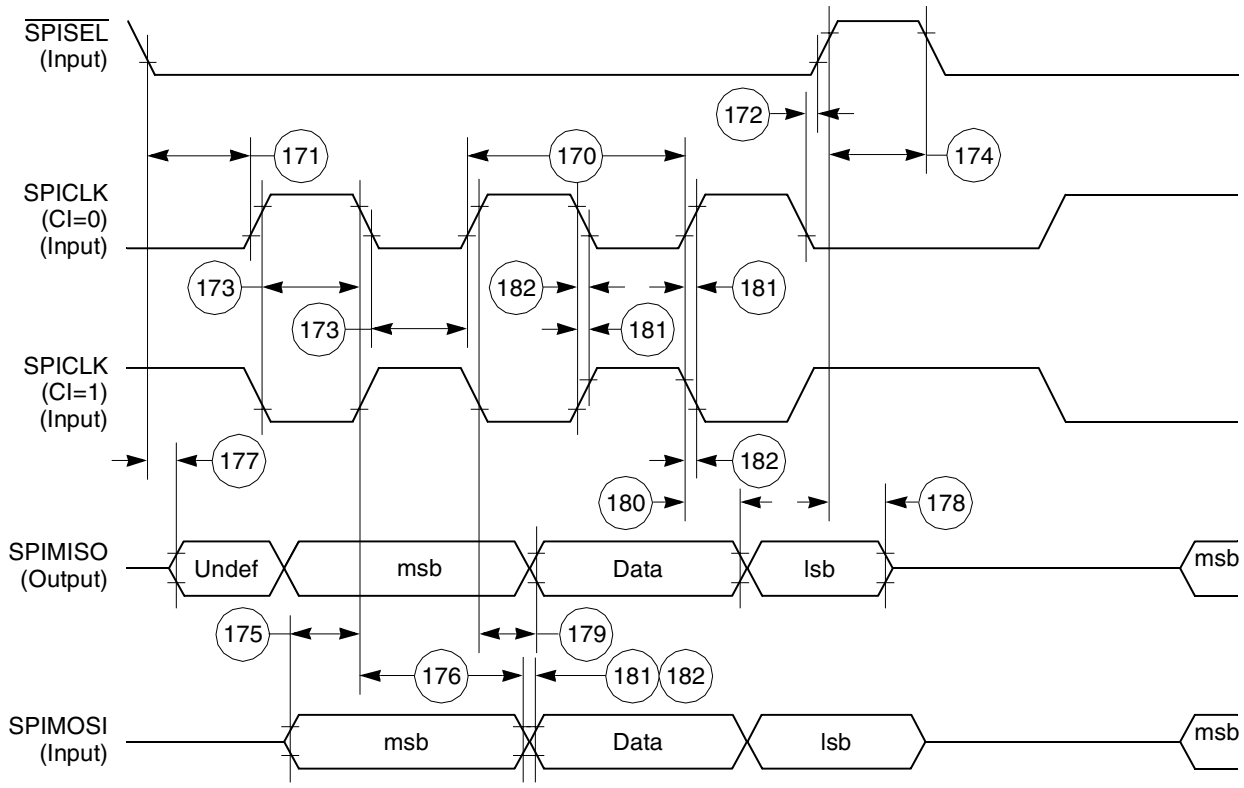

Figure 62. SPI Slave (CP = 1) Timing Diagram

14 FEC Electrical Characteristics

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

14.1 MII Receive Signal Timing (MII_RXD[3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency – 1%.

Table 26 provides information on the MII receive signal timing.

Table 26. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period

Table 31. Pin Assignments - JEDEC Standard (continued)

Name	Pin Number	Type
PC12 $\overline{\text{RTS4}}$ L1ST4	E15	Bidirectional (5V tolerant)
PC7 L1TSYNCB $\overline{\text{CTS3}}$	J14	Bidirectional (5V tolerant)
PC6 L1RSYNCB $\overline{\text{CD3}}$	K15	Bidirectional (5V tolerant)
PC5 $\overline{\text{CTS4}}$ SDACK1	J13	Bidirectional (5V tolerant)
PC4 $\overline{\text{CD4}}$	L14	Bidirectional (5V tolerant)
PD15 MII-RXD3	M14	Bidirectional (5V tolerant)
PD14 MII-RXD2	N16	Bidirectional (5V tolerant)
PD13 MII-RXD1	K13	Bidirectional (5V tolerant)
PD12 MII-MDC	N15	Bidirectional (5V tolerant)
PD11 RXD3 MII-TXERR	P16	Bidirectional (5V tolerant)
PD10 TXD3 MII-RXD0	R15	Bidirectional (5V tolerant)
PD9 RXD4 MII-TXD0	N14	Bidirectional (5V tolerant)
PD8 TXD4 MII_RX_CLK	M13	Bidirectional (5V tolerant)
PD7 $\overline{\text{RTS3}}$ MII_RX_ER	T15	Bidirectional (5V tolerant)
PD6 $\overline{\text{RTS4}}$ MII_RX_DV	N13	Bidirectional (5V tolerant)

NOTE: This is the top view of the device.

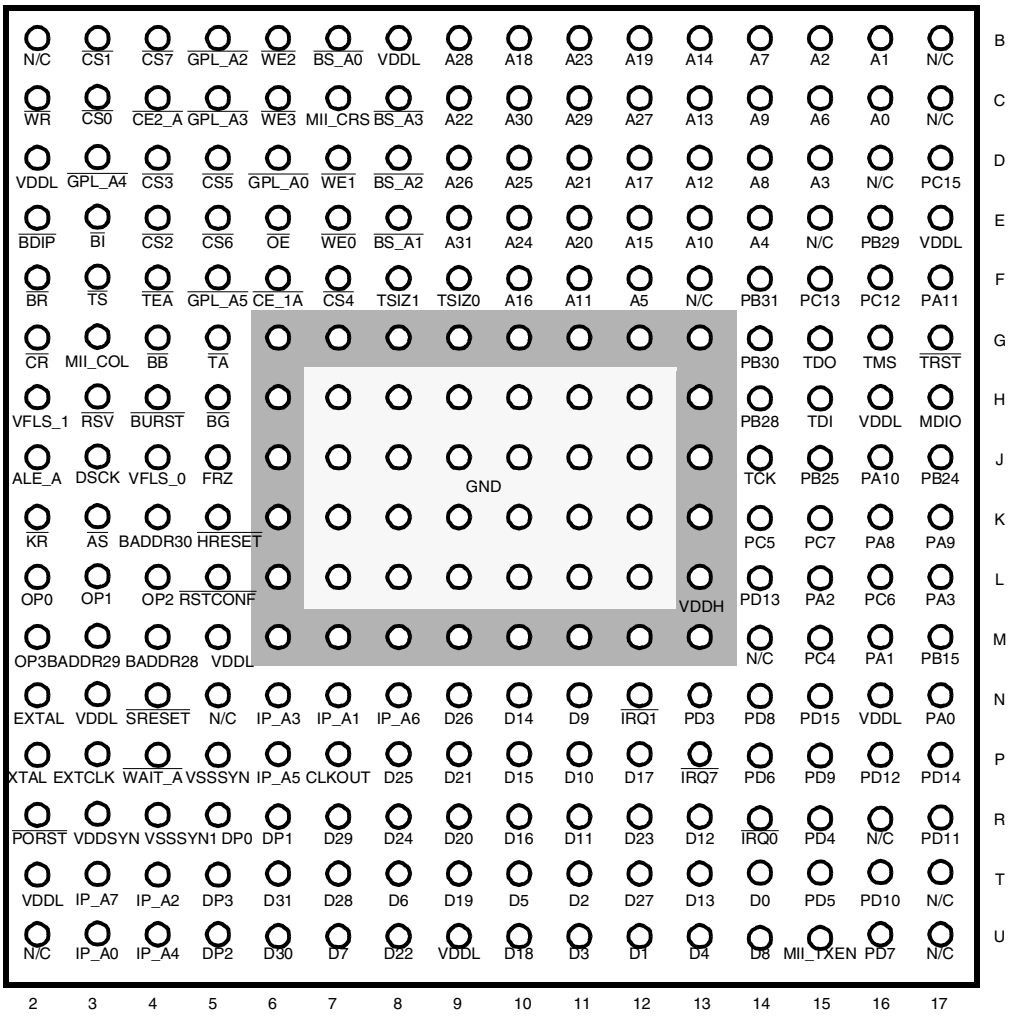

Figure 68. Pinout of the PBGA Package—non-JEDEC

Table 32 contains a list of the MPC853T input and output signals and shows multiplexing and pin assignments.

Table 32. Pin Assignments—Non-JEDEC

Name	Pin Number	Type
A[0:31]	C16, B16, B15, D15, E14, F12, C15, B14, D14, C14, E13, F11, D13, C13, B13, E12, F10, D12, B10, B12, E11, D11, C9, B11, E10, D10, D9, C12, B9, C11, C10, E9	Bidirectional Three-state (3.3 V only)
TSIZ0 REG	F9	Bidirectional Three-state (3.3 V only)
TSIZ1	F8	Bidirectional Three-state (3.3 V only)
RD/WR	C2	Bidirectional Three-state (3.3 V only)