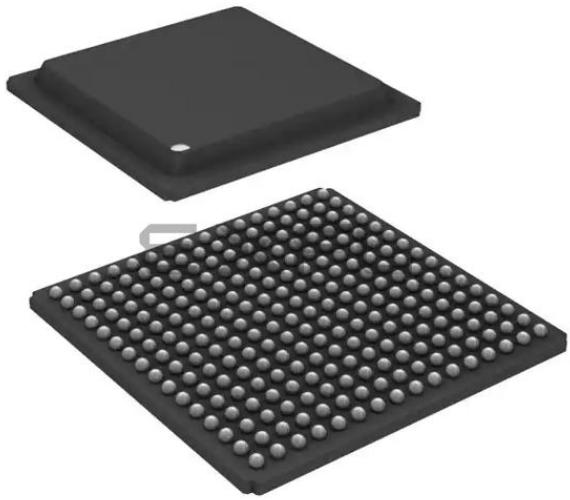


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	100MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc853tvr100a

4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC853T.

Table 3. MPC853T Thermal Resistance Data

Rating	Environment		Symbol	Value	Unit
Junction-to-ambient [1]	Natural convection	Single-layer board (1s)	$R_{\theta JA}$ [2]	49	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}$ [3]	32	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$ [3]	41	
		Four-layer board (2s2p)	$R_{\theta JMA}$ [3]	29	
Junction-to-board [4]			$R_{\theta JB}$	24	
Junction-to-case [5]			$R_{\theta JC}$	13	
Junction-to-package top [6]	Natural convection		Ψ_{JT}	3	
	Airflow (200 ft/min)		Ψ_{JT}	2	

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5 Power Dissipation

Table 4 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1 mode, where CPU frequency is twice bus speed.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages, and especially PBGA packages, is strongly dependent on the board temperature. If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)
T_B = board temperature ºC
P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

Table 8. Frequency Ranges for Standard Part Frequencies (2:1 Bus Mode)

Part Frequency	50 MHz		66 MHz		80 MHz		100 MHz	
	Min	Max	Min	Max	Min	Max	Min	Max
Core Frequency	40	50	40	66.67	40	80	40	100
Bus Frequency 2:1	20	25	20	33.33	20	40	20	50

Table 9 provides the bus operation timing for the MPC853T at 33, 40, 50, and 66 MHz.

The timing for the MPC853T bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. CLKOUT assumes a 100-pF load maximum delay.

Table 9. Bus Operation Timings

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	Bus period (CLKOUT), see Table 7	—	—	—	—	—	—	—	—	ns
B1a	EXTCLK to CLKOUT phase skew - If CLKOUT is an integer multiple of EXTCLK, then the rising edge of EXTCLK is aligned with the rising edge of CLKOUT. For a non-integer multiple of EXTCLK, this synchronization is lost, and the rising edges of EXTCLK and CLKOUT have a continuously varying phase skew.	–2	+2	–2	+2	–2	+2	–2	+2	ns
B1b	CLKOUT frequency jitter peak-to-peak	—	1	—	1	—	1	—	1	ns
B1c	Frequency jitter on EXTCLK [1]	—	0.50	—	0.50	—	0.50	—	0.50	%
B1d	CLKOUT phase jitter peak-to-peak for OSCLK ≥ 15 MHz	—	4	—	4	—	4	—	4	ns
	CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz	—	5	—	5	—	5	—	5	ns
B2	CLKOUT pulse width low (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns
B3	CLKOUT pulse width high (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns
B4	CLKOUT rise time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B5	CLKOUT fall time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B7a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B7b	CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), $\overline{STS}$ output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30) RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) valid (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B8a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR valid (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B8b	CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{STS}$ valid [3] (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B9	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3), TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, PTR High-Z (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B11	CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion (MAX = 0.25 × B1 + 6.0)	7.60	13.60	6.30	12.30	5.00	11.00	3.80	9.80	ns
B11a	CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.30 [2])	2.50	9.30	2.50	9.30	2.50	9.30	2.50	9.80	ns
B12	CLKOUT to $\overline{TS}$, $\overline{BB}$ negation (MAX = 0.25 × B1 + 4.8)	7.60	12.30	6.30	11.00	5.00	9.80	3.80	8.50	ns
B12a	CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B13	CLKOUT to $\overline{TS}$, $\overline{BB}$ High-Z (MIN = 0.25 × B1)	7.60	21.60	6.30	20.30	5.00	19.00	3.80	14.00	ns
B13a	CLKOUT to $\overline{TA}$, $\overline{BI}$ High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 × B1 + 2.5)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to $\overline{TEA}$ assertion (MAX = 0.00 × B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B15	CLKOUT to $\overline{TEA}$ High-Z (MIN = 0.00 × B1 + 2.50)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	$\overline{TA}$, $\overline{BI}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B16a	$\overline{TEA}$, $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 4.5)	4.50	—	4.50	—	4.50	—	4.50	—	ns
B16b	$\overline{BB}$, $\overline{BG}$, $\overline{BR}$, valid to CLKOUT (setup time) [3] (4MIN = 0.00 × B1 + 0.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B29c	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B29d	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B29e	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B29f	$\overline{WE}$(0:3/BS_B[0:3]) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 × B1 – 6.30)	5.00	—	3.00	—	1.10	—	0.00	—	ns
B29g	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 – 6.30)	5.00	—	3.00	—	1.10	—	0.00	—	ns
B29h	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = 0.375 × B1 – 3.30)	38.40	—	31.10	—	24.20	—	17.50	—	ns
B29i	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 – 3.30)	38.40	—	31.10	—	24.20	—	17.50	—	ns
B30	$\overline{CS}$, $\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access [8] (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B30a	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 0, CSNT =1 ACS = 10, or ACS == 11, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B30b	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31) Invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS == 11 EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns

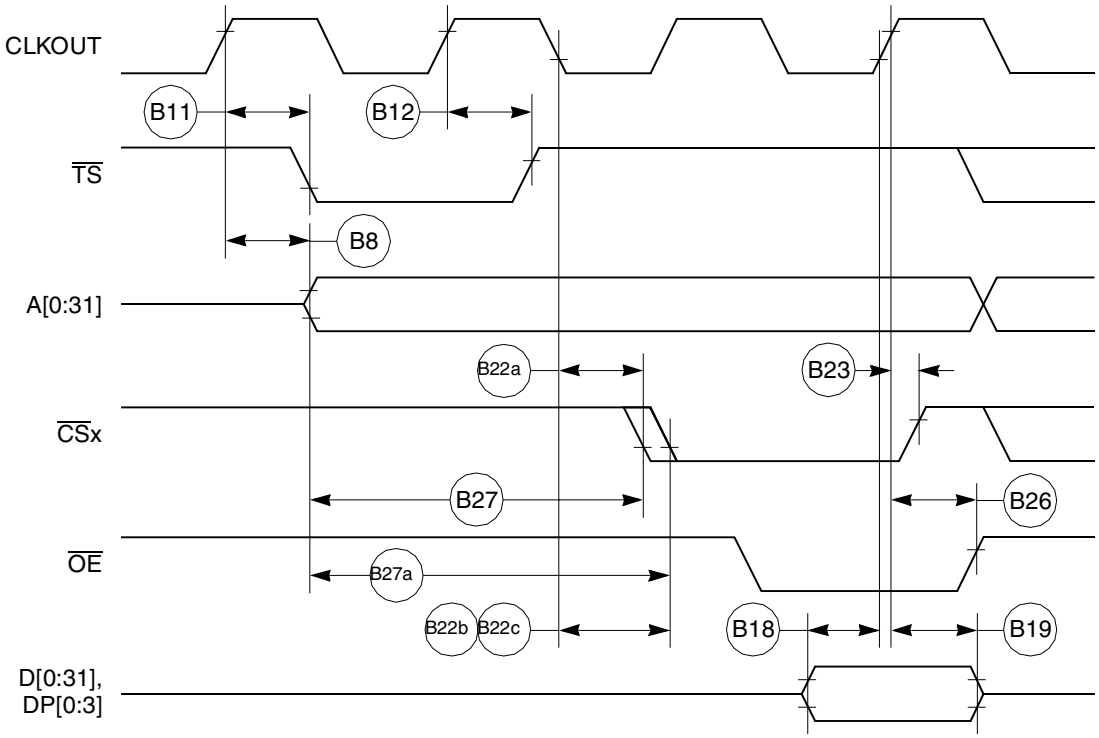


Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10, ACS = 11)

Figure 14 through Figure 16 provide the timing for the external bus write controlled by various GPCM factors.

Table 12 shows the PCMCIA port timing for the MPC853T.

Table 12. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
J95	CLKOUT to OPx valid (MAX = 0.00 × B1 + 19.00)	—	19.00	—	19.00	—	19.00	—	19.00	ns
J96	$\overline{\text{HRESET}}$ negated to OPx drive [1] (MIN = 0.75 × B1 + 3.00)	25.70	—	21.70	—	18.00	—	14.40	—	ns
J97	IP_Xx valid to CLKOUT rising edge (MIN = 0.00 × B1 + 5.00)	5.00	—	5.00	—	5.00	—	5.00	—	ns
J98	CLKOUT rising edge to IP_Xx invalid (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns

1 OP2 and OP3 only.

Figure 28 provides the PCMCIA output port timing for the MPC853T.

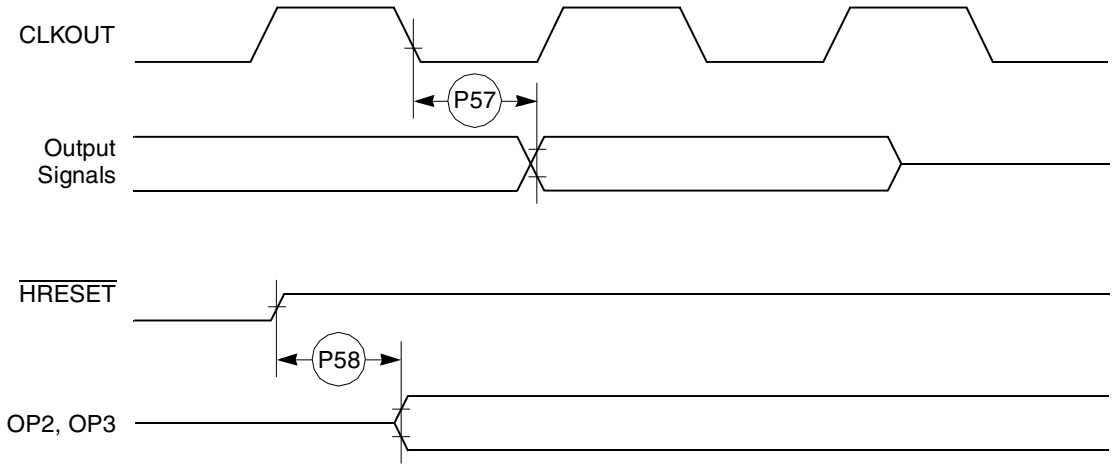


Figure 28. PCMCIA Output Port Timing

Figure 29 provides the PCMCIA in put port timing for the MPC853T.

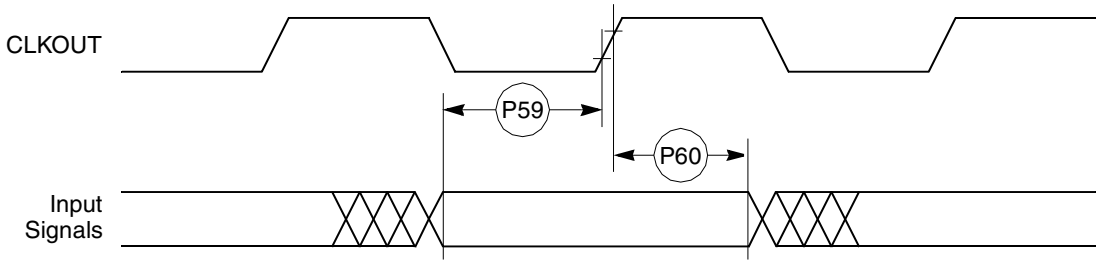


Figure 29. PCMCIA Input Port Timing

Figure 34 provides the reset timing for the debug port configuration.

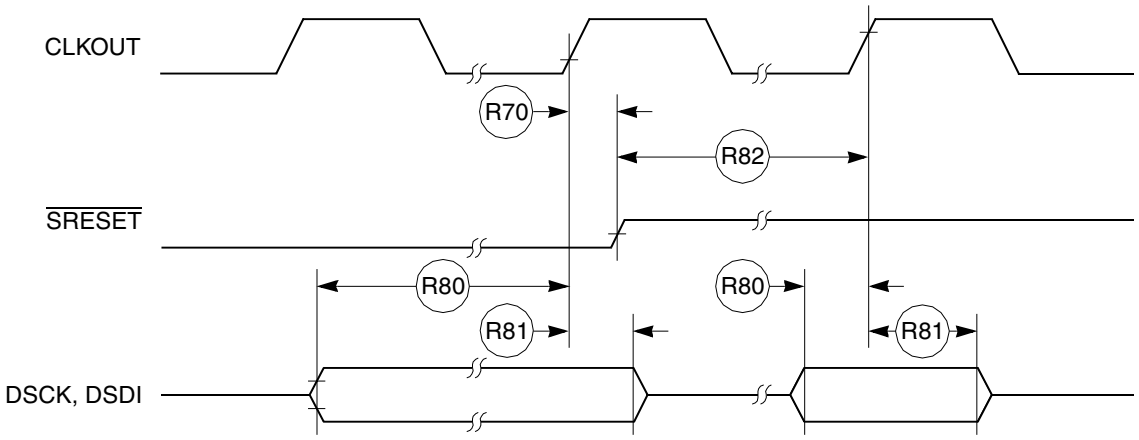


Figure 34. Reset Timing—Debug Port Configuration

12 IEEE 1149.1 Electrical Specifications

Table 15 provides the JTAG timings for the MPC853T shown in Figure 35 to Figure 38.

Table 15. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

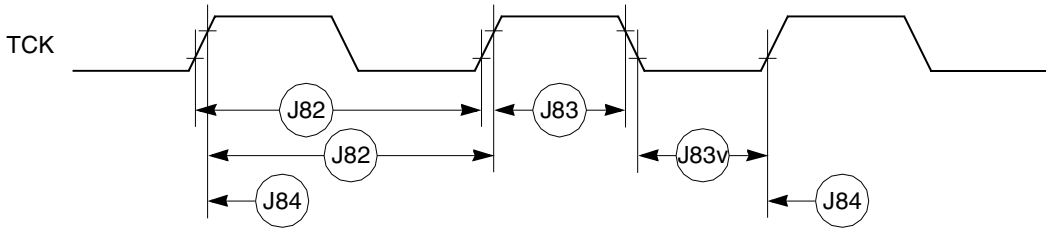


Figure 35. JTAG Test Clock Input Timing

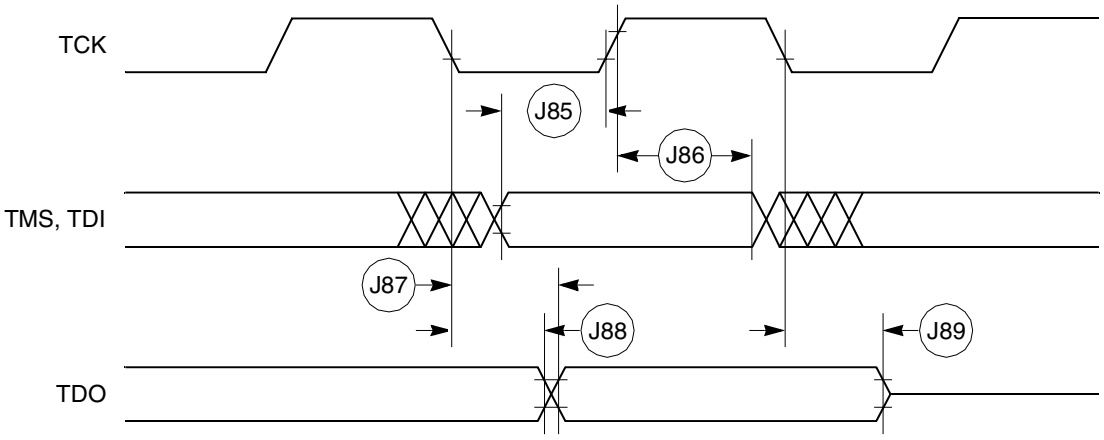


Figure 36. JTAG Test Access Port Timing Diagram

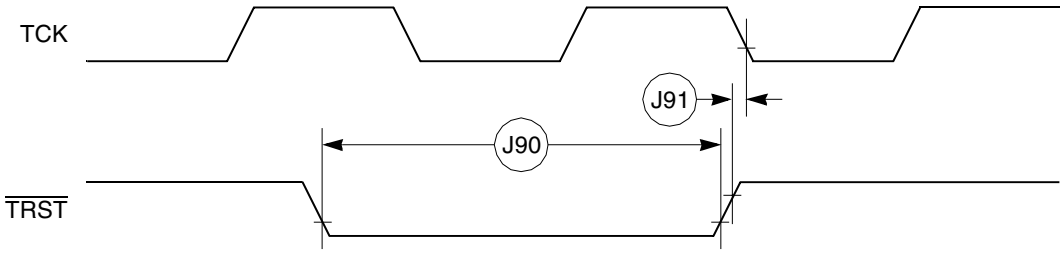


Figure 37. JTAG $\overline{\text{TRST}}$ Timing Diagram

13.4 Timer AC Electrical Specifications

Table 19 provides the general-purpose timer timings as shown in Figure 45.

Table 19. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/$\overline{\text{TGATE}}$ rise and fall time	10	—	ns
62	TIN/$\overline{\text{TGATE}}$ low time	1	—	CLK
63	TIN/$\overline{\text{TGATE}}$ high time	2	—	CLK
64	TIN/$\overline{\text{TGATE}}$ cycle time	3	—	CLK
65	CLKO low to $\overline{\text{TOUT}}$ valid	3	25	ns

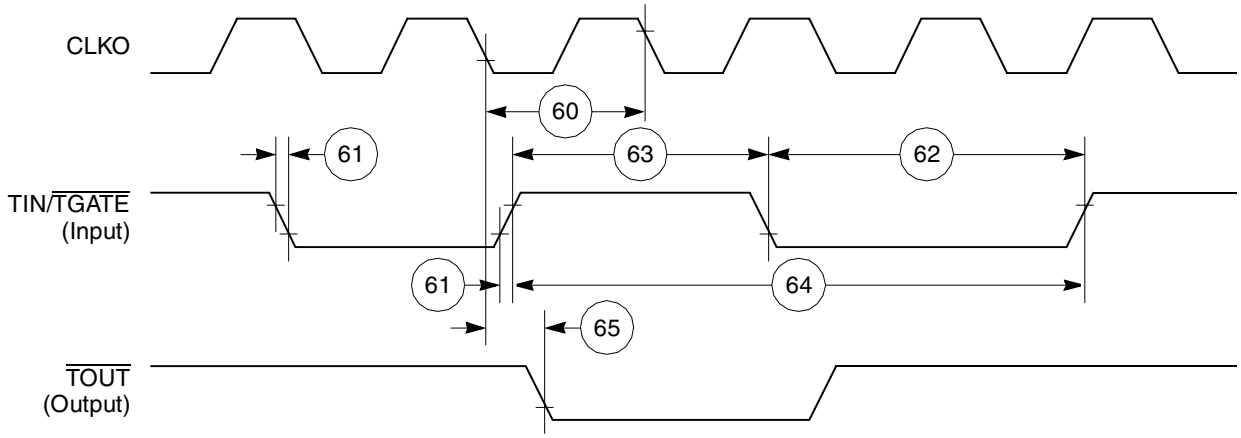


Figure 45. CPM General-Purpose Timers Timing Diagram

13.5 Serial Interface AC Electrical Specifications

Table 20 provides the serial interface (SI) timings as shown in Figure 46 to Figure 50.

Table 20. SI Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
70	L1RCLKB, L1TCLKB frequency (DSC = 0) [1, 2]	—	SYNCCLK/2 .5	MHz
71	L1RCLKB, L1TCLKB width low (DSC = 0) [2]	P + 10	—	ns
71a	L1RCLKB, L1TCLKB width high (DSC = 0) [3]	P + 10	—	ns
72	L1TXDB, L1ST1 and L1ST2, $\overline{\text{L1RQ}}$, L1CLKO rise/fall time	—	15.00	ns
73	L1RSYNCB, L1TSYNCB valid to L1CLKB edge (SYNC setup time)	20.00	—	ns
74	L1CLKB edge to L1RSYNCB, L1TSYNCB, invalid (SYNC hold time)	35.00	—	ns

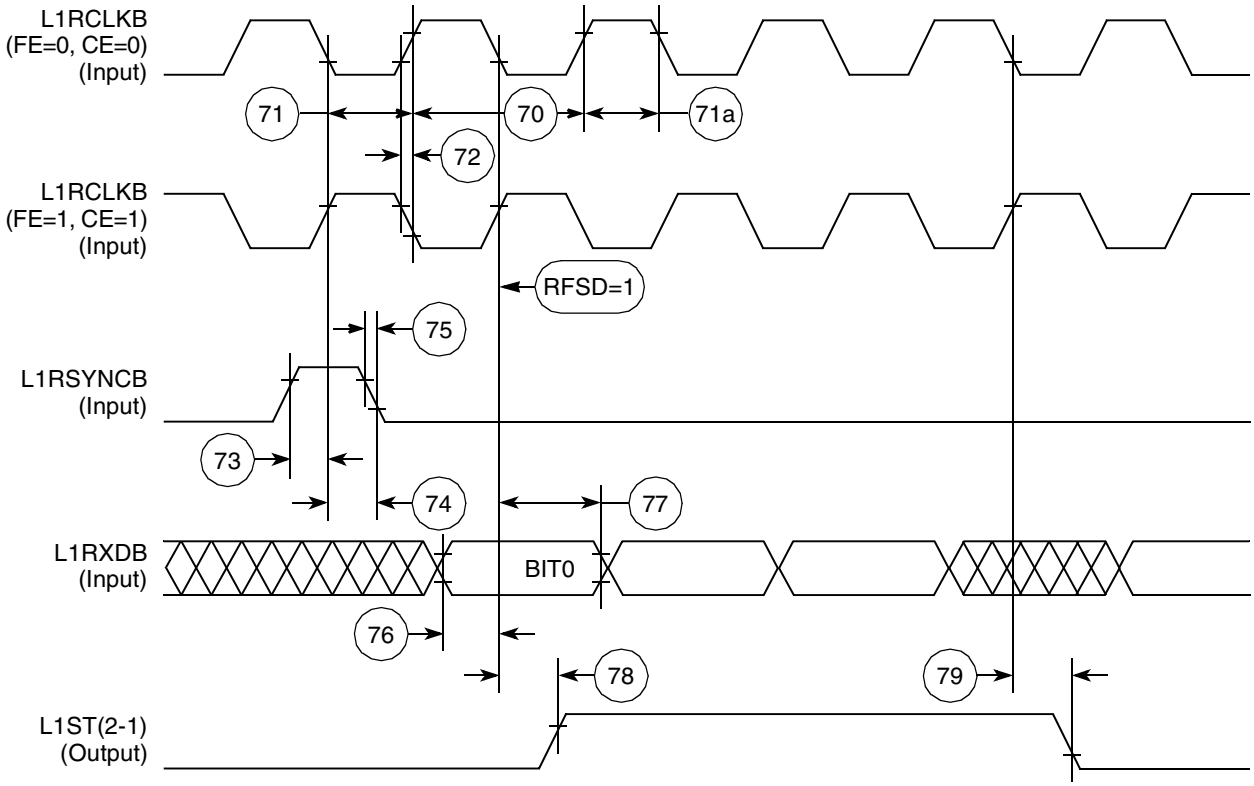


Figure 46. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

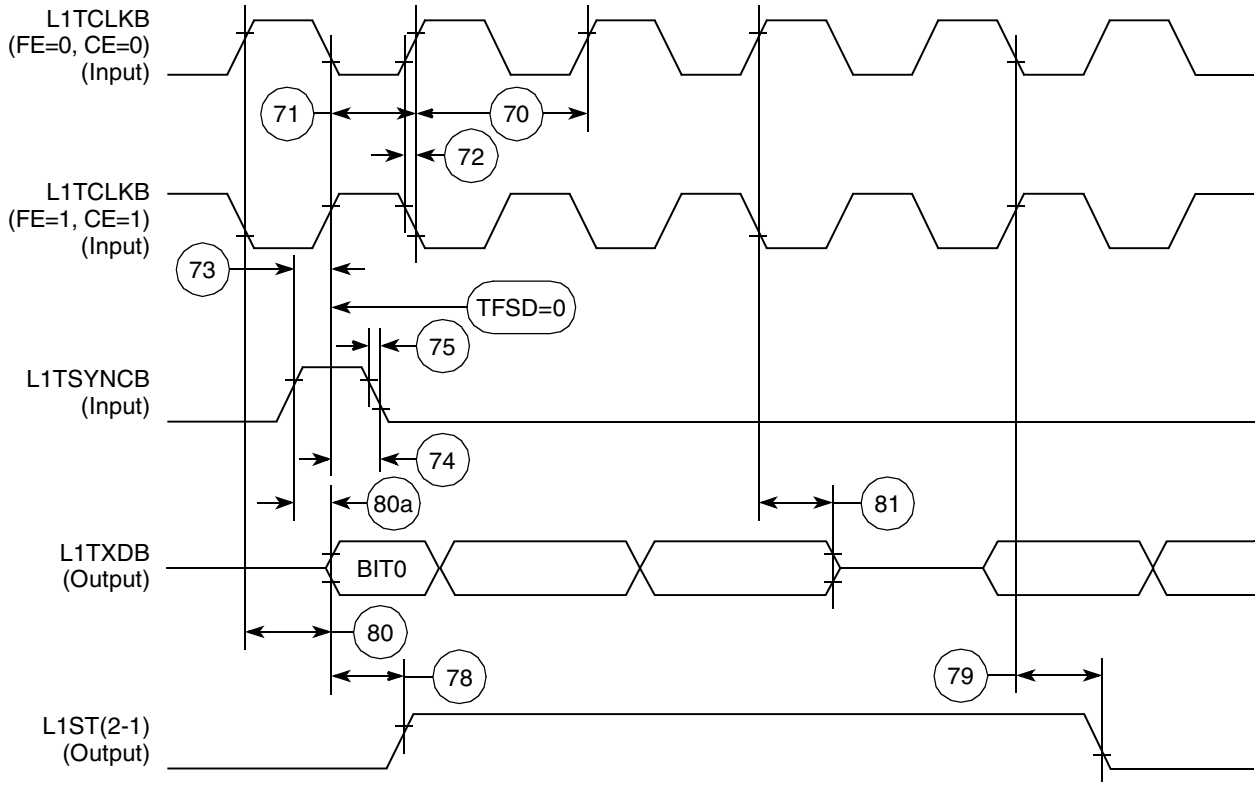


Figure 48. SI Transmit Timing Diagram (DSC = 0)

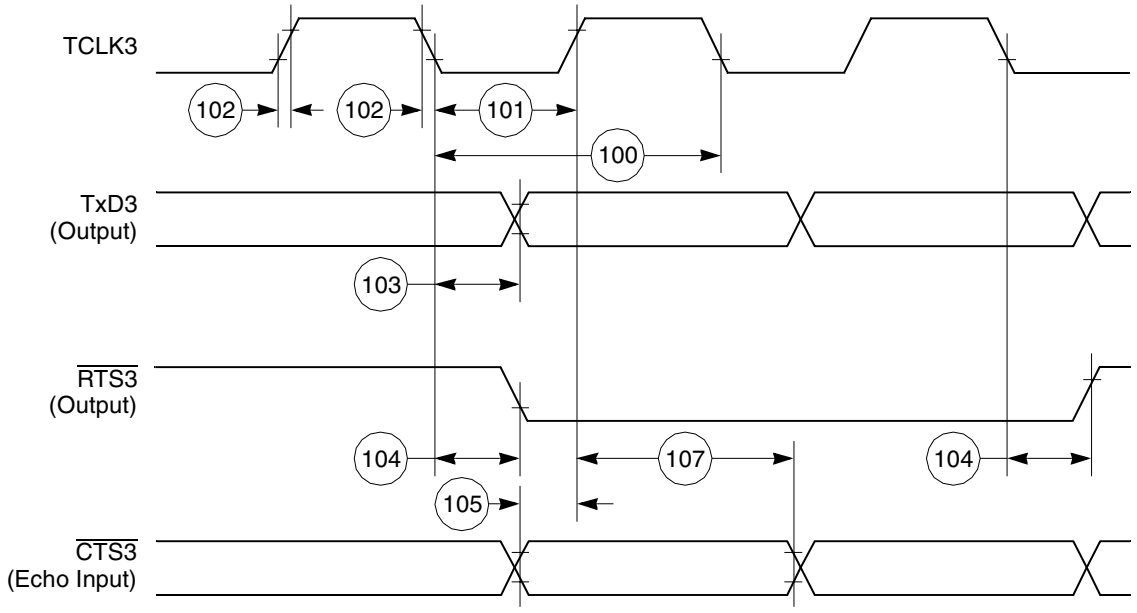


Figure 53. HDLC Bus Timing Diagram

13.7 Ethernet Electrical Specifications

Table 23 provides the Ethernet timings as shown in Figure 54 to Figure 58.

Table 23. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK3 rise/fall time	—	15	ns
122	RCLK3 width low	40	—	ns
123	RCLK3 clock period [1]	80	120	ns
124	RXD3 setup time	20	—	ns
125	RXD3 hold time	5	—	ns
126	RENA active delay (from RCLK3 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK3 rise/fall time	—	15	ns
129	TCLK3 width low	40	—	ns
130	TCLK3 clock period[1]	99	101	ns
131	TXD3 active delay (from TCLK3 rising edge)	—	50	ns
132	TXD3 inactive delay (from TCLK3 rising edge)	6.5	50	ns
133	TENA active delay (from TCLK3 rising edge)	10	50	ns

Table 23. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLK3 rising edge)	10	50	ns
135	$\overline{\text{RSTRT}}$ active delay (from TCLK3 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK3 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted [2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated [2]	—	20	ns

1 The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater than or equal to 2/1.

2 $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

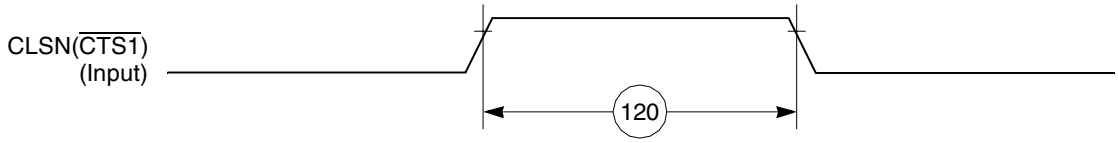


Figure 54. Ethernet Collision Timing Diagram

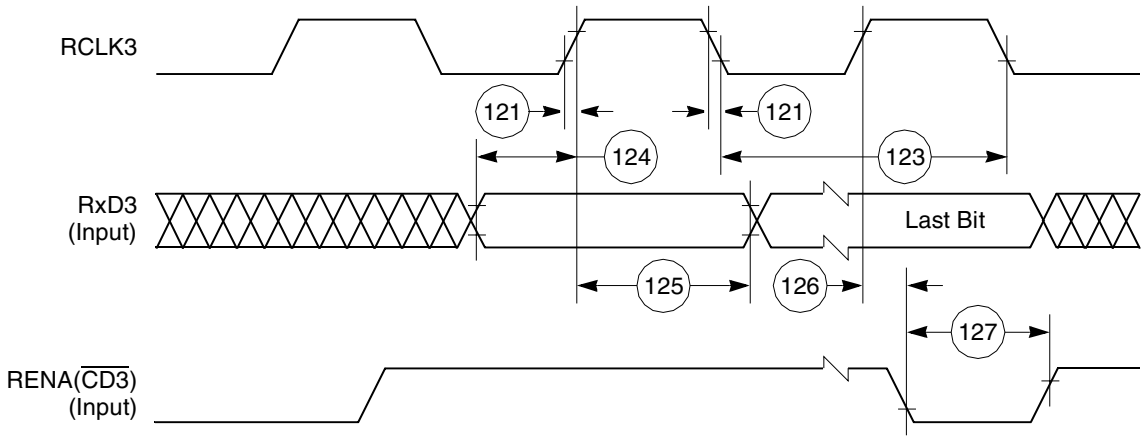


Figure 55. Ethernet Receive Timing Diagram

Figure 64 shows the MII transmit signal timing diagram.

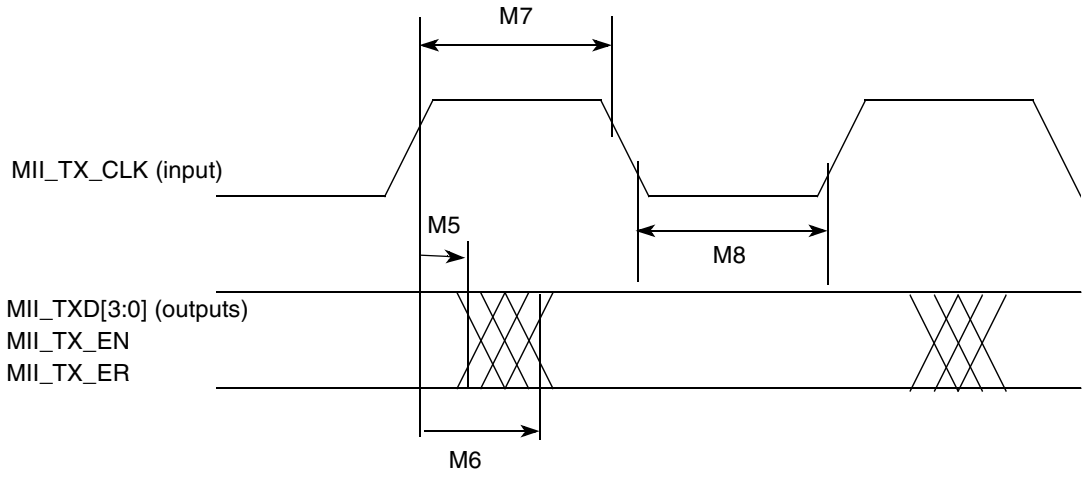


Figure 64. MII Transmit Signal Timing Diagram

14.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 28 provides information on the MII async inputs signal timing.

Table 28. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 65 shows the MII asynchronous inputs signal timing diagram.

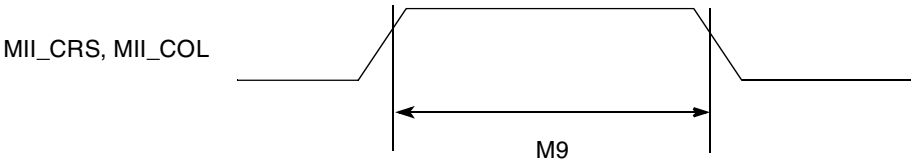


Figure 65. MII Async Inputs Timing Diagram

14.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 29 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Table 29. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns

NOTE: This is the top view of the device.

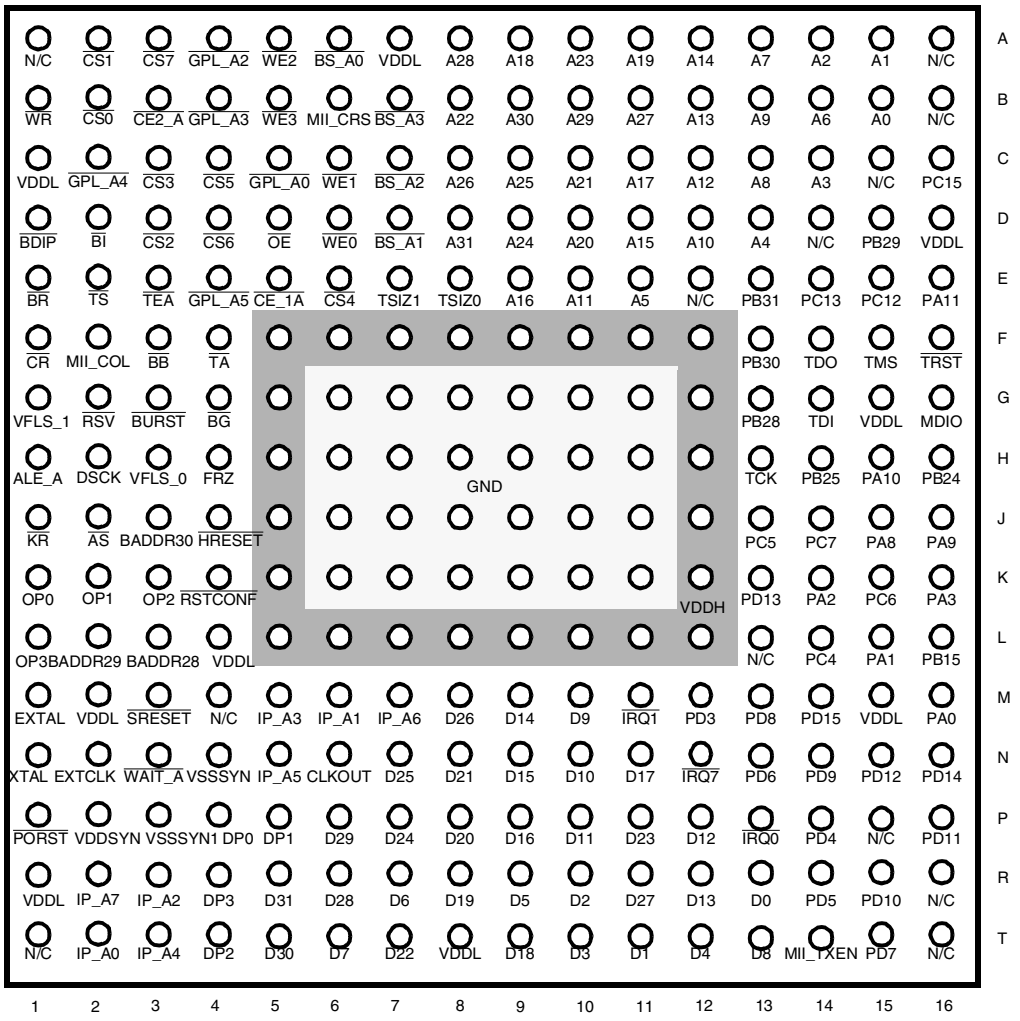


Figure 67. Pinout of the PBGA Package - JEDEC Standard

Table 31 contains a list of the MPC853T input and output signals and shows multiplexing and pin assignments.

Table 31. Pin Assignments - JEDEC Standard

Name	Pin Number	Type
A[0:31]	B15, A15, A14, C14, D13, E11, B14, A13, C13, B13, D12, E10, C12, B12, A12, D11, E9, C11, A9, A11, D10, C10, B8, A10, D9, C9, C8, B11, A8, B10, B9, D8	Bidirectional Three-state (3.3V only)
TSIZ0 REG	E8	Bidirectional Three-state (3.3V only)
TSIZ1	E7	Bidirectional Three-state (3.3V only)
RD/WR	B1	Bidirectional Three-state (3.3V only)

Table 31. Pin Assignments - JEDEC Standard (continued)

Name	Pin Number	Type
PD5 MII-TXD3	R14	Bidirectional (5V tolerant)
PD4 MII-TXD2	P14	Bidirectional (5V tolerant)
PD3 MII-TXD1	M12	Bidirectional (5V tolerant)
TMS	F15	Input (5V tolerant)
TDI DSDI	G14	Input (5V tolerant)
TCK DSCK	H13	Input (5V tolerant)
$\overline{\text{TRST}}$	F16	Input (5V tolerant)
TDO DSDO	F14	Output (5V tolerant)
MII_CRS	B6	Input
MII_MDIO	G16	Bidirectional (5V tolerant)
MII_TXEN	T14	Output (5V tolerant)
MII_COL	F2	Input
V_{SSSYN}	N4	PLL analog GND
V_{SSSYN1}	P3	PLL analog GND
V_{DDSYN}	P2	PLL analog V_{DD}
GND	G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11	Power
VDDL	A7, C1, D16, G15, L4, M2, R1, M15, T8	Power
VDDH	F5, F6, F7, F8, F9, F10, F11, F12, G5, G12, H5, H12, J5, J12, K5, K12, L5, L6, L7, L8, L9, L10, L11, L12	Power
N/C	A1, A16, B16, C15, D14, E12, L13, M4, P15, R16, T1, T16	No-connect

15.1.2 The Non-JEDEC Pinout

Figure 68 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *MPC866 PowerQUICC Family User's Manual*.

Table 32. Pin Assignments—Non-JEDEC (continued)

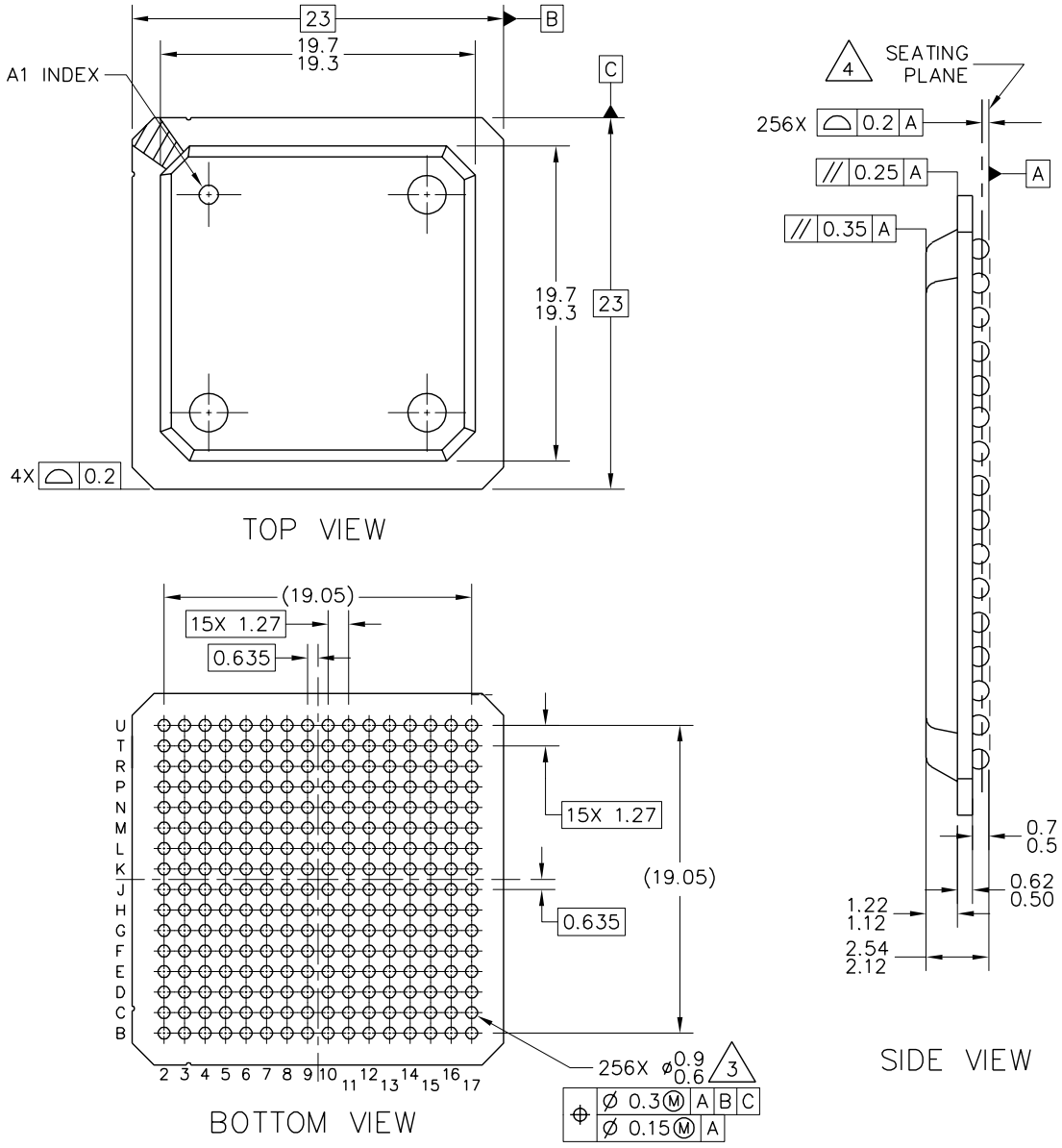
Name	Pin Number	Type
IRQ0	R14	Input (3.3 V only)
IRQ1	N12	Input (3.3 V only)
IRQ7 M_TX_CLK	P13	Input (3.3 V only)
CS[0:5]	C3, B3, E4, D4, F7, D5	Output
CS6	E5	Output
CS7	B4	Output
WE0 BS_B0 IORD	E7	Output
WE1 BS_B1 IOWR	D7	Output
WE2 BS_B2 PCOE	B6	Output
WE3 BS_B3 PCWE	C6	Output
BS_A[0:3]	B7, E8, D8, C8	Output
GPL_A0 GPL_B0	D6	Output
OE GPL_A1 GPL_B1	E6	Output
GPL_A[2:3] GPL_B[2:3] CS[2–3]	B5, C5	Output
UPWAITA GPL_A4	D3	Bidirectional (3.3 V only)
GPL_A5	F5	Output
PORESET	R2	Input (3.3 V only)
RSTCONF	L5	Input (3.3 V only)
HRESET	K5	Open drain
SRESET	N4	Open drain
XTAL	P2	Analog output
EXTAL	N2	Analog Input (3.3 V only)

Table 32. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
CLKOUT	P7	Output
EXTCLK	P3	Input (3.3 V only)
ALE_A	J2	Output
$\overline{\text{CE1\_A}}$	F6	Output
$\overline{\text{CE2\_A}}$	C4	Output
$\overline{\text{WAIT\_A}}$	P4	Input (3.3 V only)
IP_A0	U3	Input (3.3 V only)
IP_A1	N7	Input (3.3 V only)
IP_A2 $\overline{\text{IOIS16\_A}}$	T4	Input (3.3 V only)
IP_A3	N6	Input (3.3 V only)
IP_A4	U4	Input (3.3 V only)
IP_A5	P6	Input (3.3 V only)
IP_A6	N8	Input (3.3 V only)
IP_A7	T3	Input (3.3 V only)
DSCK	J3	Bidirectional Three-state (3.3 V only)
IWP[0:1] VFLS[0:1]	J4, H2	Bidirectional (3.3 V only)
OP0	L2	Bidirectional (3.3 V only)
OP1	L3	Output
OP2 MODCK1 $\overline{\text{STS}}$	L4	Bidirectional (3.3 V only)
OP3 MODCK2 DSDO	M2	Bidirectional (3.3 V only)
BADDR[28:29]	M4, M3	Output
BADDR30 $\overline{\text{REG}}$	K4	Output
$\overline{\text{AS}}$	K3	Input (3.3 V only)
PA11 RXD3 L1TXDB	F17	Bidirectional (Optional: open-drain) (5-V tolerant)

15.2 Mechanical Dimensions of the PBGA Package

Figure 69 shows the mechanical dimensions of the PBGA package.



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

Note: Solder sphere composition is 95.5%Sn 45%Ag 0.5%Cu for MPC853TVRXXX
Solder sphere composition is 62%Sn 36%Pb 2%Ag for MPC853TZTXXX

Figure 69. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package