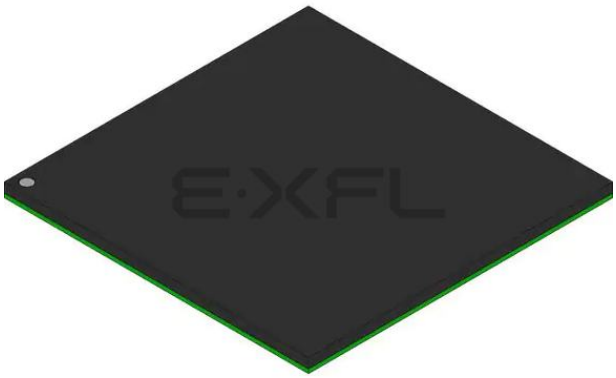

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc853tvr66a

and incorporates memory management units (MMUs), instruction and data caches. The MPC853T is a subset of this family of devices and is the main focus of this document.

2 Features

The MPC853T is comprised of three modules that each use the 32-bit internal bus: a MPC8xx core, a system integration unit (SIU), and a communications processor module (CPM). The MPC853T block diagram is shown in Figure 1.

The following list summarizes the key MPC853T features:

- Embedded MPC8xx core up to 100 MHz
- Maximum frequency operation of the external bus is 66 MHz
  - The 50-/66-MHz core frequencies support both the 1:1 and 2:1 modes.
  - The 80-/100-MHz core frequencies support 2:1 mode only.
- Single-issue, 32-bit core (compatible with the PowerPC architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch and without conditional execution.
  - 4-Kbyte data cache and 4-Kbyte instruction cache
    - Instruction cache is two-way, set-associative with 128 sets
    - Data cache is two-way, set-associative with 128 sets
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry translation look-aside buffer (TLB), fully associative instruction, and data TLBs
  - MMUs support multiple page sizes of 4 Kbytes, 16 Kbytes, 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank.
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROMs, Flash EPROMs, and other memory devices
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbytes–256 Mbytes)
  - Selectable write protection
  - On-chip bus arbitration logic
- Fast Ethernet Controller (FEC)

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used. It determines the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per the JESD51-2 specification published by JEDEC using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

8 Power Supply and Power Sequencing

This section provides design considerations for the MPC853T power supply. The MPC853T has a core voltage (V_{DDL}) and PLL voltage (V_{DDSYN}), which both operate at lower voltages than the I/O voltage V_{DDH}. The I/O section of the MPC853T is supplied with 3.3 V across V_{DDH} and V_{SS} (GND).

The signals PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15] PD[3:15], TDI, TDO, TCK, TRST, TMS, MII_TXEN, and MII_MDIO are 5-V tolerant. All inputs cannot be more than 2.5 V greater than V_{DDH}. In addition, 5-V tolerant pins can not exceed 5.5 V, and remaining input pins cannot exceed 3.465 V. This restriction applies to power up/down and normal operation.

One consequence of multiple power supplies is that when power is initially applied, the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- V_{DDL} must not exceed V_{DDH} during power up and power down.
- V_{DDL} must not exceed 1.9 V, and V_{DDH} must not exceed 3.465 V.

These cautions are necessary for the long-term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased, and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown in Figure 2 can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on power up and the 1N5820 diodes regulate the maximum potential difference on power down.

Table 6. Mandatory Reset Configuration of MPC853T (continued)

Register/Configuration	Field	Value (binary)
PCPAR (Port C pin assignment register)	PCPAR[8:11] PCDIR[14]	0
PCDIR (Port C data direction register)	PCDIR[8:11] PCDIR[14]	1

10 Layout Practices

Each V_{DD} pin on the MPC853T should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1-µF bypass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized, and additional appropriate decoupling capacitors should be used if required. Capacitor leads and associated printed circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as V_{DD} and GND planes should be used.

All output pins on the MPC853T have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads, as well as parasitic capacitances caused by the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{DD} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, please refer to Section 14.4.3, "Clock Synthesizer Power (V_{DDSYN}, V_{SSSYN}, V_{SSSYN1})" in the *MPC866 PowerQUICC Family User's Manual*.

11 Bus Signal Timing

The maximum bus speed supported by the MPC853T is 66 MHz. Table 7 shows the frequency ranges for standard part frequencies in 1:1 bus mode.

Table 7. Frequency Ranges for Standard Part Frequencies (1:1 Bus Mode)

Part Frequency	50 MHz		66 MHz	
	Min	Max	Min	Max
Core Frequency	40	50	40	66.67
Bus Frequency	40	50	40	66.67

Table 8 shows the frequency ranges for standard part frequencies in 2:1 bus mode.

Table 8. Frequency Ranges for Standard Part Frequencies (2:1 Bus Mode)

Part Frequency	50 MHz		66 MHz		80 MHz		100 MHz	
	Min	Max	Min	Max	Min	Max	Min	Max
Core Frequency	40	50	40	66.67	40	80	40	100
Bus Frequency 2:1	20	25	20	33.33	20	40	20	50

Table 9 provides the bus operation timing for the MPC853T at 33, 40, 50, and 66 MHz.

The timing for the MPC853T bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. CLKOUT assumes a 100-pF load maximum delay.

Table 9. Bus Operation Timings

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	Bus period (CLKOUT), see Table 7	—	—	—	—	—	—	—	—	ns
B1a	EXTCLK to CLKOUT phase skew - If CLKOUT is an integer multiple of EXTCLK, then the rising edge of EXTCLK is aligned with the rising edge of CLKOUT. For a non-integer multiple of EXTCLK, this synchronization is lost, and the rising edges of EXTCLK and CLKOUT have a continuously varying phase skew.	–2	+2	–2	+2	–2	+2	–2	+2	ns
B1b	CLKOUT frequency jitter peak-to-peak	—	1	—	1	—	1	—	1	ns
B1c	Frequency jitter on EXTCLK [1]	—	0.50	—	0.50	—	0.50	—	0.50	%
B1d	CLKOUT phase jitter peak-to-peak for OSCLK ≥ 15 MHz	—	4	—	4	—	4	—	4	ns
	CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz	—	5	—	5	—	5	—	5	ns
B2	CLKOUT pulse width low (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns
B3	CLKOUT pulse width high (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns
B4	CLKOUT rise time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B5	CLKOUT fall time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B7a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B32c	CLKOUT rising edge to $\overline{BS}$ valid, as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid, as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 × B1 + 6.60)	13.30	18.00	11.30	16.00	9.40	14.10	7.60	12.30	ns
B33	CLKOUT falling edge to $\overline{GPL}$ valid, as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to $\overline{GPL}$ valid, as requested by control bit GxT3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by control bit CST4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by CST2 in the corresponding word in UPM (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid, as requested by control bit BST4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid, as requested by BST1 in the corresponding word in the UPM (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid, as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns

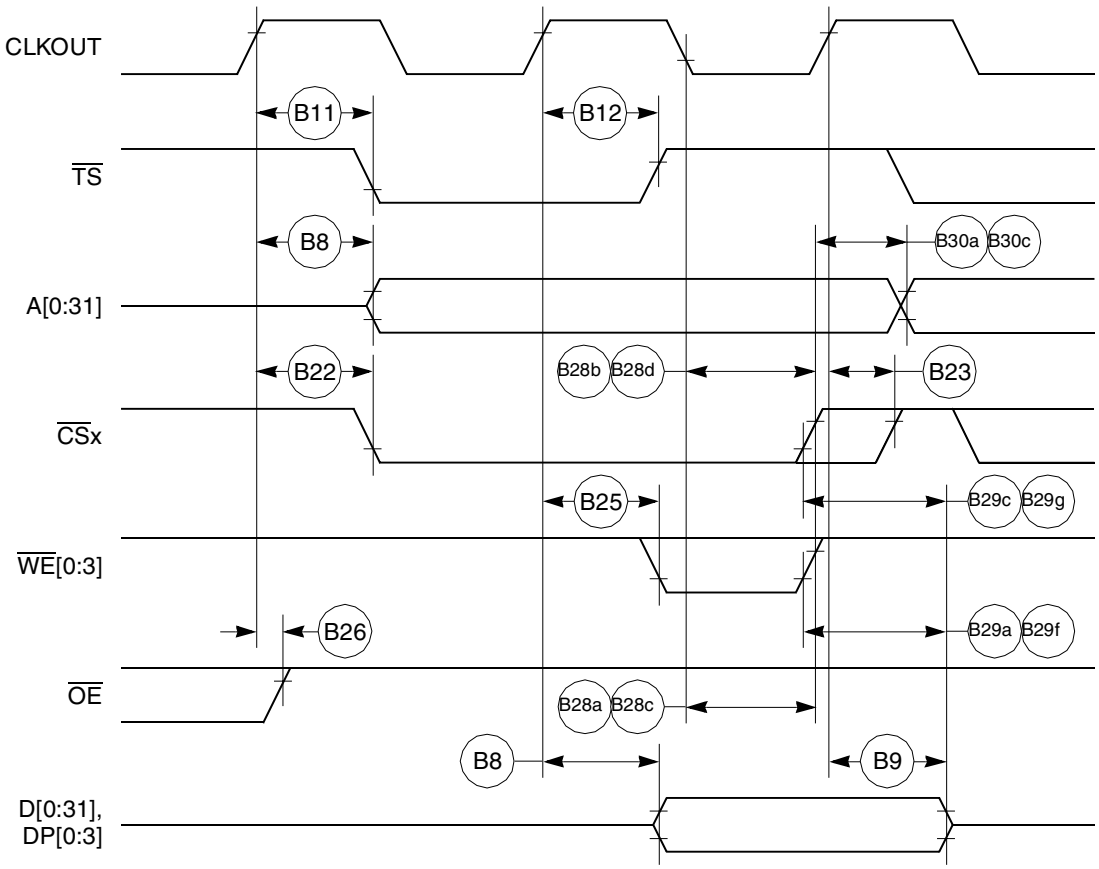

Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

Figure 20 provides the timing for the synchronous external master access controlled by the GPCM.

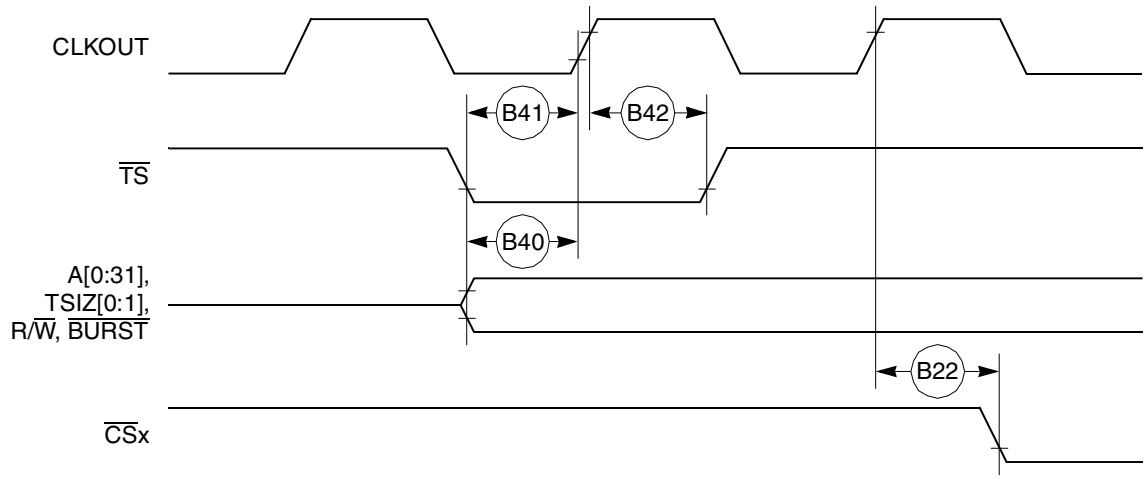

Figure 20. Synchronous External Master Access Timing (GPCM Handled—ACS = 00)

Figure 21 provides the timing for the asynchronous external master memory access controlled by the GPCM.

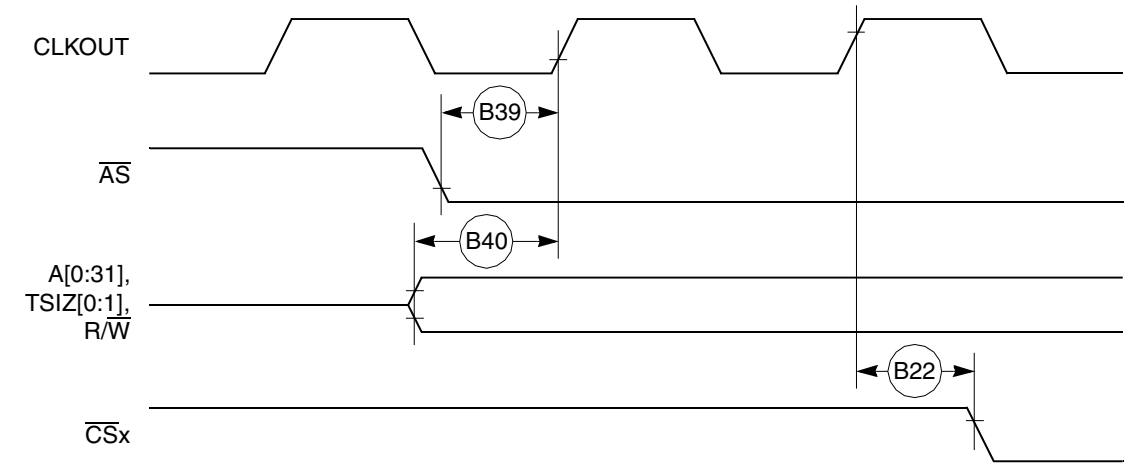

Figure 21. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 22 provides the timing for the asynchronous external master control signals negation.

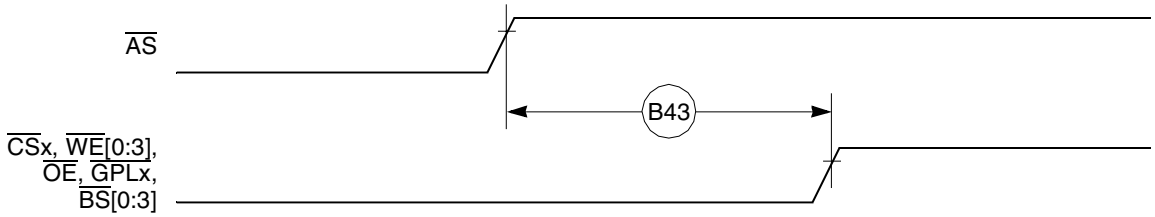

Figure 22. Asynchronous External Master—Control Signals Negation Timing

Figure 25 provides the PCMCIA access cycle timing for the external bus read.

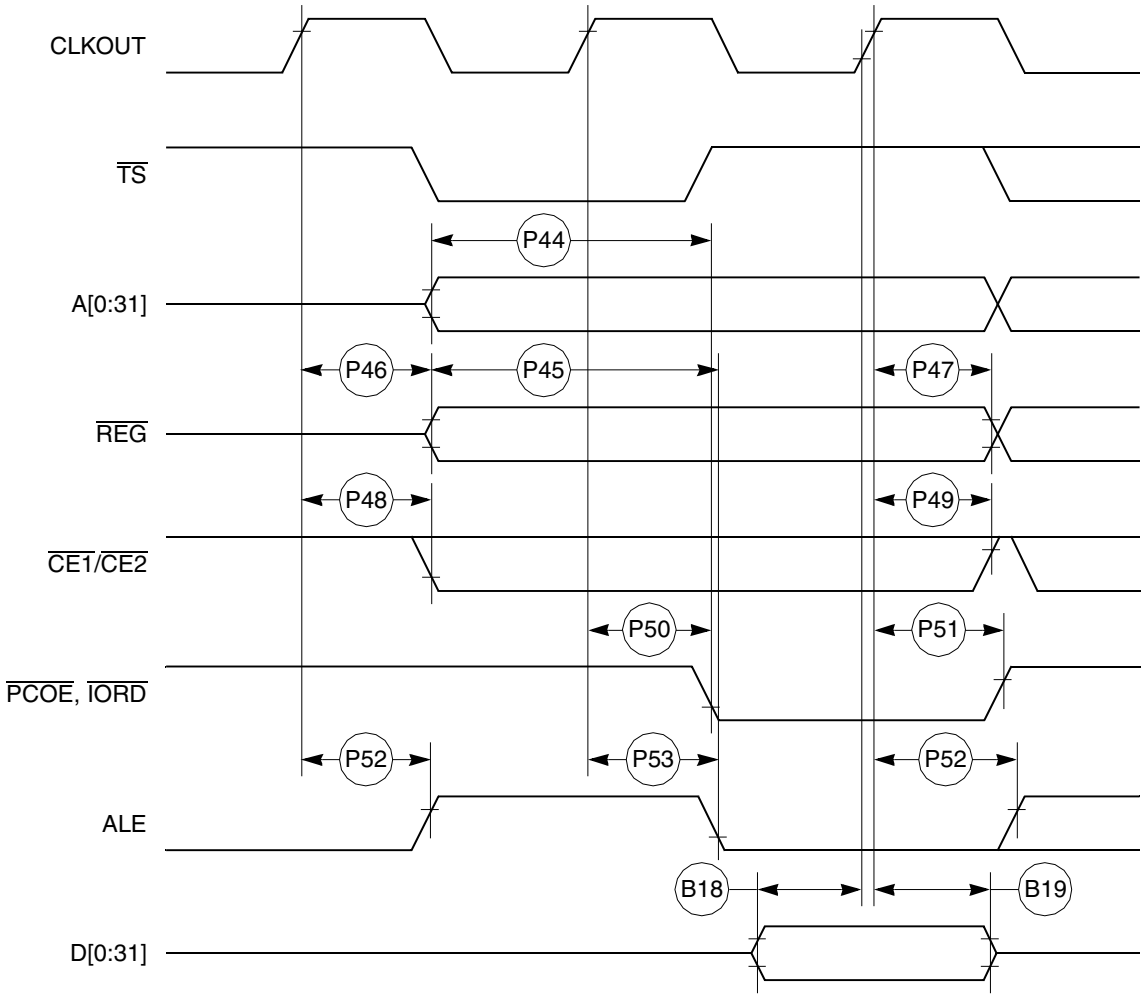

Figure 25. PCMCIA Access Cycles Timing External Bus Read

Figure 34 provides the reset timing for the debug port configuration.

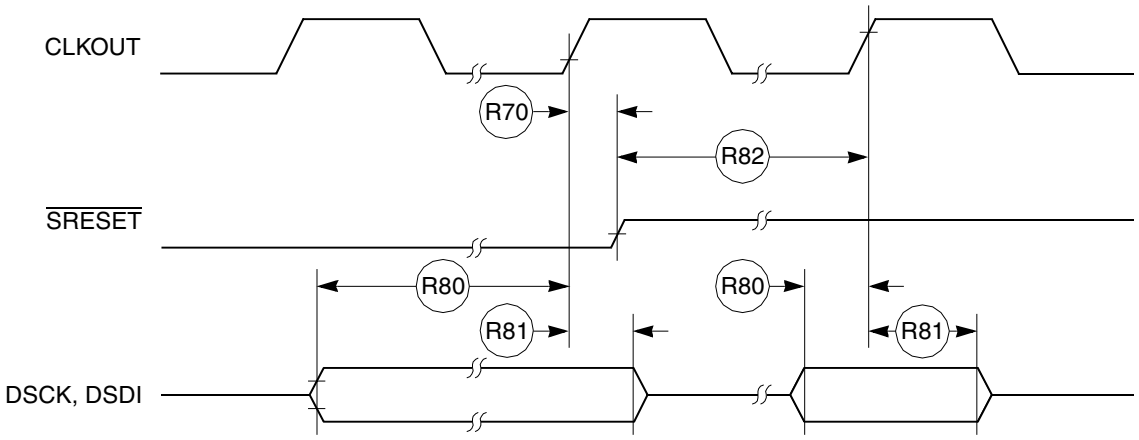

Figure 34. Reset Timing—Debug Port Configuration

12 IEEE 1149.1 Electrical Specifications

Table 15 provides the JTAG timings for the MPC853T shown in Figure 35 to Figure 38.

Table 15. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

Table 20. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
75	L1RSYNCB, L1TSYNCB rise/fall time	—	15.00	ns
76	L1RXDB valid to L1CLKB edge (L1RXDB setup time)	17.00	—	ns
77	L1CLKB edge to L1RXDB invalid (L1RXDB hold time)	13.00	—	ns
78	L1CLKB edge to L1ST1 and L1ST2 valid [4]	10.00	45.00	ns
78A	L1SYNCB valid to L1ST1 and L1ST2 valid	10.00	45.00	ns
79	L1CLKB edge to L1ST1 and L1ST2 invalid	10.00	45.00	ns
80	L1CLKB edge to L1TXDB valid	10.00	55.00	ns
80A	L1TSYNCB valid to L1TXDB valid [4]	10.00	55.00	ns
81	L1CLKB edge to L1TXDB high impedance	0.00	42.00	ns
82	L1RCLKB, L1TCLKB frequency (DSC =1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLKB, L1TCLKB width low (DSC =1)	P + 10	—	ns
83a	L1RCLKB, L1TCLKB width high (DSC = 1)[3]	P + 10	—	ns
84	L1CLKB edge to L1CLKOB valid (DSC = 1)	—	30.00	ns
85	$\overline{\text{L1RQB}}$ valid before falling edge of L1TSYNCB[4]	1.00	—	L1TCLK
86	L1GRB setup time[2]	42.00	—	ns
87	L1GRB hold time	42.00	—	ns
88	L1CLKB edge to L1SYNCB valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

1 The ratio SyncCLK/L1RCLKB must be greater than 2.5/1.

2 These specs are valid for IDL mode only.

3 Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.

4 These strobes and TxD on the first bit of the frame become valid after L1CLKB edge or L1SYNCB, whichever comes later.

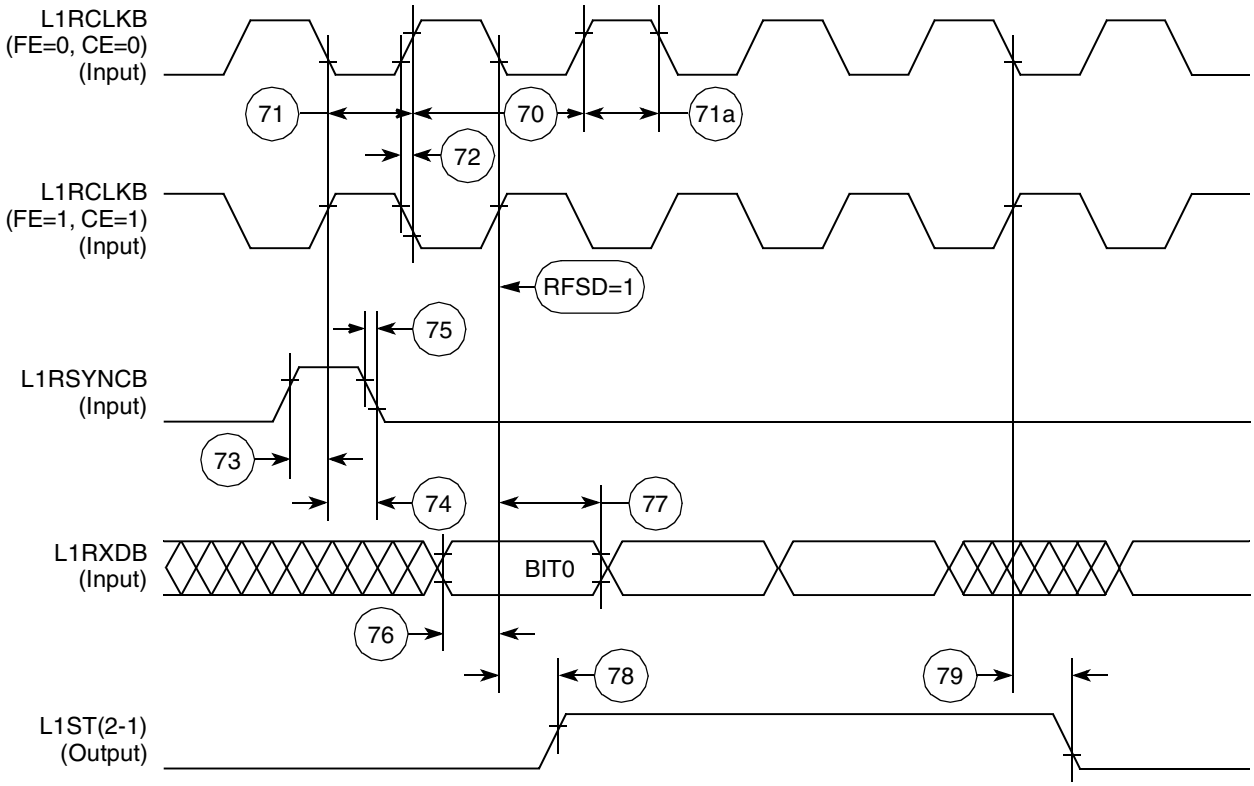

Figure 46. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

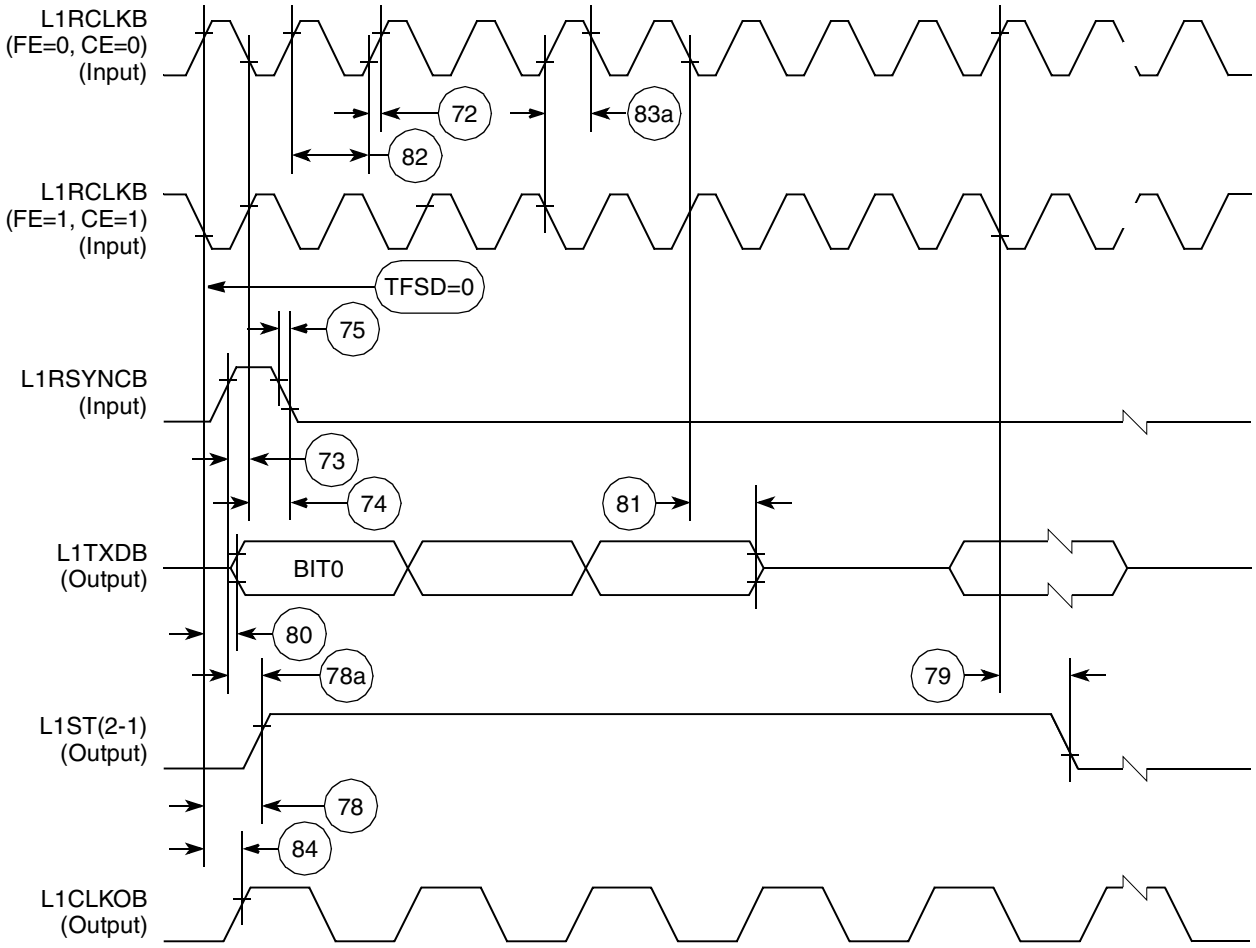

Figure 49. SI Transmit Timing with Double Speed Clocking (DSC = 1)

Figure 51 through Figure 53 show the NMSI timings.

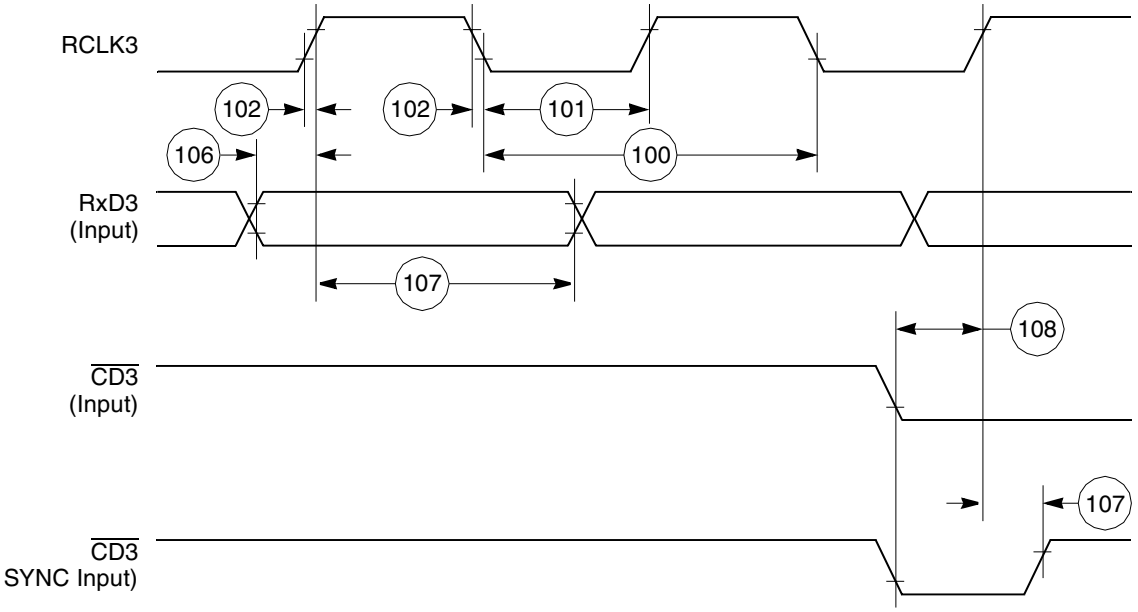

Figure 51. SCC NMSI Receive Timing Diagram

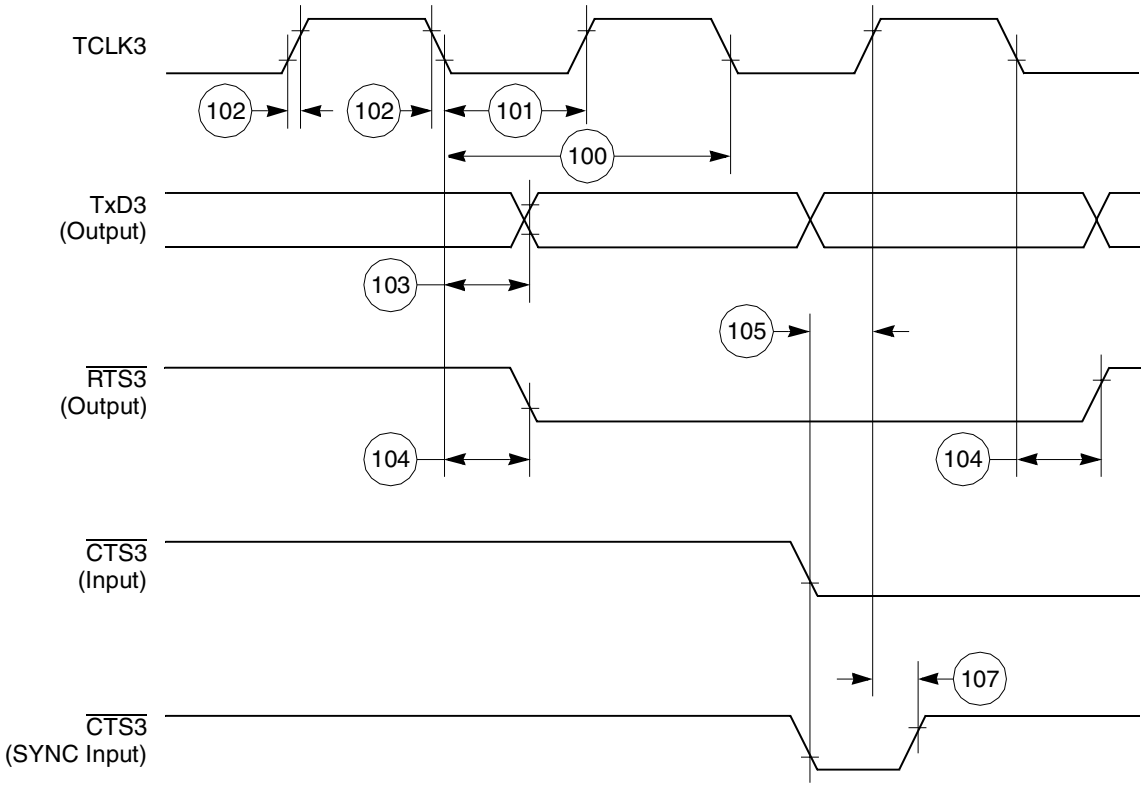

Figure 52. SCC NMSI Transmit Timing Diagram

13.8 SPI Master AC Electrical Specifications

Table 24 provides the SPI master timings as shown in Figure 59 and Figure 60.

Table 24. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	MASTER cycle time	4	1024	t_{cyc}
161	MASTER clock (SCK) high or low time	2	512	t_{cyc}
162	MASTER data setup time (inputs)	15	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	10	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns

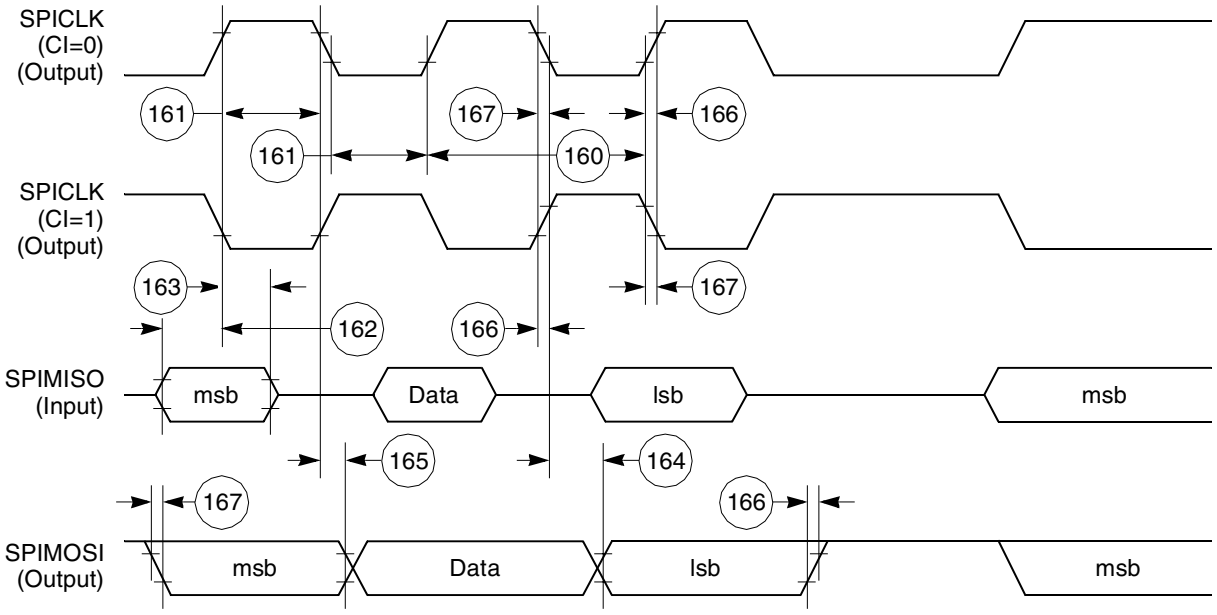

Figure 59. SPI Master (CP = 0) Timing Diagram

Figure 64 shows the MII transmit signal timing diagram.

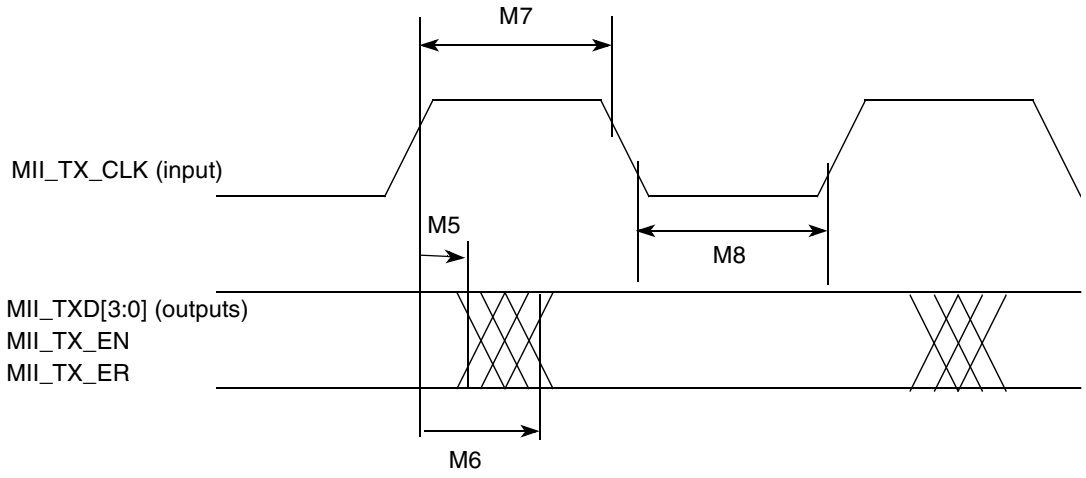

Figure 64. MII Transmit Signal Timing Diagram

14.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 28 provides information on the MII async inputs signal timing.

Table 28. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 65 shows the MII asynchronous inputs signal timing diagram.

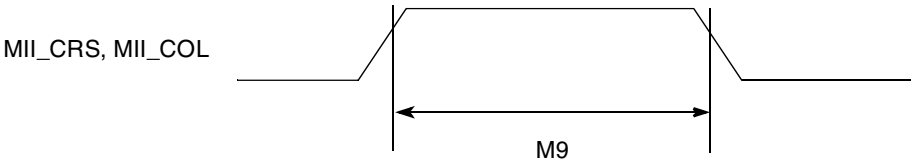

Figure 65. MII Async Inputs Timing Diagram

14.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 29 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Table 29. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns

Table 31. Pin Assignments - JEDEC Standard (continued)

Name	Pin Number	Type
CS[0:5]	B2, A2, D3, C3, E6, C4	Output
CS6	D4	Output
CS7	A3	Output
WE0 BS_B0 IORD	D6	Output
WE1 BS_B1 IOWR	C6	Output
WE2 BS_B2 PCOE	A5	Output
WE3 BS_B3 PCWE	B5	Output
BS_A[0:3]	A6, D7, C7, B7	Output
GPL_A0 GPL_B0	C5	Output
OE GPL_A1 GPL_B1	D5	Output
GPL_A[2:3] GPL_B[2:3] CS[2–3]	A4, B4	Output
UPWAITA GPL_A4	C2	Bidirectional (3.3V only)
GPL_A5	E4	Output
PORESET	P1	Input (3.3V only)
RSTCONF	K4	Input (3.3V only)
HRESET	J4	Open-drain
SRESET	M3	Open-drain
XTAL	N1	Analog Output
EXTAL	M1	Analog Input (1.8V only)
CLKOUT	N6	Output
EXTCLK	N2	Input (1.8V only)
ALE_A	H1	Output
CE1_A	E5	Output
CE2_A	B3	Output

Table 31. Pin Assignments - JEDEC Standard (continued)

Name	Pin Number	Type
PC12 $\overline{\text{RTS4}}$ L1ST4	E15	Bidirectional (5V tolerant)
PC7 L1TSYNCB $\overline{\text{CTS3}}$	J14	Bidirectional (5V tolerant)
PC6 L1RSYNCB $\overline{\text{CD3}}$	K15	Bidirectional (5V tolerant)
PC5 $\overline{\text{CTS4}}$ SDACK1	J13	Bidirectional (5V tolerant)
PC4 $\overline{\text{CD4}}$	L14	Bidirectional (5V tolerant)
PD15 MII-RXD3	M14	Bidirectional (5V tolerant)
PD14 MII-RXD2	N16	Bidirectional (5V tolerant)
PD13 MII-RXD1	K13	Bidirectional (5V tolerant)
PD12 MII-MDC	N15	Bidirectional (5V tolerant)
PD11 RXD3 MII-TXERR	P16	Bidirectional (5V tolerant)
PD10 TXD3 MII-RXD0	R15	Bidirectional (5V tolerant)
PD9 RXD4 MII-TXD0	N14	Bidirectional (5V tolerant)
PD8 TXD4 MII_RX_CLK	M13	Bidirectional (5V tolerant)
PD7 $\overline{\text{RTS3}}$ MII_RX_ER	T15	Bidirectional (5V tolerant)
PD6 $\overline{\text{RTS4}}$ MII_RX_DV	N13	Bidirectional (5V tolerant)

Table 32. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
IRQ0	R14	Input (3.3 V only)
IRQ1	N12	Input (3.3 V only)
IRQ7 M_TX_CLK	P13	Input (3.3 V only)
CS[0:5]	C3, B3, E4, D4, F7, D5	Output
CS6	E5	Output
CS7	B4	Output
WE0 BS_B0 IORD	E7	Output
WE1 BS_B1 IOWR	D7	Output
WE2 BS_B2 PCOE	B6	Output
WE3 BS_B3 PCWE	C6	Output
BS_A[0:3]	B7, E8, D8, C8	Output
GPL_A0 GPL_B0	D6	Output
OE GPL_A1 GPL_B1	E6	Output
GPL_A[2:3] GPL_B[2:3] CS[2–3]	B5, C5	Output
UPWAITA GPL_A4	D3	Bidirectional (3.3 V only)
GPL_A5	F5	Output
PORESET	R2	Input (3.3 V only)
RSTCONF	L5	Input (3.3 V only)
HRESET	K5	Open drain
SRESET	N4	Open drain
XTAL	P2	Analog output
EXTAL	N2	Analog Input (3.3 V only)

Table 32. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
CLKOUT	P7	Output
EXTCLK	P3	Input (3.3 V only)
ALE_A	J2	Output
$\overline{\text{CE1\_A}}$	F6	Output
$\overline{\text{CE2\_A}}$	C4	Output
$\overline{\text{WAIT\_A}}$	P4	Input (3.3 V only)
IP_A0	U3	Input (3.3 V only)
IP_A1	N7	Input (3.3 V only)
IP_A2 $\overline{\text{IOIS16\_A}}$	T4	Input (3.3 V only)
IP_A3	N6	Input (3.3 V only)
IP_A4	U4	Input (3.3 V only)
IP_A5	P6	Input (3.3 V only)
IP_A6	N8	Input (3.3 V only)
IP_A7	T3	Input (3.3 V only)
DSCK	J3	Bidirectional Three-state (3.3 V only)
IWP[0:1] VFLS[0:1]	J4, H2	Bidirectional (3.3 V only)
OP0	L2	Bidirectional (3.3 V only)
OP1	L3	Output
OP2 MODCK1 $\overline{\text{STS}}$	L4	Bidirectional (3.3 V only)
OP3 MODCK2 DSDO	M2	Bidirectional (3.3 V only)
BADDR[28:29]	M4, M3	Output
BADDR30 $\overline{\text{REG}}$	K4	Output
$\overline{\text{AS}}$	K3	Input (3.3 V only)
PA11 RXD3 L1TXDB	F17	Bidirectional (Optional: open-drain) (5-V tolerant)

Table 32. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
PA10 TXD3 L1RXDB	J16	Bidirectional (Optional: open-drain) (5-V tolerant)
PA9 RXD4	K17	Bidirectional (Optional: open-drain) (5-V tolerant)
PA8 TXD4	K16	Bidirectional (Optional: open-drain) (5-V tolerant)
PA3 CLK5 BRGO3 TIN3	L17	Bidirectional (5-V tolerant)
PA2 CLK6 $\overline{\text{TOUT3}}$ L1RCLKB	L15	Bidirectional (5-V tolerant)
PA1 CLK7 BRGO4 TIN4	M16	Bidirectional (5-V tolerant)
PA0 CLK8 $\overline{\text{TOUT4}}$ L1TCLKB	N17	Bidirectional (5-V tolerant)
PB31 $\overline{\text{SPISEL}}$	F14	Bidirectional (Optional: open-drain) (5-V tolerant)
PB30 SPICLK	G14	Bidirectional (Optional: open-drain) (5-V tolerant)
PB29 SPIMOSI	E16	Bidirectional (Optional: open-drain) (5-V tolerant)
PB28 SPIMISO BRGO4	H14	Bidirectional (Optional: open-drain) (5-V tolerant)
PB25 SMTXD1	J15	Bidirectional (Optional: open-drain) (5-V tolerant)