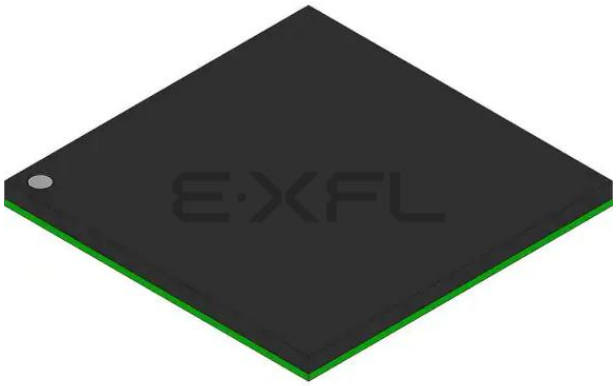

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	100MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc853tzt100a

and incorporates memory management units (MMUs), instruction and data caches. The MPC853T is a subset of this family of devices and is the main focus of this document.

2 Features

The MPC853T is comprised of three modules that each use the 32-bit internal bus: a MPC8xx core, a system integration unit (SIU), and a communications processor module (CPM). The MPC853T block diagram is shown in Figure 1.

The following list summarizes the key MPC853T features:

- Embedded MPC8xx core up to 100 MHz
- Maximum frequency operation of the external bus is 66 MHz
  - The 50-/66-MHz core frequencies support both the 1:1 and 2:1 modes.
  - The 80-/100-MHz core frequencies support 2:1 mode only.
- Single-issue, 32-bit core (compatible with the PowerPC architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch and without conditional execution.
  - 4-Kbyte data cache and 4-Kbyte instruction cache
    - Instruction cache is two-way, set-associative with 128 sets
    - Data cache is two-way, set-associative with 128 sets
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry translation look-aside buffer (TLB), fully associative instruction, and data TLBs
  - MMUs support multiple page sizes of 4 Kbytes, 16 Kbytes, 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank.
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROMs, Flash EPROMs, and other memory devices
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbytes–256 Mbytes)
  - Selectable write protection
  - On-chip bus arbitration logic
- Fast Ethernet Controller (FEC)

- SPI (serial peripheral interface)
  - Supports master and slave modes
  - Supports multiple-master operation on the same bus
- The MPC853T has a time-slot assigner (TSA) that supports one TDM bus (TDMb)
  - Allows SCCs and SMC to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame synchronization, and clocking
  - Allows dynamic changes
  - Can be internally connected to three serial channels (two SCCs and one SMC)
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant
  - Supports one independent PCMCIA socket, 8 memory or I/O windows
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a break point internally
- Normal high and normal low power modes to conserve power
- 1.8-V core and 3.3-V I/O operation with 5-V TTL compatibility. Refer to Table 5 for a listing of the 5-V tolerant pins.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages, and especially PBGA packages, is strongly dependent on the board temperature. If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)
T_B = board temperature ºC
P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

Table 6. Mandatory Reset Configuration of MPC853T (continued)

Register/Configuration	Field	Value (binary)
PCPAR (Port C pin assignment register)	PCPAR[8:11] PCDIR[14]	0
PCDIR (Port C data direction register)	PCDIR[8:11] PCDIR[14]	1

10 Layout Practices

Each V_{DD} pin on the MPC853T should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1-µF bypass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized, and additional appropriate decoupling capacitors should be used if required. Capacitor leads and associated printed circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as V_{DD} and GND planes should be used.

All output pins on the MPC853T have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads, as well as parasitic capacitances caused by the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{DD} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, please refer to Section 14.4.3, "Clock Synthesizer Power (V_{DDSYN}, V_{SSSYN}, V_{SSSYN1})" in the *MPC866 PowerQUICC Family User's Manual*.

11 Bus Signal Timing

The maximum bus speed supported by the MPC853T is 66 MHz. Table 7 shows the frequency ranges for standard part frequencies in 1:1 bus mode.

Table 7. Frequency Ranges for Standard Part Frequencies (1:1 Bus Mode)

Part Frequency	50 MHz		66 MHz	
	Min	Max	Min	Max
Core Frequency	40	50	40	66.67
Bus Frequency	40	50	40	66.67

Table 8 shows the frequency ranges for standard part frequencies in 2:1 bus mode.

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B17	CLKOUT to $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ valid (hold time) (MIN = 0.00 × B1 + 1.00 [4])	1.00	—	1.00	—	1.00	—	2.00	—	ns
B17a	CLKOUT to $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) [5] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) [5] (MIN = 0.00 × B1 + 1.00 [6])	1.00	—	1.00	—	1.00	—	2.00	—	ns
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) [7](MIN = 0.00 × B1 + 4.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold Time) [7] (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22a	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MAX = 0.00 × B1 + 8.00)	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22c	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	16.00	7.00	14.10	5.20	12.30	ns
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 (MAX = 0.00 × B1 + 8.00)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11 TRLX = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3)/BS_B[0:3] asserted (MAX = 0.00 × B1 + 9.00)	—	9.00		9.00		9.00		9.00	ns

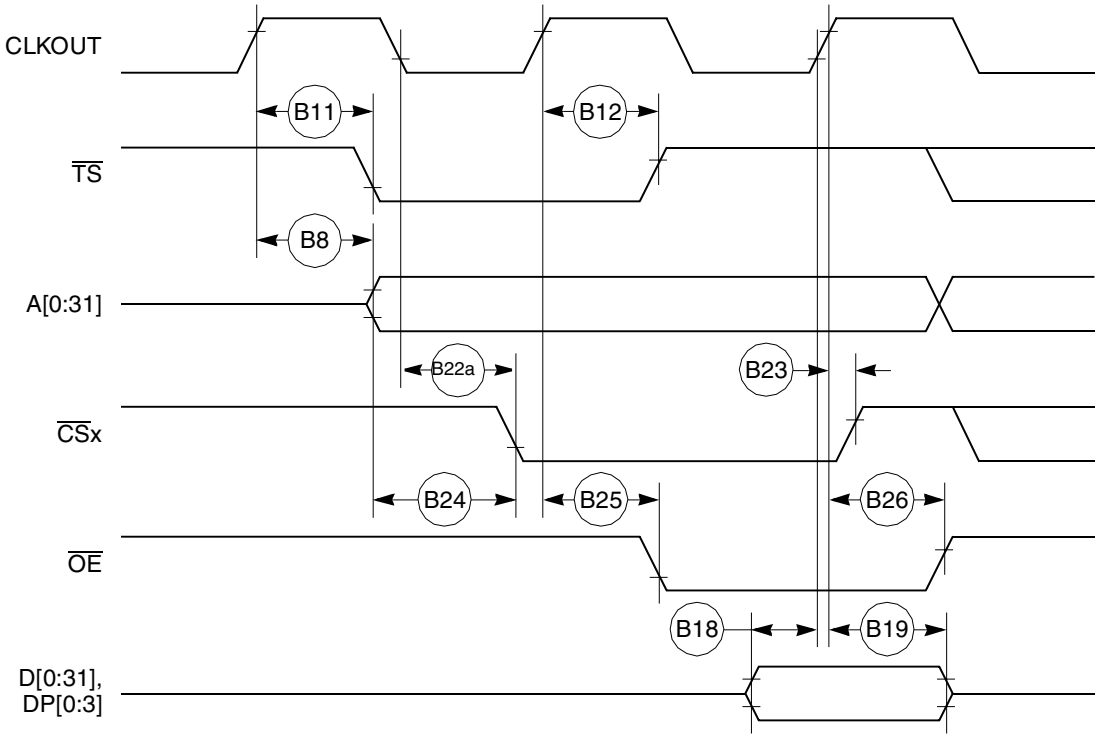


Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

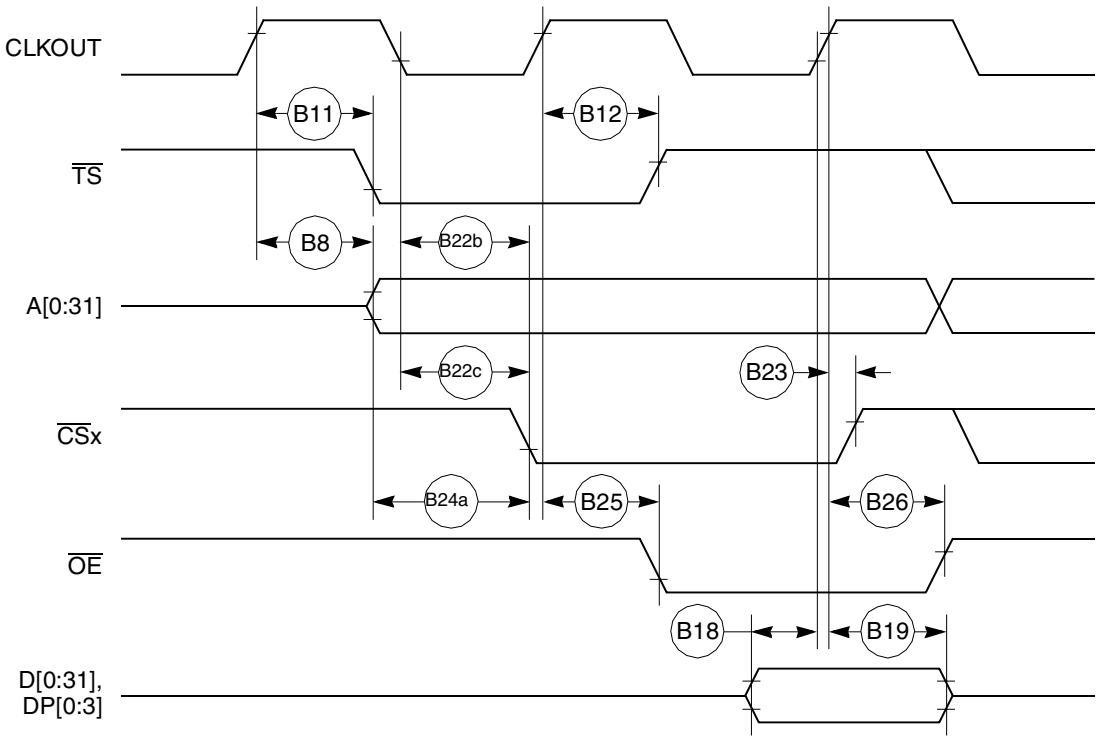


Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

Table 12 shows the PCMCIA port timing for the MPC853T.

Table 12. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
J95	CLKOUT to OPx valid (MAX = 0.00 × B1 + 19.00)	—	19.00	—	19.00	—	19.00	—	19.00	ns
J96	$\overline{\text{HRESET}}$ negated to OPx drive [1] (MIN = 0.75 × B1 + 3.00)	25.70	—	21.70	—	18.00	—	14.40	—	ns
J97	IP_Xx valid to CLKOUT rising edge (MIN = 0.00 × B1 + 5.00)	5.00	—	5.00	—	5.00	—	5.00	—	ns
J98	CLKOUT rising edge to IP_Xx invalid (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns

1 OP2 and OP3 only.

Figure 28 provides the PCMCIA output port timing for the MPC853T.

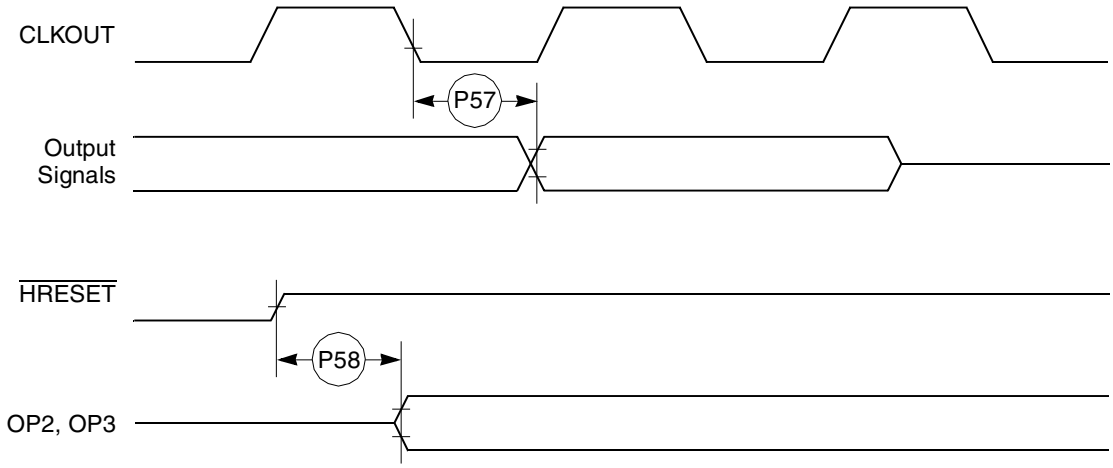


Figure 28. PCMCIA Output Port Timing

Figure 29 provides the PCMCIA in put port timing for the MPC853T.

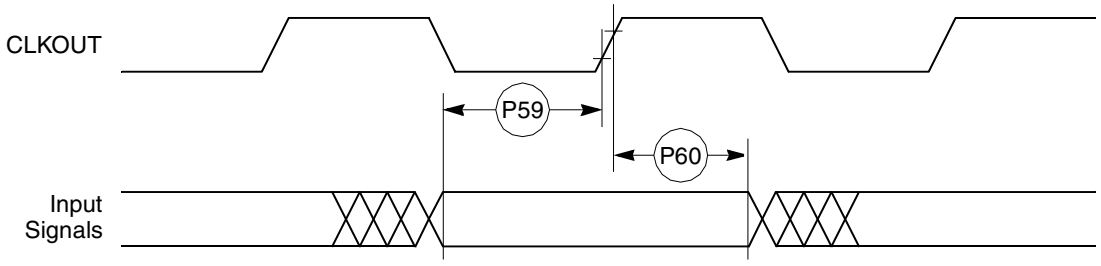


Figure 29. PCMCIA Input Port Timing

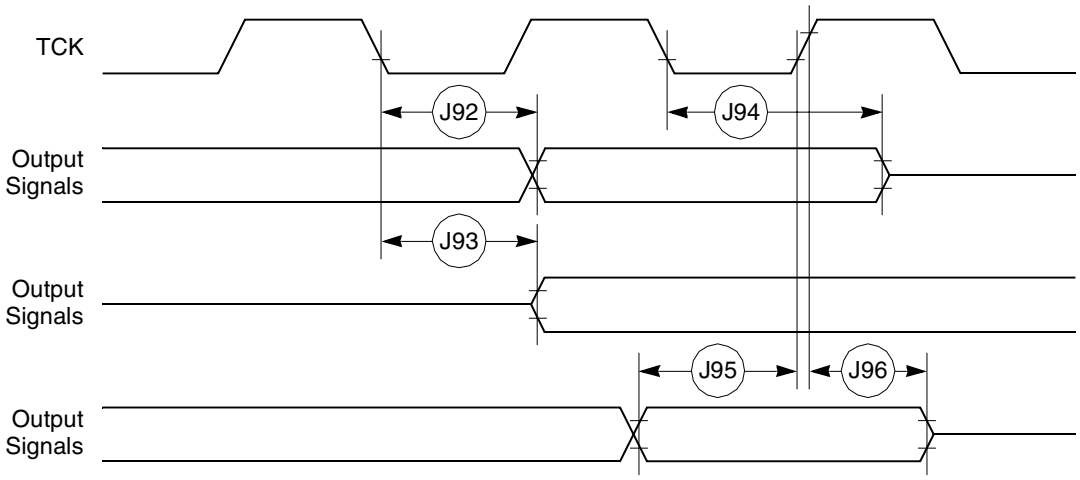


Figure 38. Boundary Scan (JTAG) Timing Diagram

13 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC853T.

13.1 Port C Interrupt AC Electrical Specifications

Table 16 provides the timings for port C interrupts.

Table 16. Port C Interrupt Timing

Num	Characteristic	33.34 MHz		Unit
		Min	Max	
35	Port C interrupt pulse width low (edge-triggered mode)	55	—	ns
36	Port C interrupt minimum time between active edges	55	—	ns

Figure 39 shows the port C interrupt detection timing.

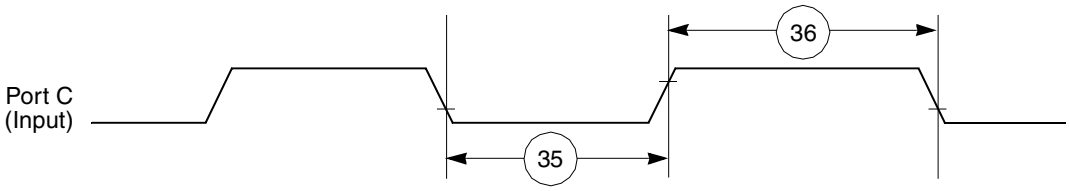


Figure 39. Port C Interrupt Detection Timing

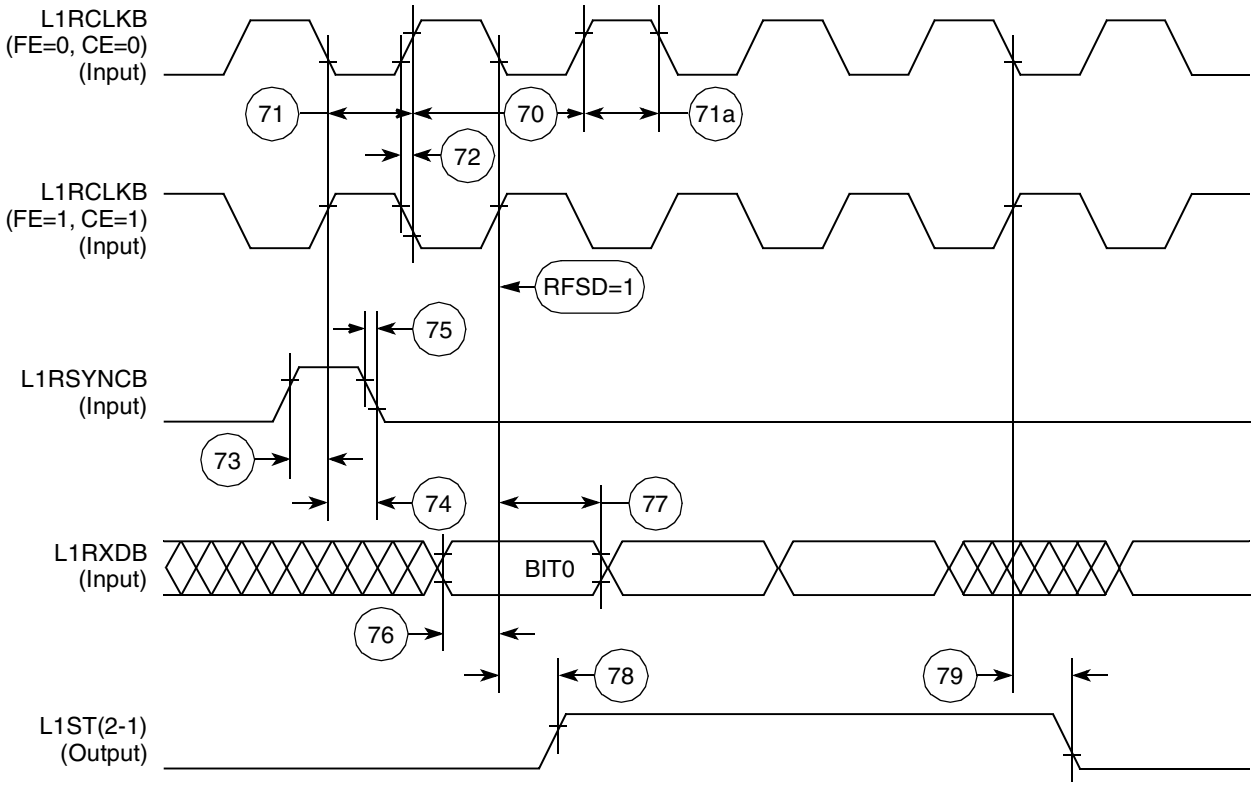


Figure 46. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

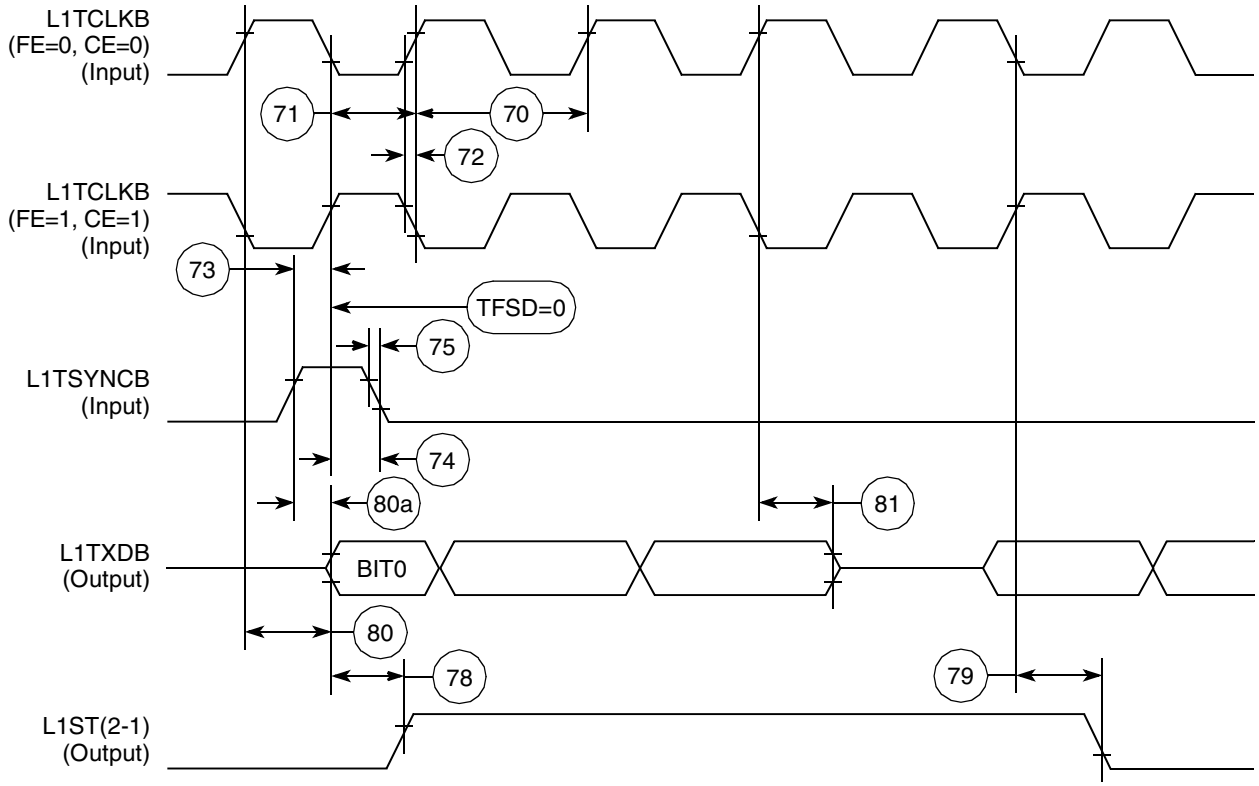


Figure 48. SI Transmit Timing Diagram (DSC = 0)

Table 23. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLK3 rising edge)	10	50	ns
135	$\overline{\text{RSTRT}}$ active delay (from TCLK3 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK3 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted [2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated [2]	—	20	ns

1 The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater than or equal to 2/1.

2 $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

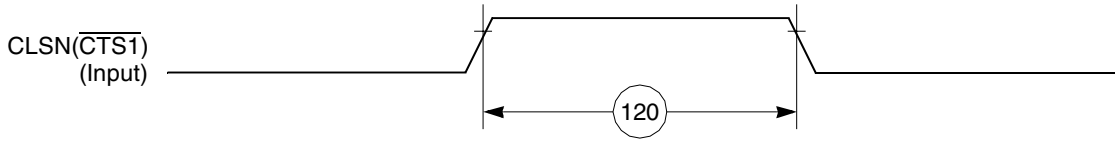


Figure 54. Ethernet Collision Timing Diagram

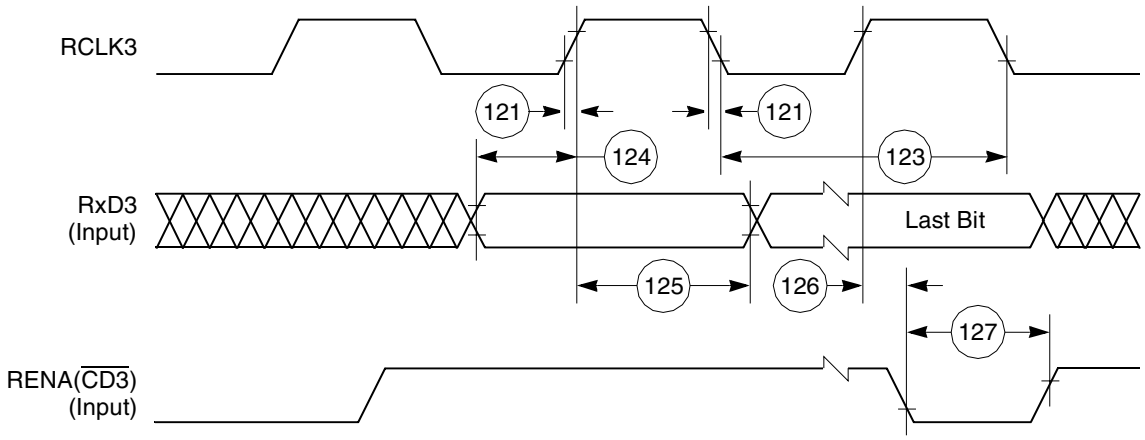
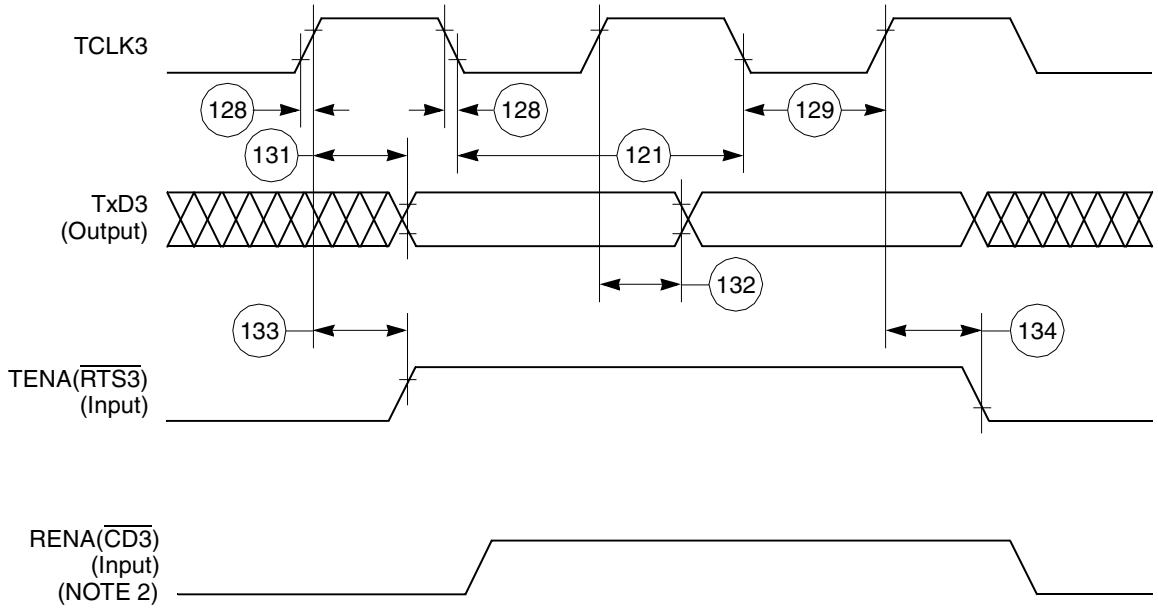


Figure 55. Ethernet Receive Timing Diagram



NOTES:
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is negated before TENA or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 56. Ethernet Transmit Timing Diagram

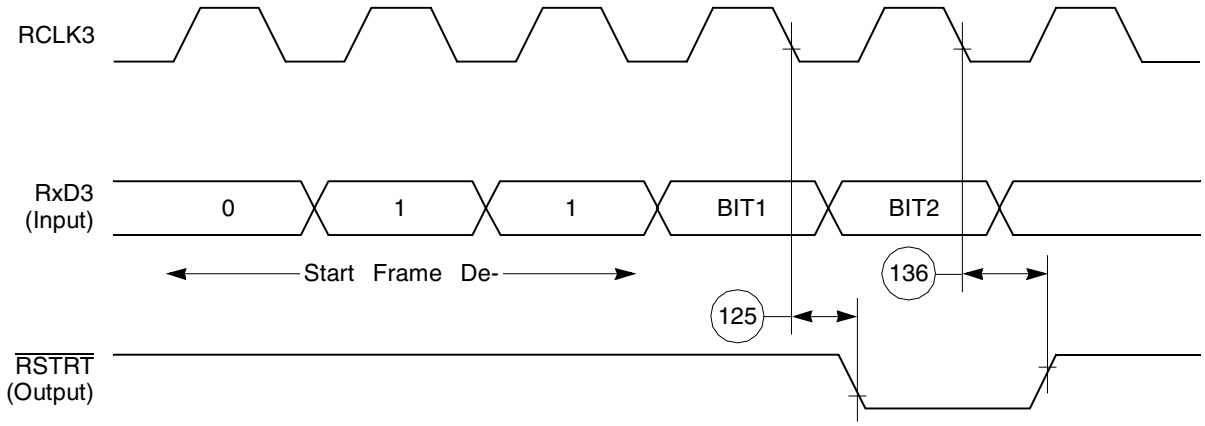


Figure 57. CAM Interface Receive Start Timing Diagram

Figure 58. CAM Interface REJECT Timing Diagram

13.8 SPI Master AC Electrical Specifications

Table 24 provides the SPI master timings as shown in Figure 59 and Figure 60.

Table 24. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	MASTER cycle time	4	1024	t_{cyc}
161	MASTER clock (SCK) high or low time	2	512	t_{cyc}
162	MASTER data setup time (inputs)	15	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	10	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns

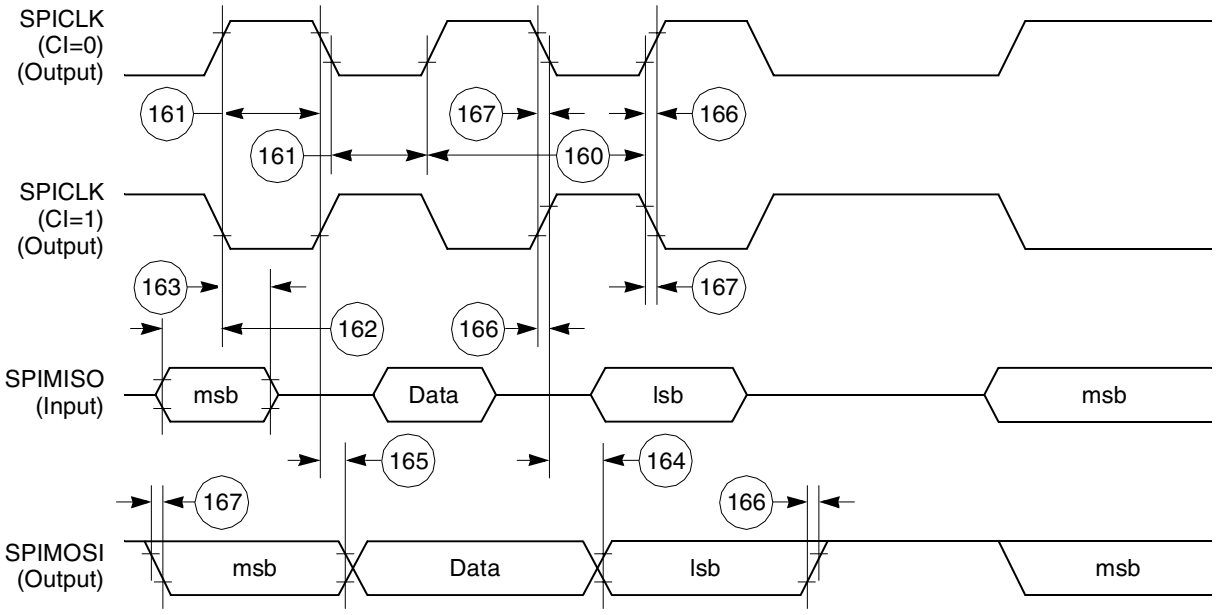


Figure 59. SPI Master (CP = 0) Timing Diagram

Figure 64 shows the MII transmit signal timing diagram.

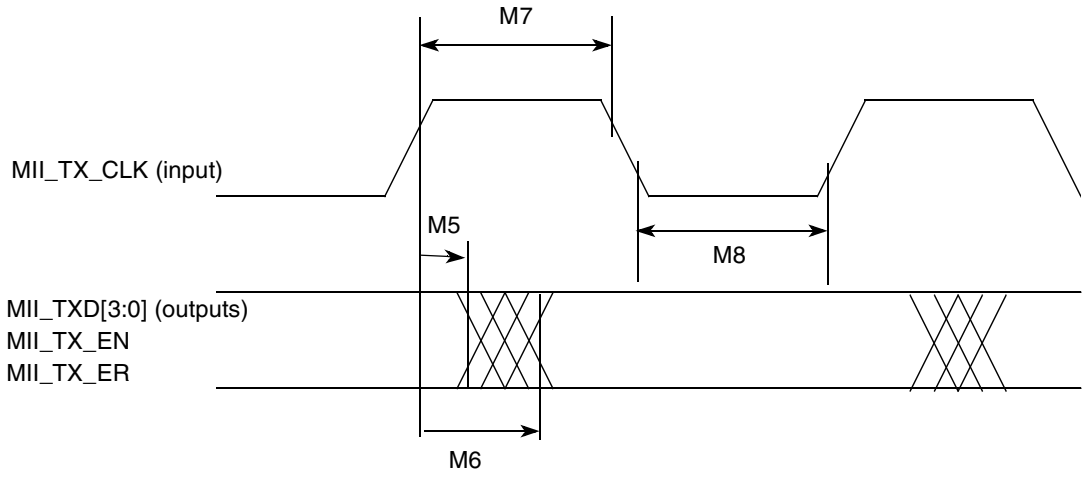


Figure 64. MII Transmit Signal Timing Diagram

14.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 28 provides information on the MII async inputs signal timing.

Table 28. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 65 shows the MII asynchronous inputs signal timing diagram.

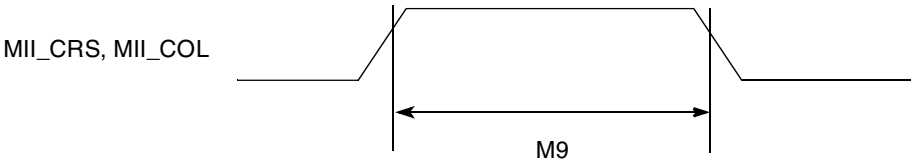


Figure 65. MII Async Inputs Timing Diagram

14.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 29 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Table 29. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns

Table 31. Pin Assignments - JEDEC Standard (continued)

Name	Pin Number	Type
PA3 CLK5 BRGO3 TIN3	K16	Bidirectional (5V tolerant)
PA2 CLK6 $\overline{\text{TOUT3}}$ L1RCLKB	K14	Bidirectional (5V tolerant)
PA1 CLK7 BRGO4 TIN4	L15	Bidirectional (5V tolerant)
PA0 CLK8 $\overline{\text{TOUT4}}$ L1TCLKB	M16	Bidirectional (5V tolerant)
PB31 $\overline{\text{SPISEL}}$	E13	Bidirectional (Optional: Open-drain) (5V tolerant)
PB30 SPICLK	F13	Bidirectional (Optional: Open-drain) (5V tolerant)
PB29 SPIMOSI	D15	Bidirectional (Optional: Open-drain) (5V tolerant)
PB28 SPIMISO BRGO4	G13	Bidirectional (Optional: Open-drain) (5V tolerant)
PB25 SMTXD1	H14	Bidirectional (Optional: Open-drain) (5V tolerant)
PB24 SMRXD1	H16	Bidirectional (Optional: Open-drain) (5V tolerant)
PB15 BRGO3	L16	Bidirectional (5V tolerant)
PC15 $\overline{\text{DREQ0}}$	C16	Bidirectional (5V tolerant)
PC13 $\overline{\text{RTS3}}$ $\overline{\text{L1RQB}}$ L1ST3	E14	Bidirectional (5V tolerant)

Table 32. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
IRQ0	R14	Input (3.3 V only)
IRQ1	N12	Input (3.3 V only)
IRQ7 M_TX_CLK	P13	Input (3.3 V only)
CS[0:5]	C3, B3, E4, D4, F7, D5	Output
CS6	E5	Output
CS7	B4	Output
WE0 BS_B0 IORD	E7	Output
WE1 BS_B1 IOWR	D7	Output
WE2 BS_B2 PCOE	B6	Output
WE3 BS_B3 PCWE	C6	Output
BS_A[0:3]	B7, E8, D8, C8	Output
GPL_A0 GPL_B0	D6	Output
OE GPL_A1 GPL_B1	E6	Output
GPL_A[2:3] GPL_B[2:3] CS[2–3]	B5, C5	Output
UPWAITA GPL_A4	D3	Bidirectional (3.3 V only)
GPL_A5	F5	Output
PORESET	R2	Input (3.3 V only)
RSTCONF	L5	Input (3.3 V only)
HRESET	K5	Open drain
SRESET	N4	Open drain
XTAL	P2	Analog output
EXTAL	N2	Analog Input (3.3 V only)

Table 32. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
CLKOUT	P7	Output
EXTCLK	P3	Input (3.3 V only)
ALE_A	J2	Output
$\overline{\text{CE1\_A}}$	F6	Output
$\overline{\text{CE2\_A}}$	C4	Output
$\overline{\text{WAIT\_A}}$	P4	Input (3.3 V only)
IP_A0	U3	Input (3.3 V only)
IP_A1	N7	Input (3.3 V only)
IP_A2 $\overline{\text{IOIS16\_A}}$	T4	Input (3.3 V only)
IP_A3	N6	Input (3.3 V only)
IP_A4	U4	Input (3.3 V only)
IP_A5	P6	Input (3.3 V only)
IP_A6	N8	Input (3.3 V only)
IP_A7	T3	Input (3.3 V only)
DSCK	J3	Bidirectional Three-state (3.3 V only)
IWP[0:1] VFLS[0:1]	J4, H2	Bidirectional (3.3 V only)
OP0	L2	Bidirectional (3.3 V only)
OP1	L3	Output
OP2 MODCK1 $\overline{\text{STS}}$	L4	Bidirectional (3.3 V only)
OP3 MODCK2 DSDO	M2	Bidirectional (3.3 V only)
BADDR[28:29]	M4, M3	Output
BADDR30 $\overline{\text{REG}}$	K4	Output
$\overline{\text{AS}}$	K3	Input (3.3 V only)
PA11 RXD3 L1TXDB	F17	Bidirectional (Optional: open-drain) (5-V tolerant)

Table 32. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
GND	H7, H8, H9, H10, H11, H12, J7, J8, J9, J10, J11, J12, K7, K8, K9, K10, K11, K12, L7, L8, L9, L10, L11, L12	Power
V_{DDL}	B8, D2, E17, H16, M5, N3, T2, N16, U9	Power
V_{DDH}	G6, G7, G8, G9, G10, G11, G12, G13, H6, H13, J6, J13, K6, K13, L6, L13, M6, M7, M8, M9, M10, M11, M12, M13	Power
N/C	B2, B17, C17, D16, E15, F13, M14, N5, R16, T17, U2, U17	No-connect

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