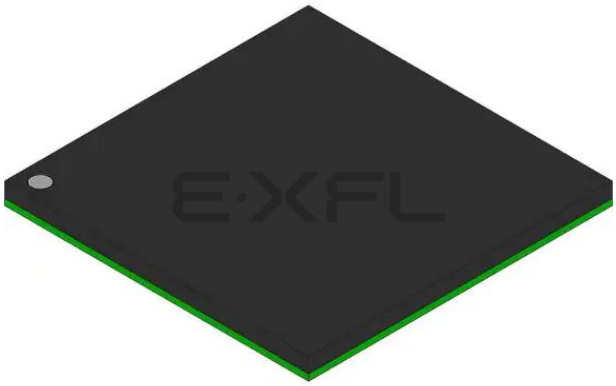

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc853tzt66a

Table 5. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Output high voltage, IOH = –2.0 mA, V_{DDH} = 3.0 V (except XTAL and open-drain pins)	V_{OH}	2.4	—	V
Output low voltage IOL = 2.0 mA (CLKOUT) IOL = 3.2 mA [3] IOL = 5.3 mA [4] IOL = 7.0 mA (Txd1/pa14, txd2/pa12) IOL = 8.9 mA ($\overline{TS}$, $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{HRESET}$, $\overline{SRESET}$)	V_{OL}	—	0.5	V

1 The PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15, PD[3:15], TDI, TDO, TCK, $\overline{TRST}$, TMS, MII_TXEN, and MII_MDIO are 5-V tolerant pins.

2 Input capacitance is periodically sampled.

3 A(0:31), TSIZ0/$\overline{REG}$, TSIZ1, D(0:31), DP(0:3)/$\overline{IRQ}$(3:6), RD/$\overline{WR}$, $\overline{BURST}$, $\overline{RSV}$/$\overline{IRQ2}$, IWP(0:1)/VFLS(0:1), RXD3/PA11, TXD3/PA10, RXD4/PA9, TXD4/PA8, TIN3/BRGO3/CLK5/PA3, BRGCLK2/$\overline{TOUT3}$/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, $\overline{TOUT4}$/CLK8/PA0, $\overline{SPISEL}$/PB31, SPICLK/PB30, SPIMOSI/PB29, BRGO4/SPIMISO/PB28, SMTXD1/PB25, SMRXD1/PB24, BRGO3/PB15, $\overline{RTS1}$/$\overline{DREQ0}$/PC15, $\overline{RTS3}$/PC13, $\overline{RTS4}$/PC12, $\overline{CTS3}$/PC7, $\overline{CD3}$/PC6, $\overline{CTS4}$/$\overline{SDACK1}$/PC5, $\overline{CD4}$/PC4, MII-RXD3/PD15, MII-RXD2/PD14, MII-RXD1/PD13, MII-MDC/PD12, MII-TXERR/RXD3/PD11, MII-RX0/TXD3/PD10, MII-TXD0/RXD4/PD9, MII-RXCLK/TXD4/PD8, MII-TXD3/PD5, MII-RXDV/$\overline{RTS4}$/PD6, MII-RXERR/$\overline{RTS3}$/PD7, MII-TXD2/REJECT3/PD4, MII-TXD1/REJECT4/PD3, MII_CRS, MII_MDIO, MII_TXEN, MII_COL

4 $\overline{BDIP}$/$\overline{GPL\_B}$(5), $\overline{BR}$, $\overline{BG}$, FRZ/$\overline{IRQ6}$, $\overline{CS}$(0:5), $\overline{CS}$(6), $\overline{CS}$(7), $\overline{WE0}$/BS_B0/$\overline{IORD}$, $\overline{WE1}$/BS_B1/$\overline{IOWR}$, $\overline{WE2}$/BS_B2/$\overline{PCOE}$, $\overline{WE3}$/ BS_B3/$\overline{PCWE}$, $\overline{BS\_A}$(0:3), $\overline{GPL\_A0}$/$\overline{GPL\_B0}$, $\overline{OE}$/$\overline{GPL\_A1}$/$\overline{GPL\_B1}$, $\overline{GPL\_A}$(2:3)/$\overline{GPL\_B}$(2:3)/$\overline{CS}$(2:3), UPWAITA/$\overline{GPL\_A4}$, $\overline{GPL\_A5}$, ALE_A, $\overline{CE}$1_A, $\overline{CE}$2_A, DSCK, OP(0:1), OP2/MODCK1/$\overline{STS}$, OP3/MODCK2/DSDO, BADDR(28:30)

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DDL} \times I_{DDL}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

NOTE

The V_{DDSYN} power dissipation is negligible.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature ºC

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (ºC/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

Table 8. Frequency Ranges for Standard Part Frequencies (2:1 Bus Mode)

Part Frequency	50 MHz		66 MHz		80 MHz		100 MHz	
	Min	Max	Min	Max	Min	Max	Min	Max
Core Frequency	40	50	40	66.67	40	80	40	100
Bus Frequency 2:1	20	25	20	33.33	20	40	20	50

Table 9 provides the bus operation timing for the MPC853T at 33, 40, 50, and 66 MHz.

The timing for the MPC853T bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. CLKOUT assumes a 100-pF load maximum delay.

Table 9. Bus Operation Timings

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	Bus period (CLKOUT), see Table 7	—	—	—	—	—	—	—	—	ns
B1a	EXTCLK to CLKOUT phase skew - If CLKOUT is an integer multiple of EXTCLK, then the rising edge of EXTCLK is aligned with the rising edge of CLKOUT. For a non-integer multiple of EXTCLK, this synchronization is lost, and the rising edges of EXTCLK and CLKOUT have a continuously varying phase skew.	–2	+2	–2	+2	–2	+2	–2	+2	ns
B1b	CLKOUT frequency jitter peak-to-peak	—	1	—	1	—	1	—	1	ns
B1c	Frequency jitter on EXTCLK [1]	—	0.50	—	0.50	—	0.50	—	0.50	%
B1d	CLKOUT phase jitter peak-to-peak for OSCLK ≥ 15 MHz	—	4	—	4	—	4	—	4	ns
	CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz	—	5	—	5	—	5	—	5	ns
B2	CLKOUT pulse width low (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns
B3	CLKOUT pulse width high (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns
B4	CLKOUT rise time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B5	CLKOUT fall time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B7a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B7b	CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), $\overline{STS}$ output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30) RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) valid (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B8a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR valid (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B8b	CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{STS}$ valid [3] (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B9	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3), TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, PTR High-Z (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B11	CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion (MAX = 0.25 × B1 + 6.0)	7.60	13.60	6.30	12.30	5.00	11.00	3.80	9.80	ns
B11a	CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.30 [2])	2.50	9.30	2.50	9.30	2.50	9.30	2.50	9.80	ns
B12	CLKOUT to $\overline{TS}$, $\overline{BB}$ negation (MAX = 0.25 × B1 + 4.8)	7.60	12.30	6.30	11.00	5.00	9.80	3.80	8.50	ns
B12a	CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B13	CLKOUT to $\overline{TS}$, $\overline{BB}$ High-Z (MIN = 0.25 × B1)	7.60	21.60	6.30	20.30	5.00	19.00	3.80	14.00	ns
B13a	CLKOUT to $\overline{TA}$, $\overline{BI}$ High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 × B1 + 2.5)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to $\overline{TEA}$ assertion (MAX = 0.00 × B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B15	CLKOUT to $\overline{TEA}$ High-Z (MIN = 0.00 × B1 + 2.50)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	$\overline{TA}$, $\overline{BI}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B16a	$\overline{TEA}$, $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 4.5)	4.50	—	4.50	—	4.50	—	4.50	—	ns
B16b	$\overline{BB}$, $\overline{BG}$, $\overline{BR}$, valid to CLKOUT (setup time) [3] (4MIN = 0.00 × B1 + 0.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns

Figure 9 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

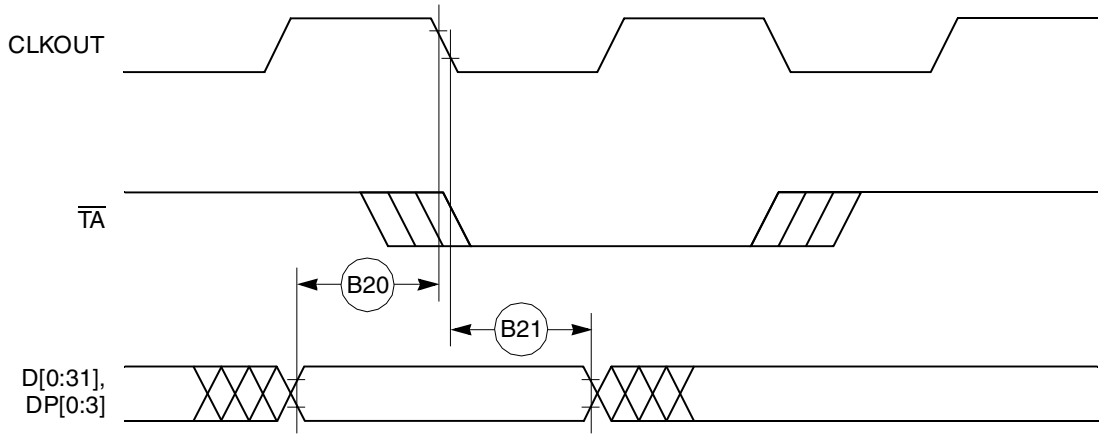

Figure 9. Input Data Timing When Controlled by the UPM in the Memory Controller and DLT3 = 1

Figure 10 through Figure 13 provide the timing for the external bus read controlled by various GPCM factors.

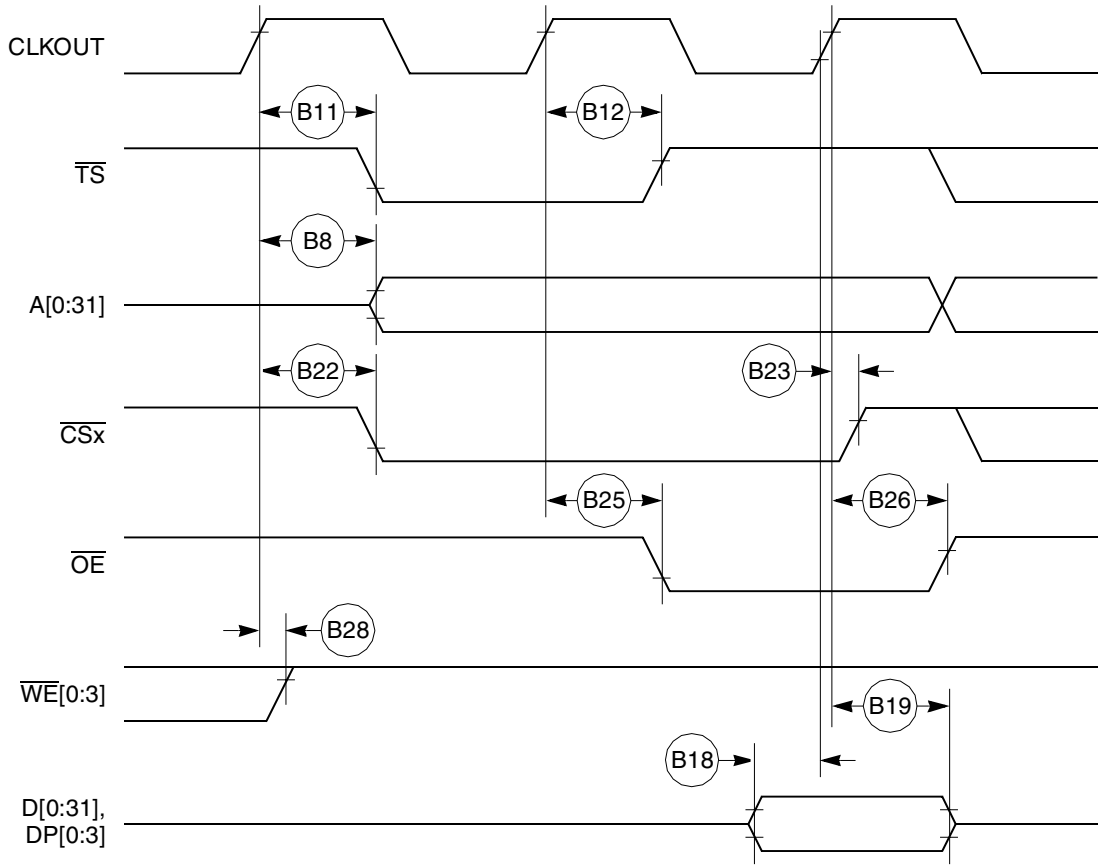

Figure 10. External Bus Read Timing (GPCM Controlled—ACS = 00)

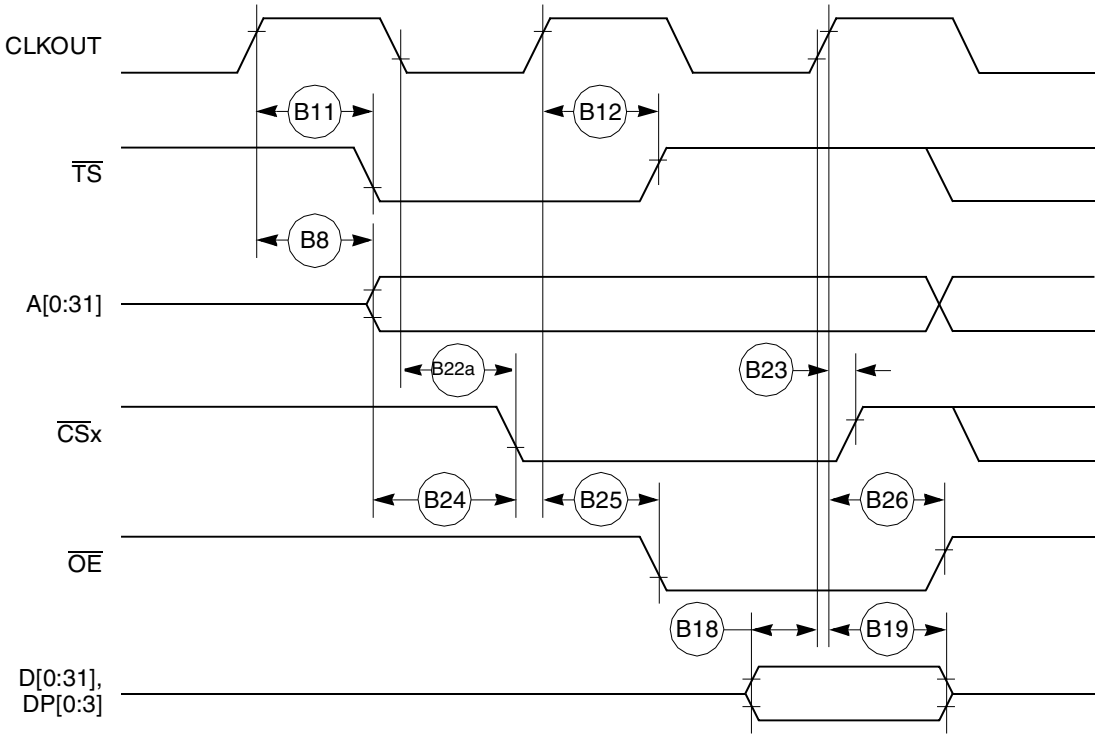

Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

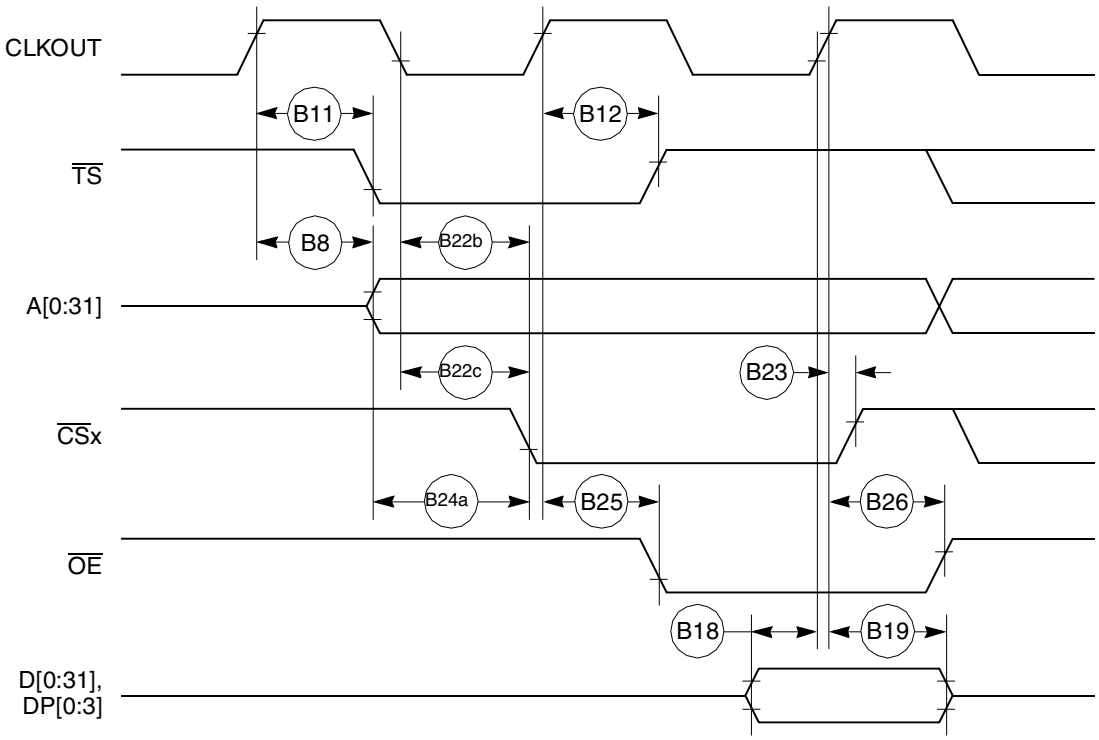

Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

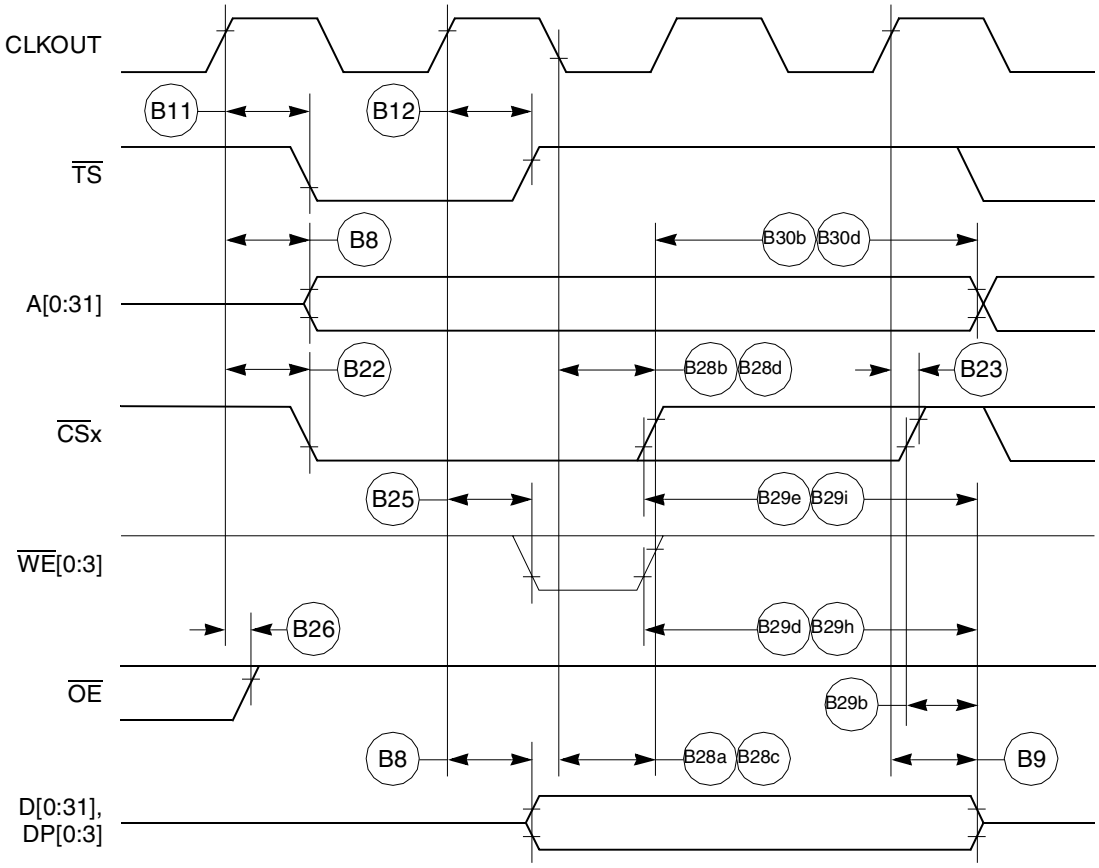

Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

Figure 17 provides the timing for the external bus controlled by the UPM.

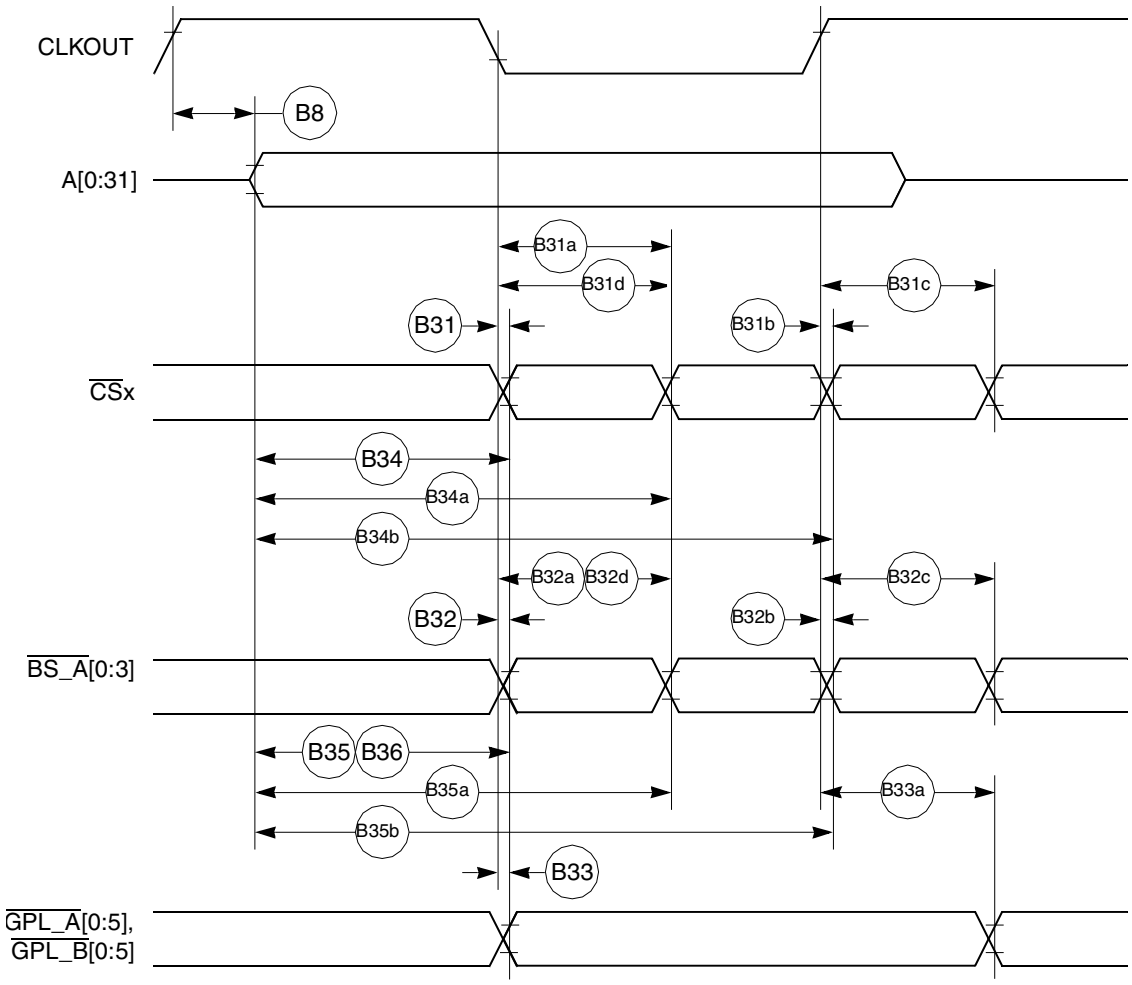

Figure 17. External Bus Timing (UPM-Controlled Signals)

Figure 25 provides the PCMCIA access cycle timing for the external bus read.

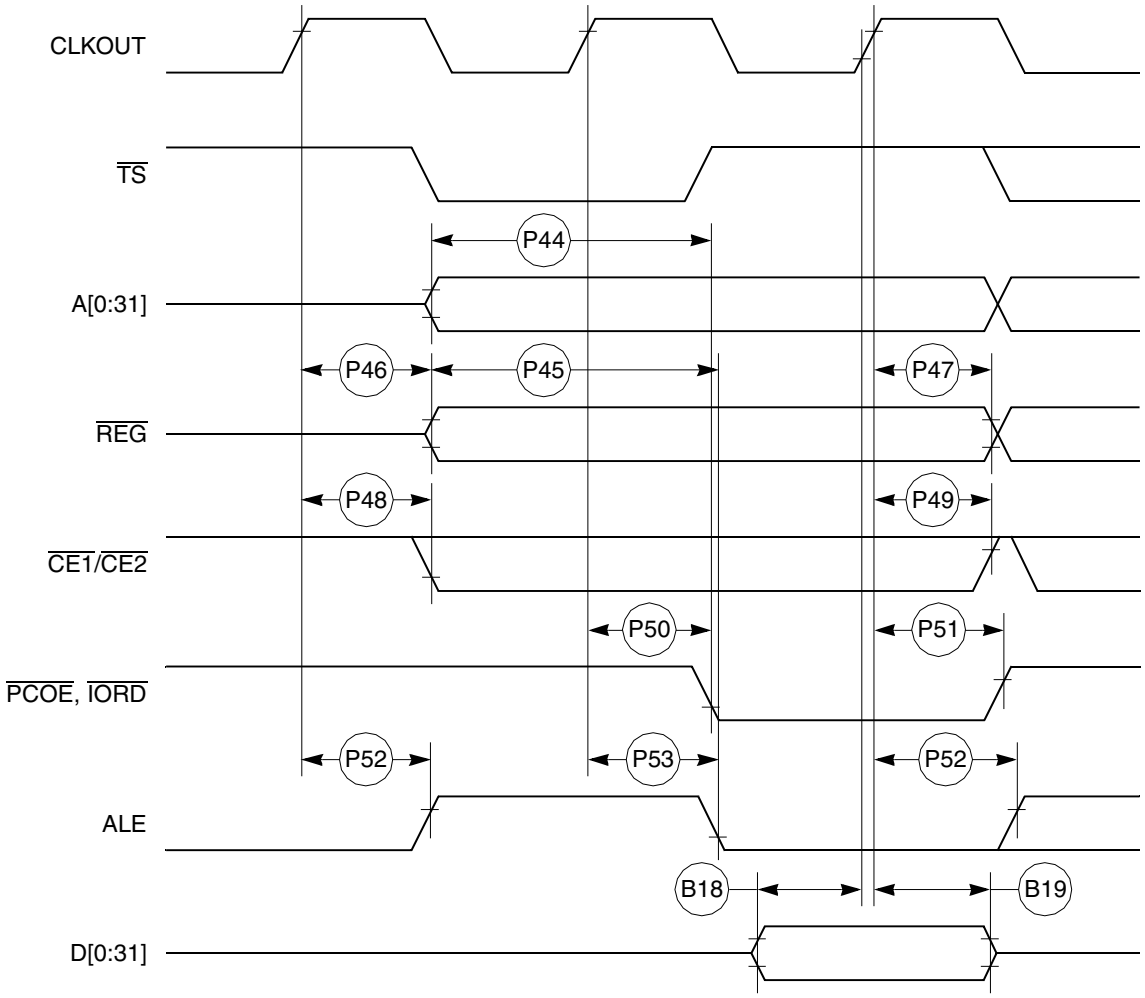

Figure 25. PCMCIA Access Cycles Timing External Bus Read

Figure 26 provides the PCMCIA access cycle timing for the external bus write.

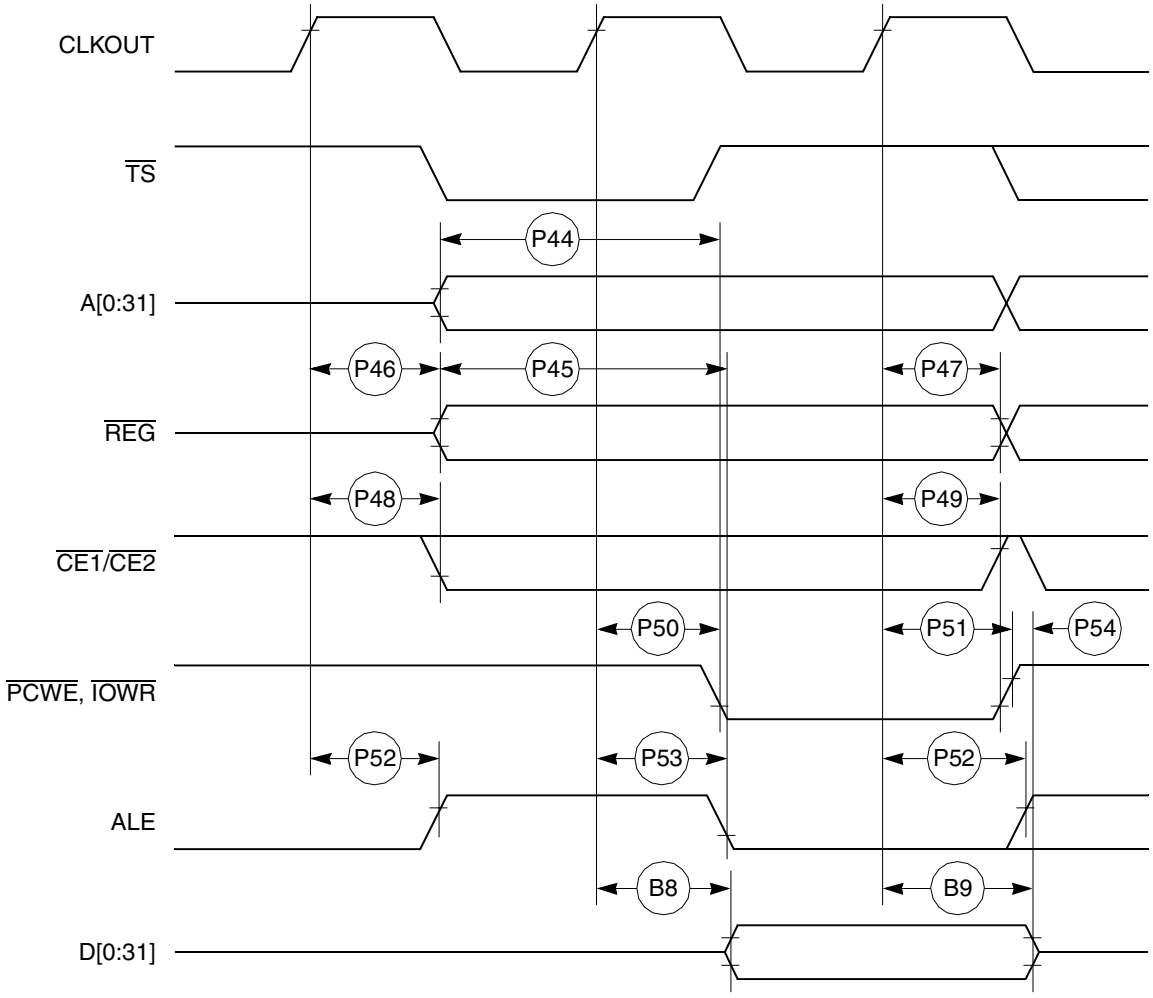

Figure 26. PCMCIA Access Cycles Timing External Bus Write

Figure 27 provides the PCMCIA WAIT signals detection timing.

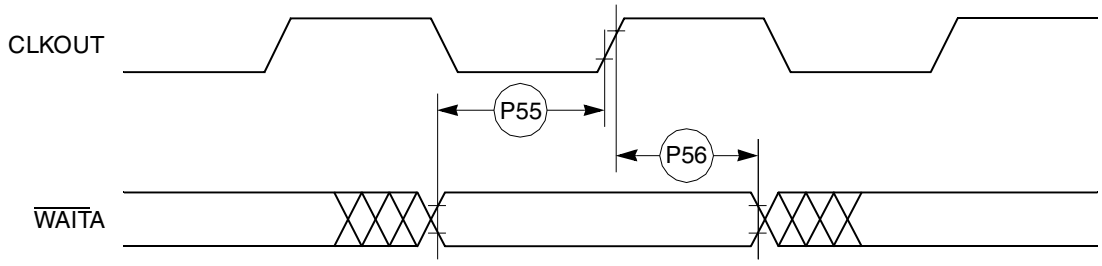

Figure 27. PCMCIA WAIT Signals Detection Timing

Table 14 shows the reset timing for the MPC853T.

Table 14. Reset Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
J82	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
J83	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
J84	$\overline{\text{RSTCONF}}$ pulse width (MIN = 17.00 × B1)	515.20	—	425.00	—	340.00	—	257.60	—	ns
J85	—	—	—	—	—	—	—	—	—	—
J86	Configuration data to HRESET rising edge setup time (MIN = 15.00 × B1 + 50.00)	504.50	—	425.00	—	350.00	—	277.30	—	ns
J87	Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time (MIN = 0.00 × B1 + 350.00)	350.00	—	350.00	—	350.00	—	350.00	—	ns
J88	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
J89	Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
J90	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
J91	$\overline{\text{RSTCONF}}$ negated to data out high impedance (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
J92	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
J93	DSDI, DSCK setup (MIN = 3.00 × B1)	90.90	—	75.00	—	60.00	—	45.50	—	ns
J94	DSDI, DSCK hold time (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
J95	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 × B1)	242.40	—	200.00	—	160.00	—	121.20	—	ns

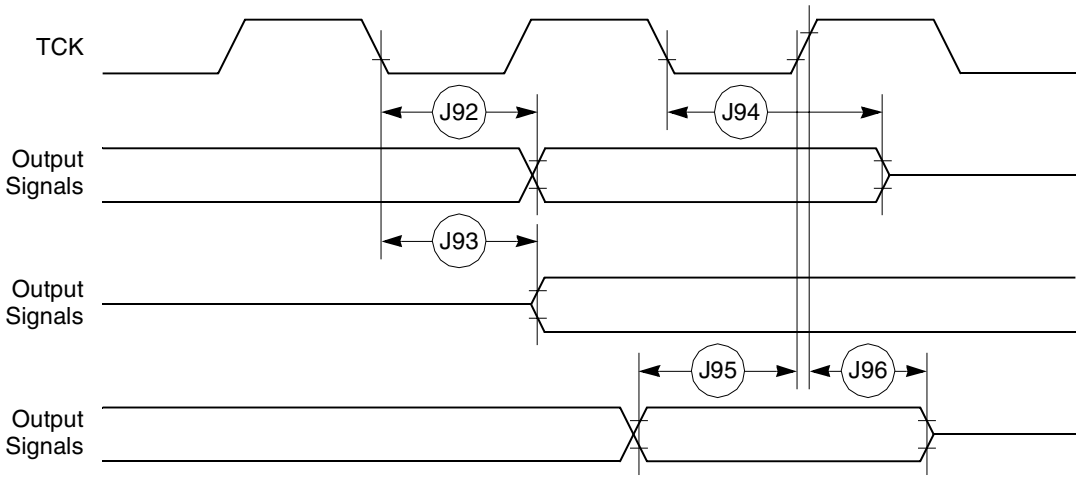

Figure 38. Boundary Scan (JTAG) Timing Diagram

13 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC853T.

13.1 Port C Interrupt AC Electrical Specifications

Table 16 provides the timings for port C interrupts.

Table 16. Port C Interrupt Timing

Num	Characteristic	33.34 MHz		Unit
		Min	Max	
35	Port C interrupt pulse width low (edge-triggered mode)	55	—	ns
36	Port C interrupt minimum time between active edges	55	—	ns

Figure 39 shows the port C interrupt detection timing.

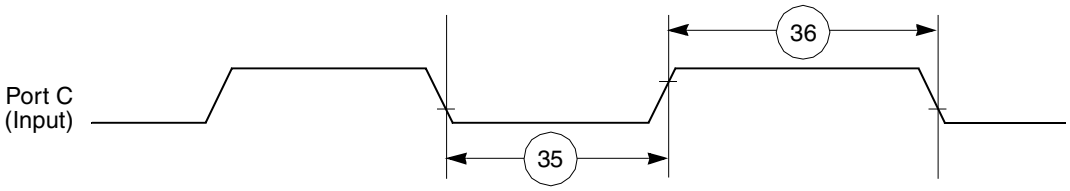

Figure 39. Port C Interrupt Detection Timing

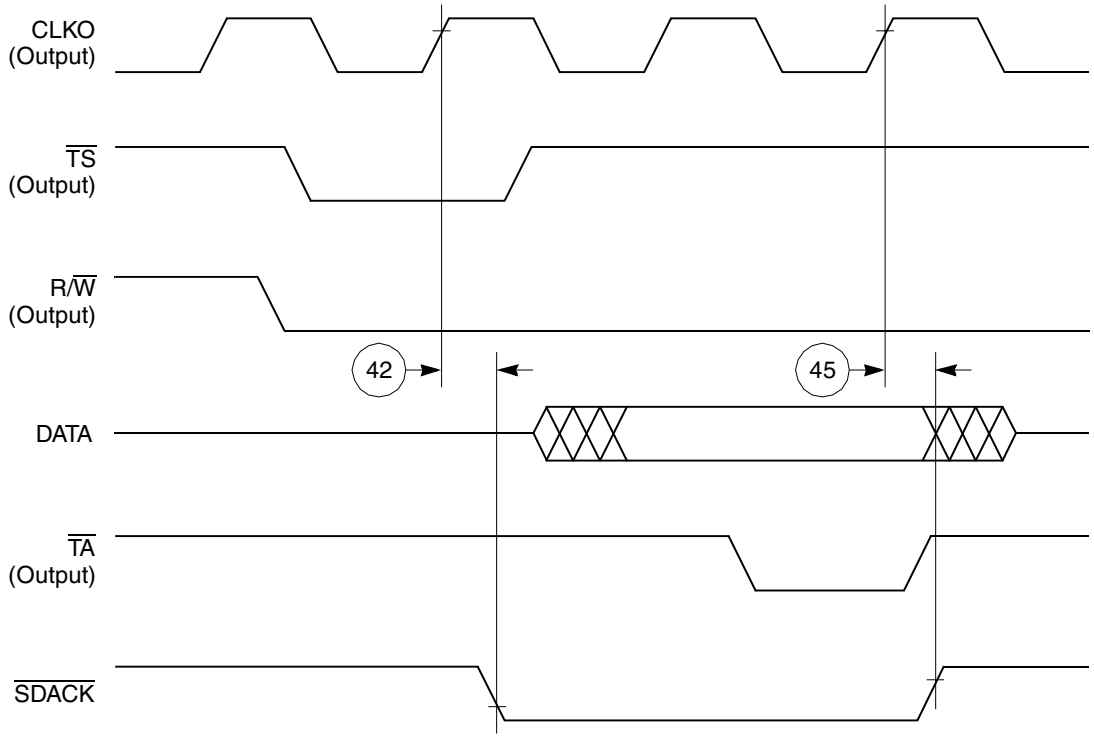

Figure 43. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA

13.3 Baud-Rate Generator AC Electrical Specifications

Table 18 provides the baud-rate generator timings as shown in Figure 44.

Table 18. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

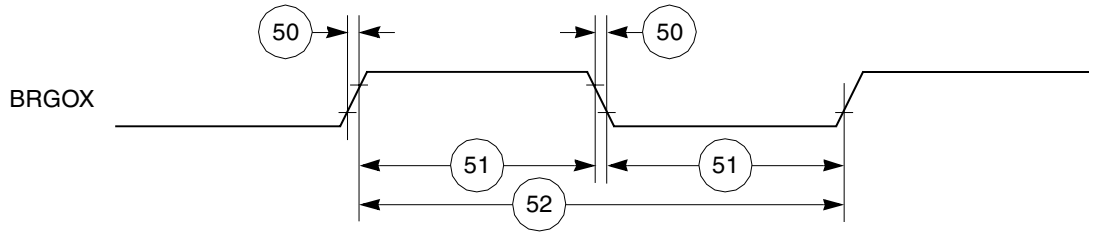

Figure 44. Baud Rate Generator Timing Diagram

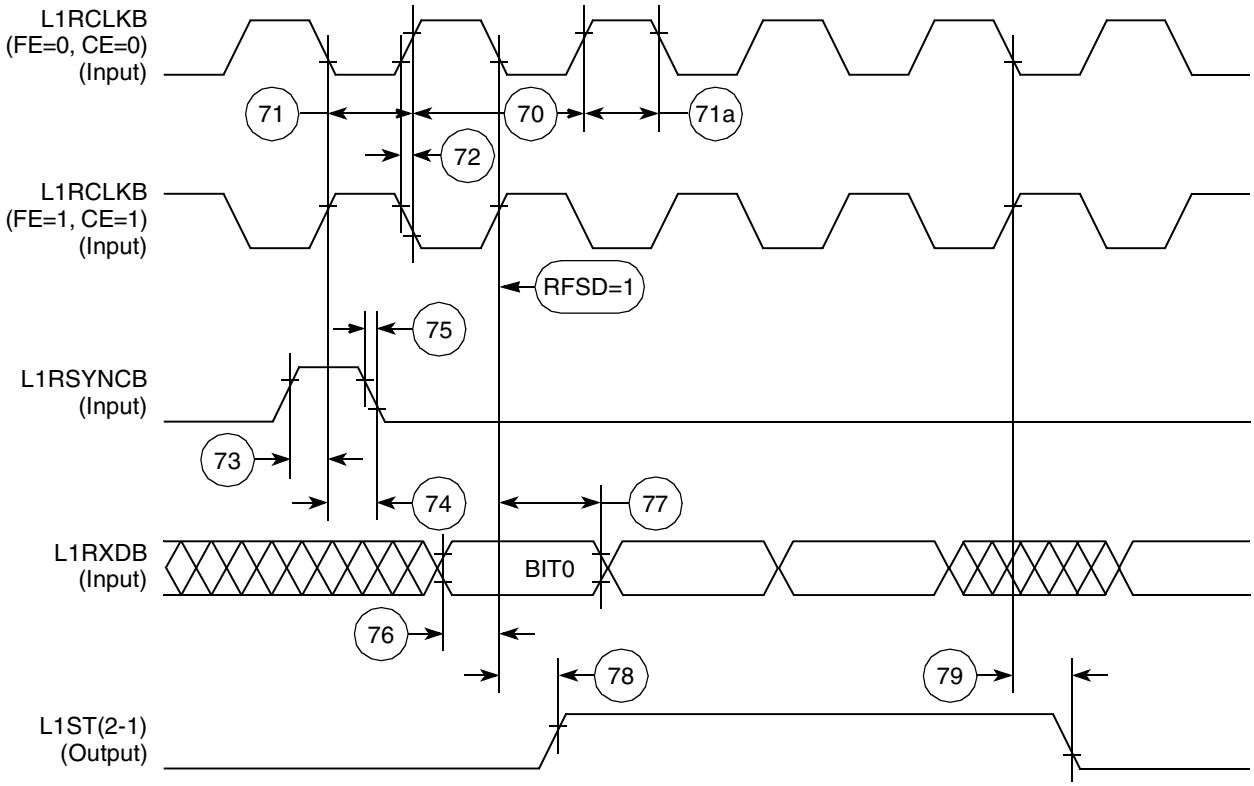

Figure 46. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

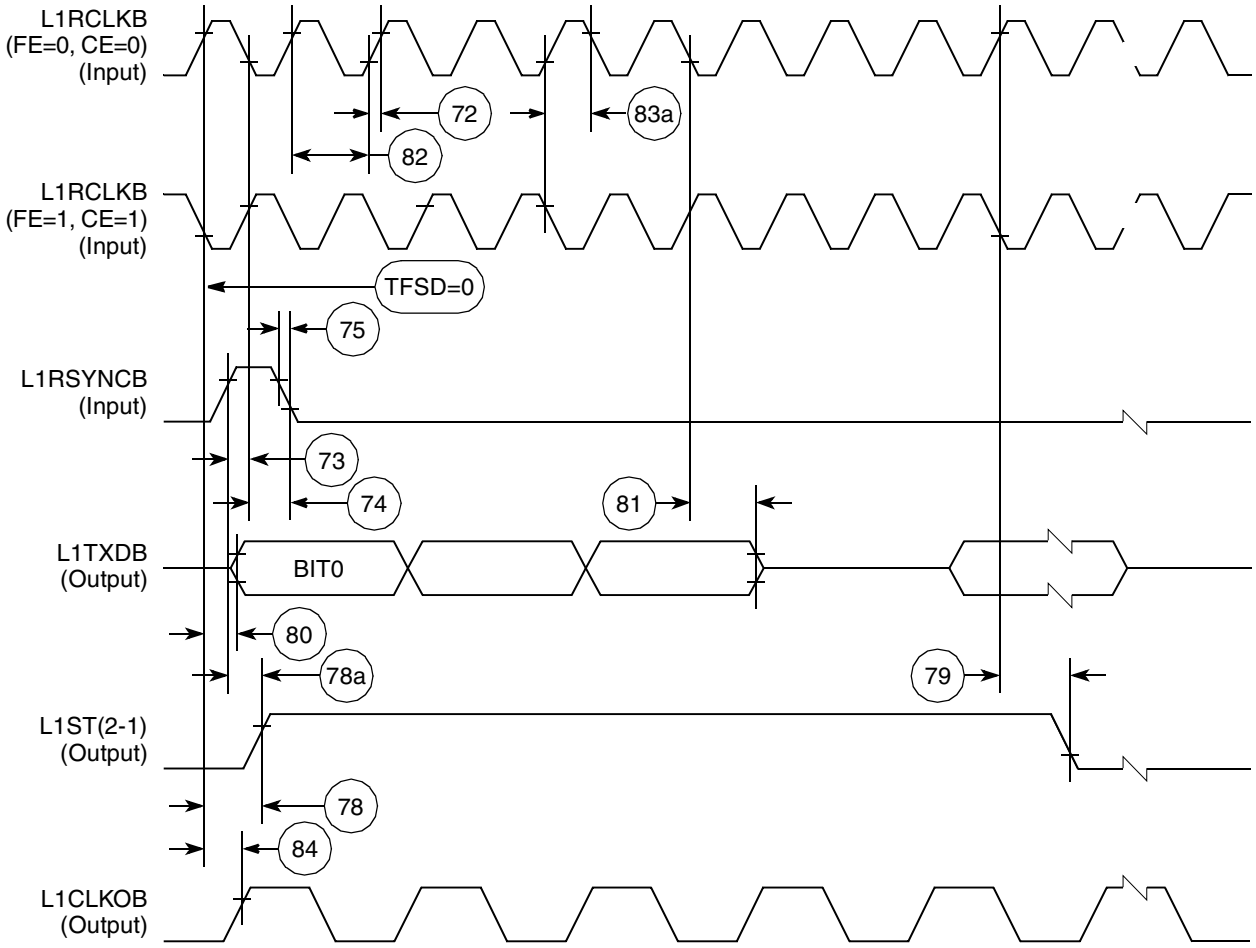

Figure 49. SI Transmit Timing with Double Speed Clocking (DSC = 1)

13.6 SCC in NMSI Mode Electrical Specifications

Table 21 provides the NMSI external clock timing.

Table 21. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK3 and TCLK3 width high [1]	1/SYNCCLK	—	ns
101	RCLK3 and TCLK3 width low	1/SYNCCLK +5	—	ns
102	RCLK3 and TCLK3 rise/fall time	—	15.00	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS3}}$ active/inactive delay (from TCLK3 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS3}}$ setup time to TCLK3 rising edge	5.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	5.00	—	ns
107	RXD3 hold time from RCLK3 rising edge [2]	5.00	—	ns
108	$\overline{\text{CD3}}$ setup Time to RCLK3 rising edge	5.00	—	ns

1 The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater than or equal to 2.25/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Table 22 provides the NMSI internal clock timing.

Table 22. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK3 and TCLK3 frequency [1]	0.00	SYNCCLK/3	MHz
102	RCLK3 and TCLK3 rise/fall time	—	—	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS3}}$ active/inactive delay (from TCLK3 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS3}}$ setup time to TCLK3 rising edge	40.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	40.00	—	ns
107	RXD3 hold time from RCLK3 rising edge [2]	0.00	—	ns
108	$\overline{\text{CD3}}$ setup time to RCLK3 rising edge	40.00	—	ns

1 The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater than or equal to 3/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Figure 63 shows MII receive signal timing.

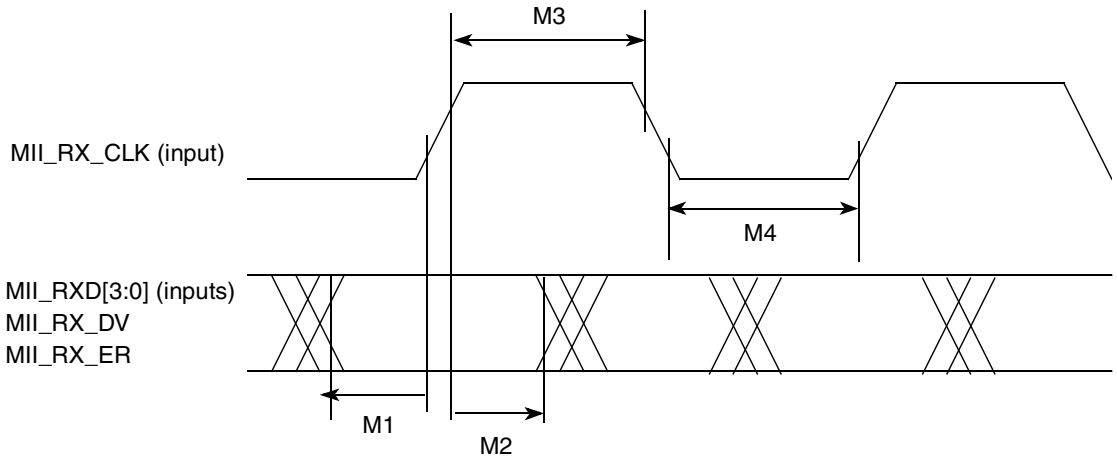

Figure 63. MII Receive Signal Timing Diagram

14.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency – 1%.

Table 27 provides information on the MII transmit signal timing.

Table 27. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	
M7	MII_TX_CLK pulse width high	35%	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period

Figure 64 shows the MII transmit signal timing diagram.

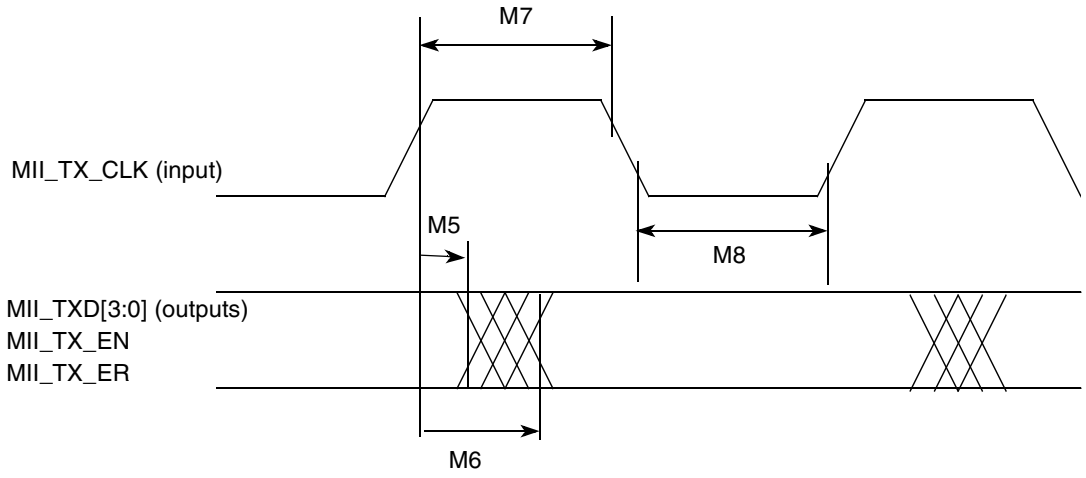

Figure 64. MII Transmit Signal Timing Diagram

14.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 28 provides information on the MII async inputs signal timing.

Table 28. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 65 shows the MII asynchronous inputs signal timing diagram.

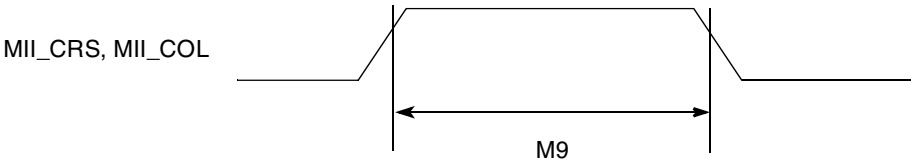

Figure 65. MII Async Inputs Timing Diagram

14.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 29 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Table 29. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns

Table 29. MII Serial Management Channel Timing (continued)

Num	Characteristic	Min	Max	Unit
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

Figure 66 shows the MII serial management channel timing diagram.

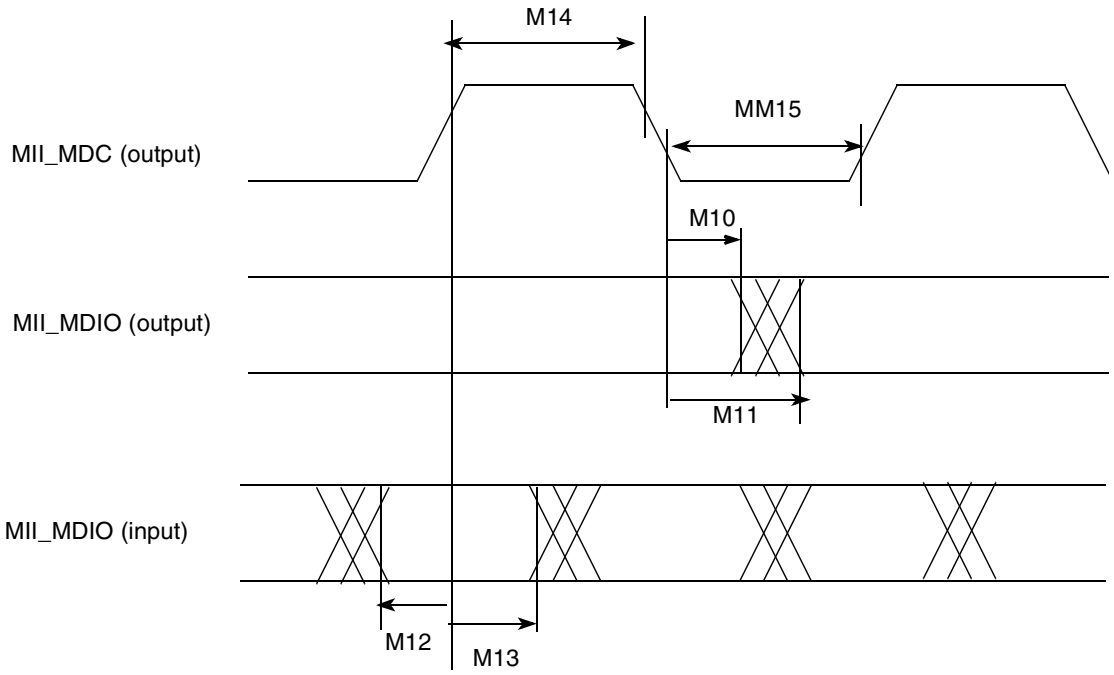

Figure 66. MII Serial Management Channel Timing Diagram

Table 31. Pin Assignments - JEDEC Standard (continued)

Name	Pin Number	Type
PC12 $\overline{\text{RTS4}}$ L1ST4	E15	Bidirectional (5V tolerant)
PC7 L1TSYNCB $\overline{\text{CTS3}}$	J14	Bidirectional (5V tolerant)
PC6 L1RSYNCB $\overline{\text{CD3}}$	K15	Bidirectional (5V tolerant)
PC5 $\overline{\text{CTS4}}$ SDACK1	J13	Bidirectional (5V tolerant)
PC4 $\overline{\text{CD4}}$	L14	Bidirectional (5V tolerant)
PD15 MII-RXD3	M14	Bidirectional (5V tolerant)
PD14 MII-RXD2	N16	Bidirectional (5V tolerant)
PD13 MII-RXD1	K13	Bidirectional (5V tolerant)
PD12 MII-MDC	N15	Bidirectional (5V tolerant)
PD11 RXD3 MII-TXERR	P16	Bidirectional (5V tolerant)
PD10 TXD3 MII-RXD0	R15	Bidirectional (5V tolerant)
PD9 RXD4 MII-TXD0	N14	Bidirectional (5V tolerant)
PD8 TXD4 MII_RX_CLK	M13	Bidirectional (5V tolerant)
PD7 $\overline{\text{RTS3}}$ MII_RX_ER	T15	Bidirectional (5V tolerant)
PD6 $\overline{\text{RTS4}}$ MII_RX_DV	N13	Bidirectional (5V tolerant)

Table 32. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
GND	H7, H8, H9, H10, H11, H12, J7, J8, J9, J10, J11, J12, K7, K8, K9, K10, K11, K12, L7, L8, L9, L10, L11, L12	Power
V_{DDL}	B8, D2, E17, H16, M5, N3, T2, N16, U9	Power
V_{DDH}	G6, G7, G8, G9, G10, G11, G12, G13, H6, H13, J6, J13, K6, K13, L6, L13, M6, M7, M8, M9, M10, M11, M12, M13	Power
N/C	B2, B17, C17, D16, E15, F13, M14, N5, R16, T17, U2, U17	No-connect