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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	CPU32
Core Size	32-Bit Single-Core
Speed	20.97MHz
Connectivity	EBI/EMI, SCI, SPI, UART/USART
Peripherals	WDT
Number of I/O	48
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	132-BCQFP
Supplier Device Package	132-CERQUAD (22.36x22.36)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts68332va20a

Signal Description

Figure 1 illustrates the functional signal groups and Table 1 lists the signals and their function.

Table 1. Signal Index

Signal Name	Mnemonic	Function
Address Bus	A23 - A0	24-bit address bus
Data Bus	D15 - D0	16-bit data bus used to transfer byte or word data per bus cycle
Data Bus Function Codes	FC2 - FC0	Identify the processor state and the address space of the current bus cycle
Boot Chip Select	$\overline{\text{CSBOOT}}$	Chip-select boot stat up ROM containing user's reset vector and initialization program
Chip Selects	$\overline{\text{CS10}}$ - $\overline{\text{CSO}}$	Enables peripherals at programmed addresses
Bus Request	$\overline{\text{BR}}$	Indicates that an external device requires bus mastership
Bus Grant	$\overline{\text{BG}}$	Indicates that current bus cycle is complete and the TS68332 has relinquished the bus
Bus Grant Acknowledge	$\overline{\text{BGACK}}$	Indicates that an external device has assumed bus mastership
Data and Size Acknowledgement	$\overline{\text{DSACK1}}$, $\overline{\text{DSACK0}}$	Provides asynchronous data transfers and dynamic bus sizing
Autovector	$\overline{\text{AVEC}}$	Requests an automatic vector during an interrupt acknowledge cycle
Read-Modify-Write Cycle	$\overline{\text{RMC}}$	Identifies the bus cycle as part of an indivisible read-modify-write cycle
Address Strobe	$\overline{\text{AS}}$	Indicates that a valid address is on the address bus
Data Strobe	$\overline{\text{DS}}$	During a read cycle, DS indicates that an external device should place valid data on the data bus. During a write cycle, DS indicates that valid data is on the data bus.
Size	SIZ1 - SIZ0	Indicates the number of bytes remaining to be transferred for this cycle
Read/Write	R/$\overline{\text{W}}$	Indicates the direction of data transfer on the bus
Interrupt Request Level	$\overline{\text{IRQ7}}$ - $\overline{\text{IRQ0}}$	Provides an interrupt priority level to the CPU
Reset	$\overline{\text{RESET}}$	System reset
Halt	$\overline{\text{HALT}}$	Suspend external bus activity
Bus Error	$\overline{\text{BERR}}$	Indicates that an erroneous bus operation is being attempted
System Clockout	CLKOUT	Internal system clock
Crystal Oscillator	EXTAL, XTAL	Connection for an external crystal to the internal oscillator circuit
External Filter Capacitor	XFC	Connection pin for an external capacitor to filter the circuit of the phase-locked loop
Clock Mode Select	MODCK	Selects the source of the internal system clock
Instruction Fetch	$\overline{\text{IFETCH}}$	Indicates when the CPU is performing an instruction word pre-fetch and when the instruction pipeline has been flushed
Instruction Pipe	$\overline{\text{IPIPE}}$	Used to track movement of words through the instruction pipeline
Breakpoint	$\overline{\text{BKPT}}$	Signals a hardware breakpoint to the CPU
Freeze	FREEZE	Indicates that the CPU has acknowledged a breakpoint
Quotient Out	QUOT	Serial I/O and clock for background debug mode
Test Mode Enable	$\overline{\text{TSTME}}$	Hardware enable for test mode
Three-State Control	TSC	Places all output drivers in a high-impedance state

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{DD}	Supply Voltage		-0.3	+7.0	V
V_I	Input Voltage		-0.3	+7.0	V
P_{DMAX}	Max Power Dissipation	Low Power Operation		600	mW
		Stand By Mode		500	mW
T_{case}	Operating Temperature	M Suffix	-55	+125	°C
		V Suffix	-40	+85	°C
T_{stg}	Storage Temperature		-55	+150	°C
T_{leads}	Lead Temperature	Max 5 Sec. Soldering		+270	°C

Table 3. Thermal Characteristics (at 25°C)

Package	Symbol	Parameter	Value	Unit
PGA 132	θ_{J-A}	Thermal Resistance Ceramic Junction-to-ambient	TBD	°C/W
	θ_{J-C}	Thermal Resistance Ceramic Junction-to-case	10	°C/W
CERQUAD 132	θ_{J-A}	Thermal Resistance Ceramic Junction-to-ambient	TBD	°C/W
	θ_{J-C}	Thermal Resistance Ceramic Junction-to-case	10	°C/W

Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \cdot V_{CC}$, Watts - Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins - User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Static Characteristics

Table 4. DC Characteristics. V_{DD} and V_{DDSYN} = 5.0V_{DC} ± 10% for 16.78 MHz and 5.0V_{DC} ± 5% for 20.97 MHz; V_{SS} = 0V_{DC}; T_C = -55°C to +125°C or -40°C to +85°C

Number	Symbol	Parameter		16.78 MHz		20.97 MHz		Unit
				Min	Max	Min	Max	
1	V_{IH}	Input High Voltage		0.7 (V_{DD})	V_{DD}+0.3	0.7(V_{DD})	V_{DD}+0.3	V
2	V_{IL}	Input Low Voltage		V_{SS} - 0.3	0.2(V_{DD})	V_{SS} - 0.3	0.2(V_{DD})	V
3	V_{HYS}	Input Hysteresis(1)		0.5	-	0.5	-	V
4	I_{IN}	Input Leakage Current(2) V_{IN} = V_{DD} or V_{SS}	Input-only pins	- 2.5	2.5	- 2.5	2.5	µA
5	I_{OZ}	High Impedance (off-state) Leakage Current (2) V_{IN} = V_{DD} or $V_{SS\,L}$	All input/output and output pins	- 2.5	2.5	- 2.5	2.5	µA
6	V_{OH}	CMOS Output High Voltage(2)(3) I_{OH} = -10.0 µA	Group 1, 2, 4 input/output and all output pins and all output pins	V_{DD} - 0.2	-	V_{DD} - 0.2	-	V
7	V_{OL}	CMOS Output High Voltage(2) I_{OH} = -10.0 µA	Group 1, 2, 4 input/output and all output pins	-	0.2	-	0.2	V
8	V_{OH}	Output High Voltage(2)(3) I_{OH} = -0.8 mA	Group 1, 2, 4 input/output and all output pins	V_{DD} - 0.8	-	V_{DD} - 0.8	-	V
9	V_{OL}	Output Low Voltage(2) I_{OL} = 1.6 mA	Group 1 I/O pins CLKOUT, FREEZE/QUOT, $\overline{\text{IPIPE}}$	-	0.4	-	0.4	V
		I_{OL} = 5.3 mA	Group 2, 4 I/O pins, $\overline{\text{CSBOOT}}$, $\overline{\text{BG}}$/$\overline{\text{CS}}$	-	0.4	-	0.4	V
		I_{OL} = 12 mA	Group 3	-	0.4	-	0.4	V
10	V_{IHTSC}	Three State Control Input High Voltage		1.6(V_{DD})	9.1	1.6(V_{DD})	9.1	V
11	I_{MSP}	Data Bus Mode Select Pull-up Current(5)						
		V_{IN} = V_{IL}	DATA [15:0]	-	-120	-	-120	µA
		V_{IN} = V_{IH}	DATA [15:0]	-15	-	- 15	-	µA
12		V_{DD} supply current(5)						
	I_{DD}	RUN(6)		-	124	-	140	mA
	I_{DD}	RUN, TPU emulation mode		-	134	-	150	mA
	S_{IDD}	LPSTOP, 32.768 kHz crystal, VCO off (STSIM = 0)		-	350	-	350	µA
	S_{IDD}	LPSTOP (external clock input frequency = maximum f_{sys})		-	5	-	5	mA

Test Conditions Specific to the Device

Time Definitions

The times specified in Table 6 as dynamic characteristics are defined in Figure 4 to Figure 15 below, by a reference number given the column “NUM” of the tables together with the relevant figure number.

Figure 4. Clkout Output Timing Diagram

Note: Timing shown with respect to 20% and 70% V_{DD}.

Figure 5. External Input Timing Diagram

Note: Timing shown with respect to 20% and 70% V_{DD}. Pulse width shown with respect to 50% $V_{DD.}$

Figure 6. ECLK Output Timing Diagram

Note: Timing Shown With Respect To 20% And 7% V_{DD}.

Figure 19. Supervisor Programming Model Supplement

Data Types

Six basic data types are supported:

- bits
- packaged binary-coded decimal digits
- byte integers (8 bits)
- word integers (16 bits)
- long-word integers (32 bits)
- quad-word integers (64 bits)

Organization In Registers

The eight data registers can store data operands of 1, 8, 16, 32 and 64 bits and addresses of 16 or 32 bits. The seven address registers and the two stack pointers are used for address operands of 16 or 32 bits. The PC is 32 bits wide.

System Features

The CPU32 includes a number of features to aid system implementation. These include a privilege mechanism, separation of address spaces, multilevel priority interrupts, trap instructions, and a trace facility.

The privilege mechanism provides user and supervisor privilege states, privileged instructions, and external distinction of user and supervisor state references. The processor separates references between program and data space. This permits sharing of code segments that access separate data segments.

The CPU32 supports seven priority levels for 199 memory vectored interrupts. For each interrupt, the vector location can be provided externally or generated internally. The seventh level provides a non-maskable interrupt capability.

To simplify system development, instructions are provided to check internal processor conditions and allow software traps. The trace facility allows instruction-by-instruction tracing of program execution without alteration of the program or special hardware.

Virtual Memory

The full addressing range of the CPU32 on the TS68332 is 16-Mbyte in each of eight address spaces. Even though most systems implement a smaller physical memory, the system can be made to appear to have a full 16-Mbyte of memory available to each user program by using virtual memory techniques.

Instructions

68000 Family Compatibility

It is the philosophy of the 68000 family that all user-code programs can execute unchanged on a more advanced processor, and supervisor-mode programs and exception handlers should require only minimal alteration.

The CPU32 can be thought of as an intermediate member of the 68000 family. Object code from an TS68000 or 68010 may be executed on the CPU32, and many of the instruction and addressing mode extensions of the TS68020 are also supported. Refer to the CPU32 reference manual for a detailed comparison of the CPU32 and TS68020 instruction set (see also Table 7).

New Instructions

Two new instructions have been added to the TS68000 instruction set for use in controller applications. They are low power stop (LPSTOP) and table lookup and interpolate (TBL).

Low Power Stop (LPSTOP): In applications where power consumption is a consideration, the CPU32 forces the device into a low-power standby mode when immediate processing is not required. The low-power stop mode is entered by executing the LPSTOP instruction.

The processor will remain in this mode until a user-specification (or higher) interrupt level or reset occurs.

Table Lookup and Interpolate (TBL): To maximize throughput for real-time applications, reference data is often “pre-calculated” and stored in memory for quick access. The storage of each data point would require an inordinate amount of memory. The table instruction requires only a sample of data points stored in the array, reducing memory requirements. This single instruction allows intermediate values to be recovered by linear interpolation, thus significantly increasing CPU throughput compared with earlier interpolation methods which used several instructions. The results are optionally rounded with the round-to-nearest algorithm.

Development Support

The following features have been implemented on the CPU32 to enhance the instrumentation and development environment:

- 68000 family development support,
- background debug mode,
- deterministic opcode tracking,
- hardware breakpoints.

68000 Family Development Support

All 68000 family members include features to facilitate applications development. These features include the following:

Trace On Instruction: 68000 family processors include an instruction-by-instruction tracing facility as an aid to program development. The CPU32 also allows the user to trace only those instructions causing a change in program flow.

Breakpoint Instruction: An emulator may insert software breakpoints into the target code to indicate when a breakpoint has occurred. On the CPU32, this function is provided via illegal instructions, $4848-$484F, to serve as breakpoint instructions.

Unimplemented Instruction Emulation: During instruction execution, when an attempt is made to execute an illegal instruction, an illegal instruction exception occurs. Unimplemented instructions (F-line, A-line,...) utilize separate exception vectors to permit efficient emulation of unimplemented instructions in software.

Background Debug Mode

Microcomputer systems generally provide a debugger, implemented in software, for system analysis at the lowest level. The background debug mode in the CPU32 is unique in that the debugger has been implemented in CPU microcode. Registers can be viewed and/or altered, memory can be read or written to, and test features can be invoked. Incorporating these capabilities on-chip simplifies the environment in which the in-circuit emulator operates.

Deterministic Opcode Tracking

CPU 32 function code outputs are augmented by two supplementary signals to monitor the instruction pipeline. The instruction pipe (PIPE) output indicates the start of each new instruction and each mid-instruction pipeline advance. The instruction fetch (FETCH) output identifies the bus cycles in which the operand is loaded into the instruction pipeline. Pipeline flushes are also signaled with IFETCH. Monitoring these two signals allows a bus analyzer to synchronize itself to the instruction stream and monitor its activity.

On-chip Breakpoint Hardware

An external breakpoint trap on any memory access.

Table 7. Instruction Set Summary

Mnemonic	Description
ABCD	Add Decimal with Extend
ADD	Add
ADDA	Add Address
ADDI	Add Immediate
ADDQ	Add Quick
ADDX	Add with Extend
AND	Logical AND
ANDI	Logical AND Immediate
ASL, ASR	Arithmetic Shift Left and Right
Bcc	Branch Conditionally
BCHG	Test Bit and Change
BCLR	Test Bit and Clear
BGND	Background
BKPT	Breakpoint
BRA	Branch
BSET	Test Bit and Set
BSR	Branch to Subroutine
BTST	Test Bit
CHK, CHK2	Check Register Against Upper and Lower Bounds
CLR	Clear
CMP	Compare
CMPA	Compare Address
CMPI	Compare Immediate
CMPM	Compare Memory to Memory
CMP2	Compare Register Against Upper and Lower Bounds
DBcc	Test Condition, Decrement and Branch
DIVS, DIVSL	Signed Divide
DIVU, DIVUL	Unsigned Divide

EOR	Logical Exclusive OR
EORI	Logical Exclusive OR Immediate
EXG	Exchange Registers
EXT, EXTB	Sign Extend
ILLEGAL	Take Illegal Instruction Trap
JMP	Jump
JSR	Jump to Subroutine
LEA	Load Effective Address
LINK	Link and Allocate
LPSTOP	Low Power Stop
LSL, LSR	Logical Shift Left and Right
MOVE	Move
MOVE CCR	Move Condition Code Register
MOVE SR	Move Status Register
MOVE USP	Move User Stack Pointer
MOVEA	Move Address
MOVEC	Move Control Register
MOVEM	Move Multiple Registers
MOVEP	Move Peripheral
MOVEQ	Move Quick
MOVES	Move Alternate Addree Space
MULS, MULS.L	Signed Multiply
MULU, MULU.L	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Negate
NEGX	Negate with Extend
NOP	No Operation
OR	Logical Inclusive OR
ORI	Logical Inclusive OR Immediate
PEA	Push Effective Address
RESET	Reset External Devices
ROL, ROR	Rotate Left and Right
ROXL, ROXR	Rotate with Extend Left and Right
RTD	Return and De-allocate
RTE	Return from Exception
RTR	Return and Restore Codes
RTS	Return from Subroutine

Figure 22. Clock Submodule Block Diagram

Note: Must be low leakage capacitor.

Clock Synthesizer

The clock synthesizer (Figure 22) can operate from an on-chip phase locked loop (PLL) using an external crystal connected between the EXTAL and XTAL pins as a reference frequency source. A 32.768 kHz watch crystal provides an inexpensive reference, but the reference crystal frequency can be any frequency from 25 - 50 kHz. Outside the 25 - 50 kHz range, an external oscillator can be used with the on-chip synthesizer and VCO, or the frequency can be driven directly into the EXTAL pin (the XTAL pin should be left floating for this case).

The system clock frequency is programmable from 131 kHz to the maximum clock frequency with a resolution of 131 kHz. A separate power pin (V_{DDSYN}) is used to allow the clock circuits to run with the rest of the MCU powered down and to provide increased noise immunity for the clock circuits. If for some reason the external signal is removed from the device then the clock synthesizer will generate its own internal clock signal to allow the device to enter some kind of error recovery routine. This is known as LIMP mode. The clock frequency generated will not have an associated timing spec but should be around 9 MHz.

Chip-select Submodule

Typical microcomputer systems require external hardware to provide select signals to external peripherals. This MCU integrates these functions on-chip in order to provide the cost, speed, and reliability benefits of a higher level of integration. The chip-select signals can also be programmed as output enable, read or write strobe, or IACK signals.

Since initialization software would probably reside in a peripheral memory device controlled by the chip-select circuits, a CSBOOT register provides default reset values to support bootstrap operation.

The chip-select submodule supports the following programmable features: