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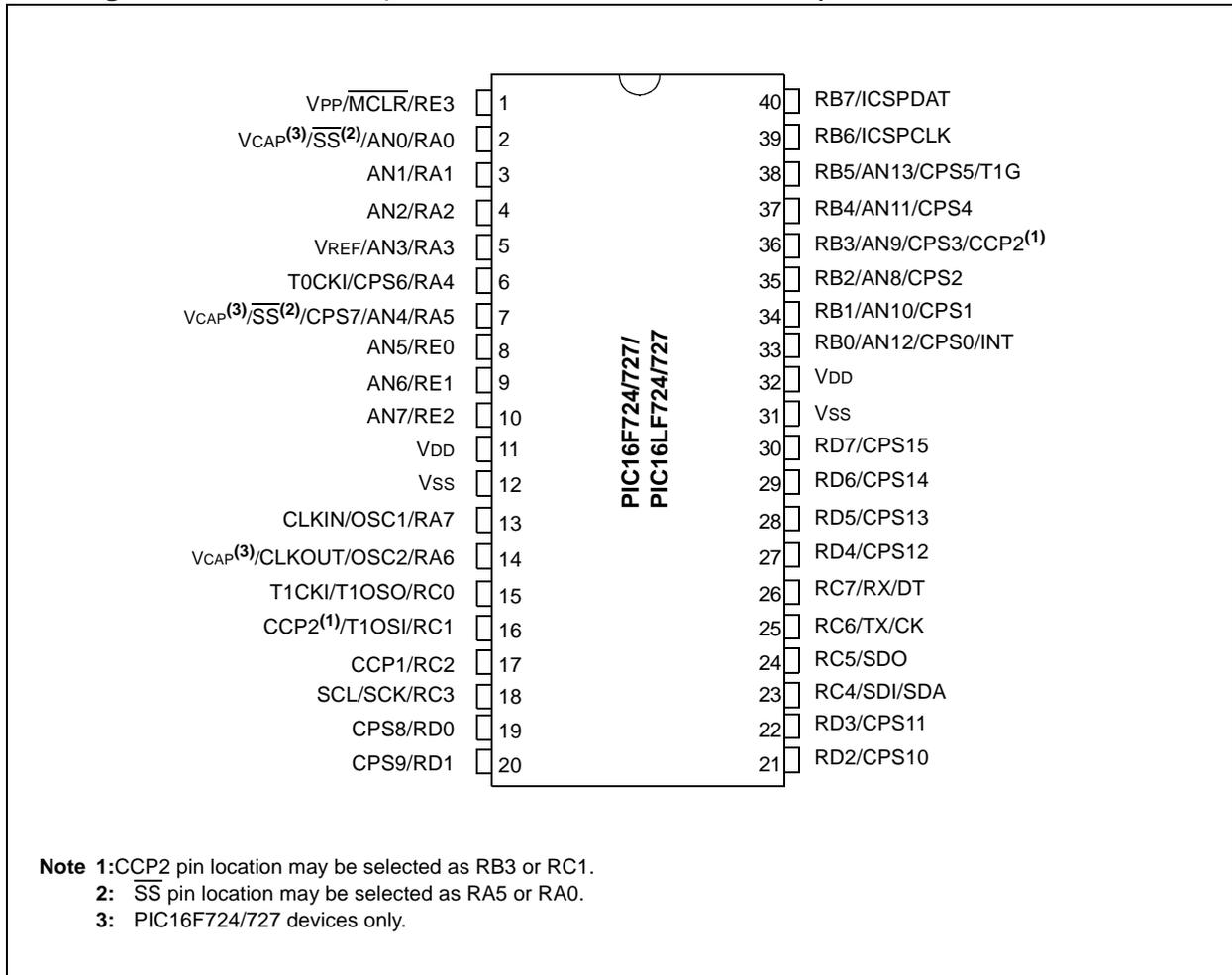
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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f722-e-ss

PIC16(L)F722/3/4/6/7

Pin Diagrams – 40-PIN PDIP (PIC16F724/727/PIC16LF724/727)



PIC16(L)F722/3/4/6/7

TABLE 1-1: PIC16(L)F722/3/4/6/7 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/ \overline{SS} /VCAP	RA0	TTL	CMOS	General purpose I/O.
	AN0	AN	—	A/D Channel 0 input.
	\overline{SS}	ST	—	Slave Select input.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F72X only).
RA1/AN1	RA1	TTL	CMOS	General purpose I/O.
	AN1	AN	—	A/D Channel 1 input.
RA2/AN2	RA2	TTL	CMOS	General purpose I/O.
	AN2	AN	—	A/D Channel 2 input.
RA3/AN3/VREF	RA3	TTL	CMOS	General purpose I/O.
	AN3	AN	—	A/D Channel 3 input.
	VREF	AN	—	A/D Voltage Reference input.
RA4/CPS6/T0CKI	RA4	TTL	CMOS	General purpose I/O.
	CPS6	AN	—	Capacitive sensing input 6.
	T0CKI	ST	—	Timer0 clock input.
RA5/AN4/CPS7/ \overline{SS} /VCAP	RA5	TTL	CMOS	General purpose I/O.
	AN4	AN	—	A/D Channel 4 input.
	CPS7	AN	—	Capacitive sensing input 7.
	\overline{SS}	ST	—	Slave Select input.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F72X only).
RA6/OSC2/CLKOUT/VCAP	RA6	TTL	CMOS	General purpose I/O.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	Fosc/4 output.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F72X only).
RA7/OSC1/CLKIN	RA7	TTL	CMOS	General purpose I/O.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	CMOS	—	External clock input (EC mode).
	CLKIN	ST	—	RC oscillator connection (RC mode).
RB0/AN12/CPS0/INT	RB0	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN12	AN	—	A/D Channel 12 input.
	CPS0	AN	—	Capacitive sensing input 0.
	INT	ST	—	External interrupt.
RB1/AN10/CPS1	RB1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN10	AN	—	A/D Channel 10 input.
	CPS1	AN	—	Capacitive sensing input 1.
RB2/AN8/CPS2	RB2	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN8	AN	—	A/D Channel 8 input.
	CPS2	AN	—	Capacitive sensing input 2.
RB3/AN9/CPS3/CCP2	RB3	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN9	AN	—	A/D Channel 9 input.
	CPS3	AN	—	Capacitive sensing input 3.
	CCP2	ST	CMOS	Capture/Compare/PWM2.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C = Schmitt Trigger input with I²C
HV = High Voltage XTAL = Crystal levels

PIC16(L)F722/3/4/6/7

TABLE 2-1: PIC16(L)F722/3/4/6/7 SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Page
Bank 0											
00h ⁽²⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	29,37
01h	TMR0	Timer0 Module Register								xxxx xxxx	105,37
02h ⁽²⁾	PCL	Program Counter (PC) Least Significant Byte								0000 0000	28,37
03h ⁽²⁾	STATUS	IRP	RP1	RP0	\overline{TO}	\overline{PD}	Z	DC	C	0001 1xxx	25,37
04h ⁽²⁾	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	29,37
05h	PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx xxxx	51,37
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	60,37
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	70,37
08h ⁽³⁾	PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	77,37
09h	PORTE	—	—	—	—	RE3	RE2 ⁽³⁾	RE1 ⁽³⁾	RE0 ⁽³⁾	---- xxxx	81,37
0Ah ^(1, 2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	28,37
0Bh ⁽²⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	44,37
0Ch	PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	47,37
0Dh	PIR2	—	—	—	—	—	—	—	CCP2IF	---- --0	48,37
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	113,37
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	113,37
10h	T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYN\overline{C}}$	—	TMR1ON	0000 00-0	117,37
11h	TMR2	Timer2 Module Register								0000 0000	120,37
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	121,37
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	161,37
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	178,37
15h	CCPR1L	Capture/Compare/PWM Register (LSB)								xxxx xxxx	130,37
16h	CCPR1H	Capture/Compare/PWM Register (MSB)								xxxx xxxx	130,37
17h	CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	129,37
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	148,37
19h	TXREG	USART Transmit Data Register								0000 0000	147,37
1Ah	RCREG	USART Receive Data Register								0000 0000	145,37
1Bh	CCPR2L	Capture/Compare/PWM Register 2 (LSB)								xxxx xxxx	130,37
1Ch	CCPR2H	Capture/Compare/PWM Register 2 (MSB)								xxxx xxxx	130,37
1Dh	CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	129,37
1Eh	ADRES	A/D Result Register								xxxx xxxx	100,37
1Fh	ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	$\overline{GO/DONE}$	ADON	--00 0000	99,37

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

- Note** 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter.
- 2: These registers can be addressed from any bank.
- 3: These registers/bits are not implemented on PIC16F722/723/726/PIC16LF722/723/726 devices, read as '0'.
- 4: Accessible only when SSPM<3:0> = 1001.
- 5: Accessible only when SSPM<3:0> ≠ 1001.
- 6: This bit is always '1' as RE3 is input-only.

PIC16(L)F722/3/4/6/7

3.1 MCLR

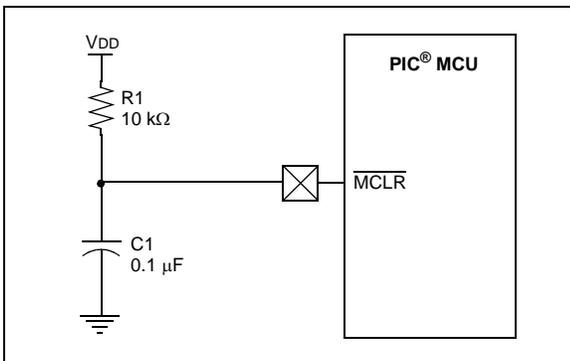
The PIC16(L)F722/3/4/6/7 has a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

It should be noted that a Reset does not drive the MCLR pin low.

Voltages applied to the pin that exceed its specification can result in both MCLR Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the MCLR pin no longer be tied directly to VDD. The use of an RC network, as shown in Figure 3-2, is suggested.

An internal MCLR option is enabled by clearing the MCLRE bit in the Configuration Word register. When MCLRE = 0, the Reset signal to the chip is generated internally. When the MCLRE = 1, the RE3/MCLR pin becomes an external Reset input. In this mode, the RE3/MCLR pin has a weak pull-up to VDD. In-Circuit Serial Programming is not affected by selecting the internal MCLR option.

FIGURE 3-2: RECOMMENDED MCLR CIRCUIT



3.2 Power-on Reset (POR)

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. A maximum rise time for VDD is required. See Section 23.0 “Electrical Specifications” for details. If the BOR is enabled, the maximum rise time specification does not apply. The BOR circuitry will keep the device in Reset until VDD reaches VBOR (see Section 3.5 “Brown-Out Reset (BOR)”).

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to Application Note AN607, *Power-up Trouble Shooting* (DS00607).

3.3 Power-up Timer (PWRT)

The Power-up Timer provides a fixed 64 ms (nominal) time out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates from the WDT oscillator. For more information, see Section 7.3 “Internal Clock Modes”. The chip is kept in Reset as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A Configuration bit, PWRTÉ, can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should be enabled when Brown-out Reset is enabled, although it is not required.

The Power-up Timer delay will vary from chip-to-chip and vary due to:

- VDD variation
- Temperature variation
- Process variation

See DC parameters for details (Section 23.0 “Electrical Specifications”).

Note: The Power-up Timer is enabled by the PWRTÉ bit in the Configuration Word.

3.4 Watchdog Timer (WDT)

The WDT has the following features:

- Shares an 8-bit prescaler with Timer0
- Time-out period is from 17 ms to 2.2 seconds, nominal
- Enabled by a Configuration bit

WDT is cleared under certain conditions described in Table 3-1.

3.4.1 WDT OSCILLATOR

The WDT derives its time base from 31 kHz internal oscillator.

Note: When the Oscillator Start-up Timer (OST) is invoked, the WDT is held in Reset, because the WDT Ripple Counter is used by the OST to perform the oscillator delay count. When the OST count has expired, the WDT will begin counting (if enabled).

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TABLE 3-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	0000h	0001 1xxx	---- --0x
$\overline{\text{MCLR}}$ Reset during normal operation	0000h	000u uuuu	---- --uu
$\overline{\text{MCLR}}$ Reset during Sleep	0000h	0001 0uuu	---- --uu
WDT Reset	0000h	0000 uuuu	---- --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu
Brown-out Reset	0000h	0001 1xxx	---- --10
Interrupt Wake-up from Sleep	PC + 1 ⁽¹⁾	uuu1 0uuu	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and Global Interrupt Enable bit, GIE, is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

TABLE 3-6: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets ⁽¹⁾
STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu
PCON	—	—	—	—	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	---- --qq	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition. Shaded cells are not used by Resets.

Note 1: Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.

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4.5.3 PIE2 REGISTER

The PIE2 register contains the interrupt enable bits, as shown in Register 4-3.

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 4-3: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	CCP2IE
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-1 **Unimplemented:** Read as '0'

bit 0 **CCP2IE:** CCP2 Interrupt Enable bit

1 = Enables the CCP2 interrupt

0 = Disables the CCP2 interrupt

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4.5.5 PIR2 REGISTER

The PIR2 register contains the interrupt flag bits, as shown in Register 4-5.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 4-5: PIR2: PERIPHERAL INTERRUPT REQUEST REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	CCP2IF
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7-1 **Unimplemented:** Read as '0'

bit 0 **CCP2IF:** CCP2 Interrupt Flag bit

Capture Mode:

- 1 = A TMR1 register capture occurred (must be cleared in software)
- 0 = No TMR1 register capture occurred

Compare Mode:

- 1 = A TMR1 register compare match occurred (must be cleared in software)
- 0 = No TMR1 register compare match occurred

PWM mode:

Unused in this mode

TABLE 4-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
OPTION_REG	RBP <u>U</u>	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIE2	—	—	—	—	—	—	—	CCP2IE	---- ----0	---- ----0
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIR2	—	—	—	—	—	—	—	CCP2IF	---- ----0	---- ----0

Legend: — = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Capture, Compare and PWM.

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6.2.1 ANSELA REGISTER

The ANSELA register (Register 6-4) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no affect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

REGISTER 6-4: ANSELA: PORTA ANALOG SELECT REGISTER

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **ANSA<5:0>:** Analog Select between Analog or Digital Function on pins RA<5:0>, respectively

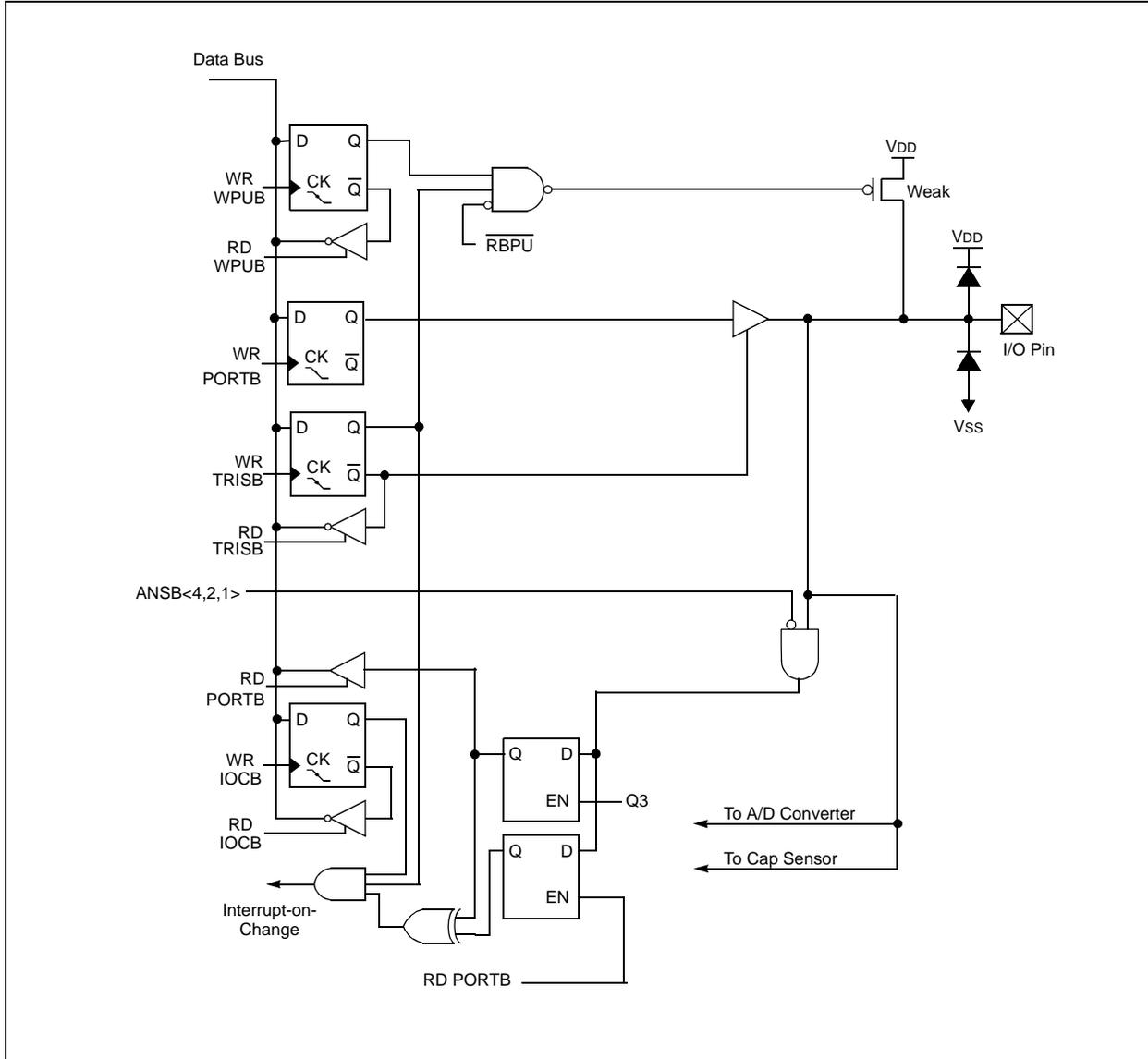
0 = Digital I/O. Pin is assigned to port or Digital special function.

1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital Input buffer disabled.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

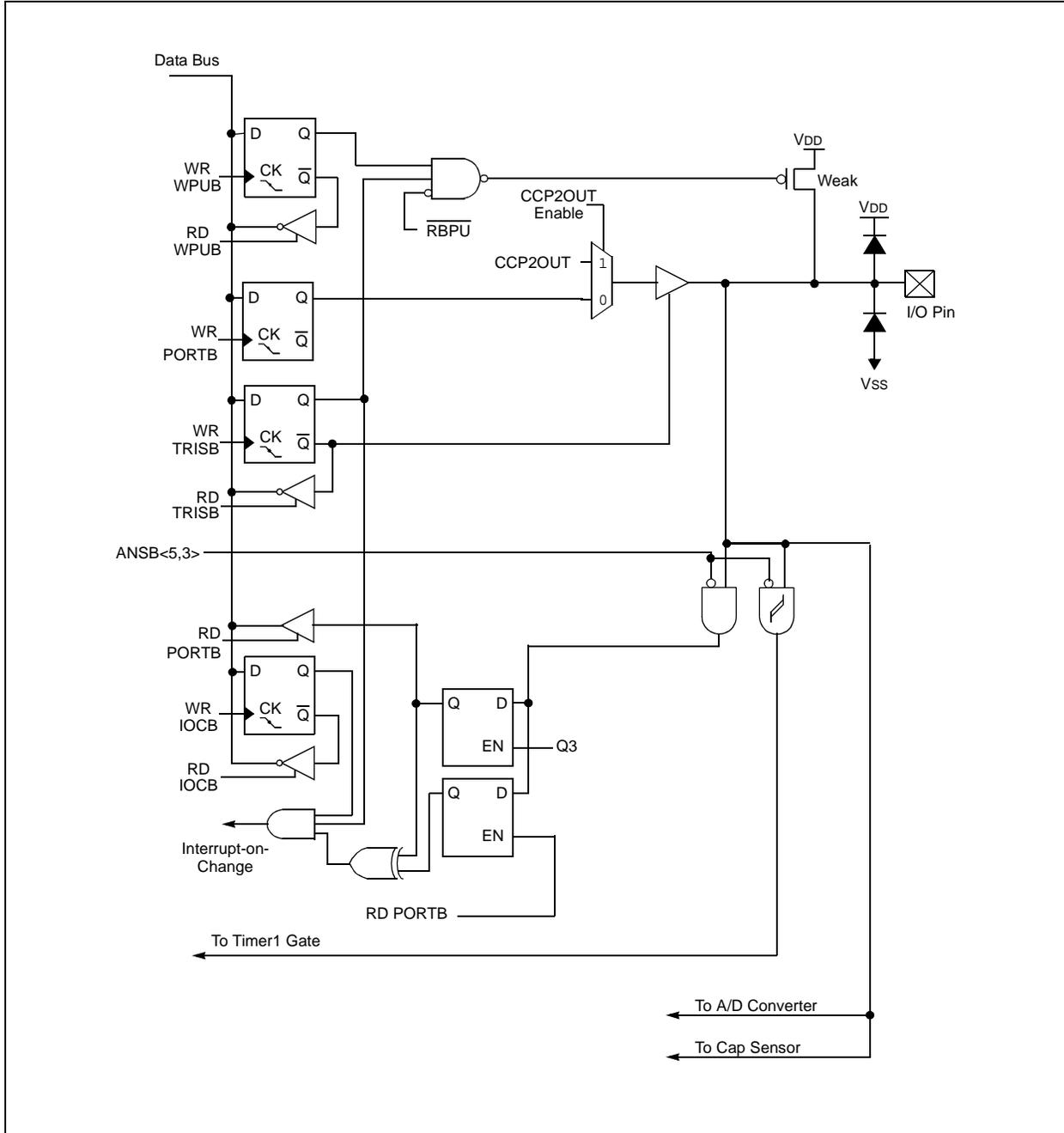
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FIGURE 6-8: BLOCK DIAGRAM OF RB4, RB<2:1>



PIC16(L)F722/3/4/6/7

FIGURE 6-10: BLOCK DIAGRAM OF RB5



9.1 ADC Configuration

When configuring and using the ADC, the following functions must be considered:

- Port configuration
- Channel selection
- ADC voltage reference selection
- ADC conversion clock source
- Interrupt control
- Results formatting

9.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRIS and ANSEL bits. Refer to **Section 6.0 “I/O Ports”** for more information.

Note: Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.

9.1.2 CHANNEL SELECTION

The CHS bits of the ADCON0 register determine which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion. Refer to **Section 9.2 “ADC Operation”** for more information.

9.1.3 ADC VOLTAGE REFERENCE

The ADREF bits of the ADCON1 register provides control of the positive voltage reference. The positive voltage reference can be either V_{DD} , an external voltage source or the internal Fixed Voltage Reference. The negative voltage reference is always connected to the ground reference. See **Section 10.0 “Fixed Voltage Reference”** for more details on the Fixed Voltage Reference.

9.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS bits of the ADCON1 register. There are seven possible clock options:

- $F_{osc}/2$
- $F_{osc}/4$
- $F_{osc}/8$
- $F_{osc}/16$
- $F_{osc}/32$
- $F_{osc}/64$
- FRC (dedicated internal oscillator)

The time to complete one bit conversion is defined as TAD. One full 8-bit conversion requires 10 TAD periods as shown in Figure 9-2.

For correct conversion, the appropriate TAD specification must be met. Refer to the A/D conversion requirements in **Section 23.0 “Electrical Specifications”** for more information. Table 9-1 gives examples of appropriate ADC clock selections.

Note: Unless using the FRC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.

14.1 Analog MUX

The capacitive sensing module can monitor up to 16 inputs. The capacitive sensing inputs are defined as CPS<15:0>. To determine if a frequency change has occurred the user must:

- Select the appropriate CPS pin by setting the CPSCCH<3:0> bits of the CPSCON1 register
- Set the corresponding ANSEL bit
- Set the corresponding TRIS bit
- Run the software algorithm

Selection of the CPSx pin while the module is enabled will cause the capacitive sensing oscillator to be on the CPSx pin. Failure to set the corresponding ANSEL and TRIS bits can cause the capacitive sensing oscillator to stop, leading to false frequency readings.

14.2 Capacitive Sensing Oscillator

The capacitive sensing oscillator consists of a constant current source and a constant current sink, to produce a triangle waveform. The CPSOUT bit of the CPSCON0 register shows the status of the capacitive sensing oscillator, whether it is a sinking or sourcing current. The oscillator is designed to drive a capacitive load (single PCB pad) and at the same time, be a clock source to either Timer0 or Timer1. The oscillator has three different current settings as defined by CPSCRNG<1:0> of the CPSCON0 register. The different current settings for the oscillator serve two purposes:

- Maximize the number of counts in a timer for a fixed time base
- Maximize the count differential in the timer during a change in frequency

14.3 Timer resources

To measure the change in frequency of the capacitive sensing oscillator, a fixed time base is required. For the period of the fixed time base, the capacitive sensing oscillator is used to clock either Timer0 or Timer1. The frequency of the capacitive sensing oscillator is equal to the number of counts in the timer divided by the period of the fixed time base.

14.4 Fixed Time Base

To measure the frequency of the capacitive sensing oscillator, a fixed time base is required. Any timer resource or software loop can be used to establish the fixed time base. It is up to the end user to determine the method in which the fixed time base is generated.

Note: The fixed time base can not be generated by timer resource the capacitive sensing oscillator is clocking.

14.4.1 TIMER0

To select Timer0 as the timer resource for the capacitive sensing module:

- Set the T0XCS bit of the CPSCON0 register
- Clear the T0CS bit of the OPTION register

When Timer0 is chosen as the timer resource, the capacitive sensing oscillator will be the clock source for Timer0. Refer to **Section 11.0 “Timer0 Module”** for additional information.

14.4.2 TIMER1

To select Timer1 as the timer resource for the capacitive sensing module, set the TMR1CS<1:0> of the T1CON register to ‘11’. When Timer1 is chosen as the timer resource, the capacitive sensing oscillator will be the clock source for Timer1. Because the Timer1 module has a gate control, developing a time base for the frequency measurement can be simplified using either:

- The Timer0 overflow flag
- The Timer2 overflow flag
- The WDT overflow flag

It is recommend that one of these flags, in conjunction with the toggle mode of the Timer1 Gate, is used to develop the fixed time base required by the software portion of the capacitive sensing module. Refer to **Section 12.0 “Timer1 Module with Gate Control”** for additional information.

TABLE 14-1: TIMER1 ENABLE FUNCTION

TMR1ON	TMR1GE	Timer1 Operation
0	0	Off
0	1	Off
1	0	On
1	1	Count Enabled by input

17.1.2 SLAVE MODE

For any SPI device acting as a slave, the data is transmitted and received as external clock pulses appear on SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

17.1.2.1 Slave Mode Operation

The SSP consists of a transmit/receive shift register (SSPSR) and a buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPBUF holds the data that was written to the SSPSR until the received data is ready.

The slave has no control as to when data will be clocked in or out of the device. All data that is to be transmitted, to a master or another slave, must be loaded into the SSPBUF register before the first clock pulse is received.

Once eight bits of data have been received:

- Received byte is moved to the SSPBUF register
- BF bit of the SSPSTAT register is set
- SSPIF bit of the PIR1 register is set

Any write to the SSPBUF register during transmission/reception of data will be ignored and the Write Collision Detect bit, WCOL of the SSPCON register, will be set. User software must clear the WCOL bit so that it can be determined if the following write(s) to the SSPBUF register completed successfully.

The user's firmware must read SSPBUF, clearing the BF flag, or the SSPOV bit of the SSPCON register will be set with the reception of the next byte and communication will be disabled.

A SPI module transmits and receives at the same time, occasionally causing dummy data to be transmitted/received. It is up to the user to determine which data is to be used and what can be discarded.

17.1.2.2 Enabling Slave I/O

To enable the serial port, the SSPEN bit of the SSPCON register must be set. If a Slave mode of operation is selected in the SSPM bits of the SSPCON register, the SDI, SDO, SCK pins will be assigned as serial port pins.

For these pins to function as serial port pins, they must have their corresponding data direction bits set or cleared in the associated TRIS register as follows:

- SDI configured as input
- SDO configured as output
- SCK configured as input

Optionally, a fourth pin, Slave Select (\overline{SS}) may be used in Slave mode. Slave Select may be configured to operate on one of the following pins via the SSSEL bit in the APFCON register.

- RA5/AN4/ \overline{SS}
- RA0/AN0/ \overline{SS}

Upon selection of a Slave Select pin, the appropriate bits must be set in the ANSELA and TRISA registers. Slave Select must be set as an input by setting the corresponding bit in TRISA, and digital I/O must be enabled on the \overline{SS} pin by clearing the corresponding bit of the ANSELA register.

17.1.2.3 Slave Mode Setup

When initializing the SSP module to SPI Slave mode, compatibility must be ensured with the master device. This is done by programming the appropriate control bits of the SSPCON and SSPSTAT registers. These control bits allow the following to be specified:

- SCK as clock input
- Idle state of SCK (CKP bit)
- Data input sample phase (SMP bit)
- Output data on rising/falling edge of SCK (CKE bit)

Figure 17-4 and Figure 17-5 show example waveforms of Slave mode operation.

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17.2.2 START AND STOP CONDITIONS

During times of no data transfer (Idle time), both the clock line (SCL) and the data line (SDA) are pulled high through external pull-up resistors. The Start and Stop conditions determine the start and stop of data transmission. The Start condition is defined as a high-to-low transition of the SDA line while SCL is high. The Stop condition is defined as a low-to-high transition of the SDA line while SCL is high.

Figure 17-9 shows the Start and Stop conditions. A master device generates these conditions for starting and terminating data transfer. Due to the definition of the Start and Stop conditions, when data is being transmitted, the SDA line can only change state when the SCL line is low.

17.2.3 ACKNOWLEDGE

After the valid reception of an address or data byte, the hardware automatically will generate the Acknowledge (ACK) pulse and load the SSPBUF register with the received value currently in the SSPSR register. There are certain conditions that will cause the SSP module not to generate this ACK pulse. They include any or all of the following:

- The Buffer Full bit, BF of the SSPSTAT register, was set before the transfer was received.
- The SSP Overflow bit, SSPOV of the SSPCON register, was set before the transfer was received.
- The SSP Module is being operated in Firmware Master mode.

In such a case, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF of the PIR1 register is set. Table 17-2 shows the results of when a data transfer byte is received, given the status of bits BF and SSPOV. Flag bit BF is cleared by reading the SSPBUF register, while bit SSPOV is cleared through software.

FIGURE 17-9: START AND STOP CONDITIONS

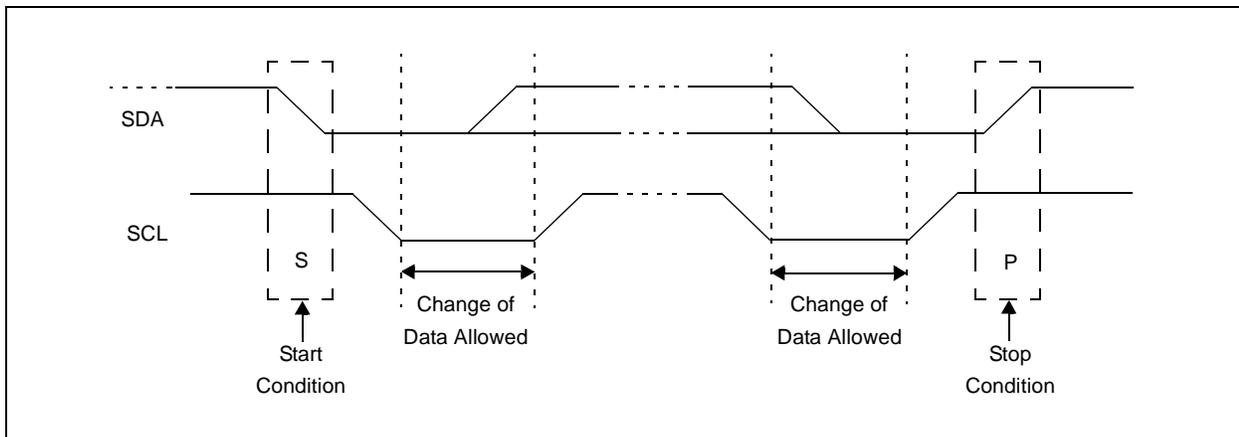


TABLE 17-2: DATA TRANSFER RECEIVED BYTE ACTIONS

Status Bits as Data Transfer is Received		SSPSR → SSPBUF	Generate $\overline{\text{ACK}}$ Pulse	Set bit SSPIF (SSP Interrupt occurs if enabled)
BF	SSPOV			
0	0	Yes	Yes	Yes
1	0	No	No	Yes
1	1	No	No	Yes
0	1	No	No	Yes

Note 1: Shaded cells show the conditions where the user software did not properly clear the overflow condition.

FIGURE 23-18: SPI SLAVE MODE TIMING (CKE = 0)

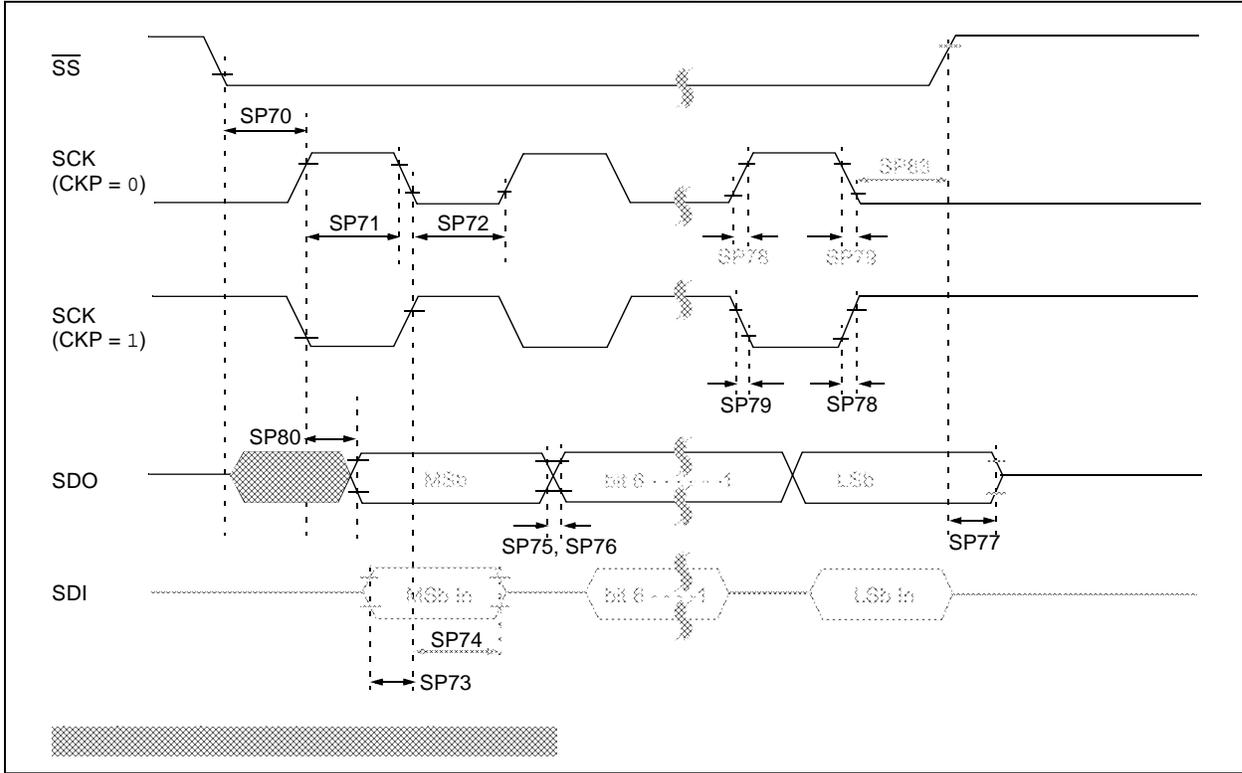


FIGURE 23-19: SPI SLAVE MODE TIMING (CKE = 1)

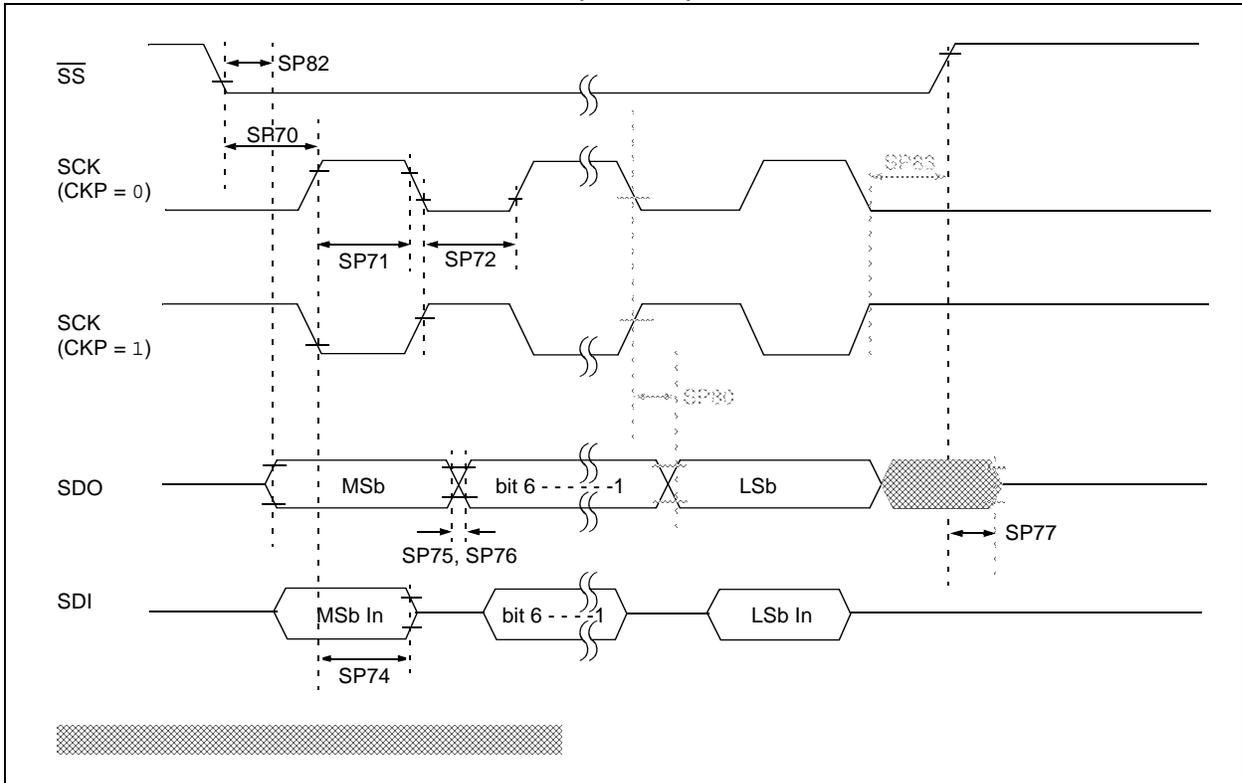


FIGURE 24-7: PIC16F722/3/4/6/7 TYPICAL I_{DD} vs. V_{DD} OVER F_{osc} , EXTRC MODE, $V_{CAP} = 0.1 \mu F$

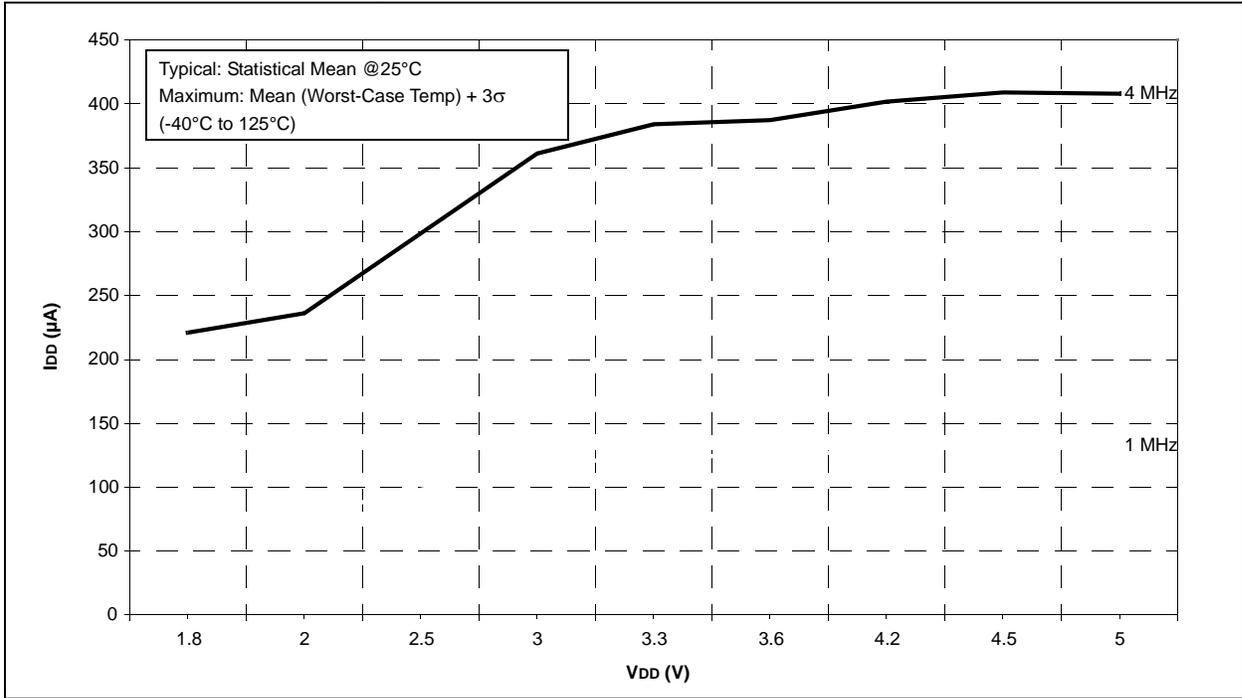
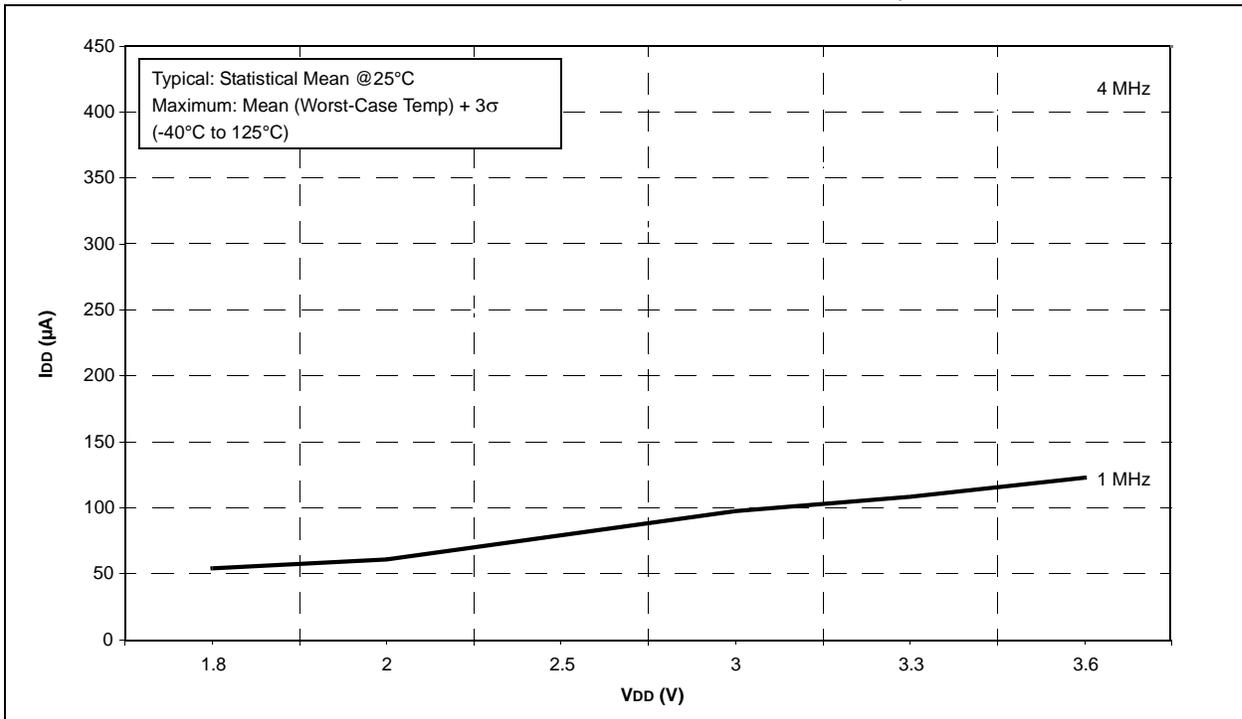


FIGURE 24-8: PIC16LF722/3/4/6/7 TYPICAL I_{DD} vs. V_{DD} OVER F_{osc} , EXTRC MODE



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FIGURE 24-39: PIC16F722/3/4/6/7 CAP SENSE LOW POWER IPD vs. VDD, VCAP = 0.1 μ F

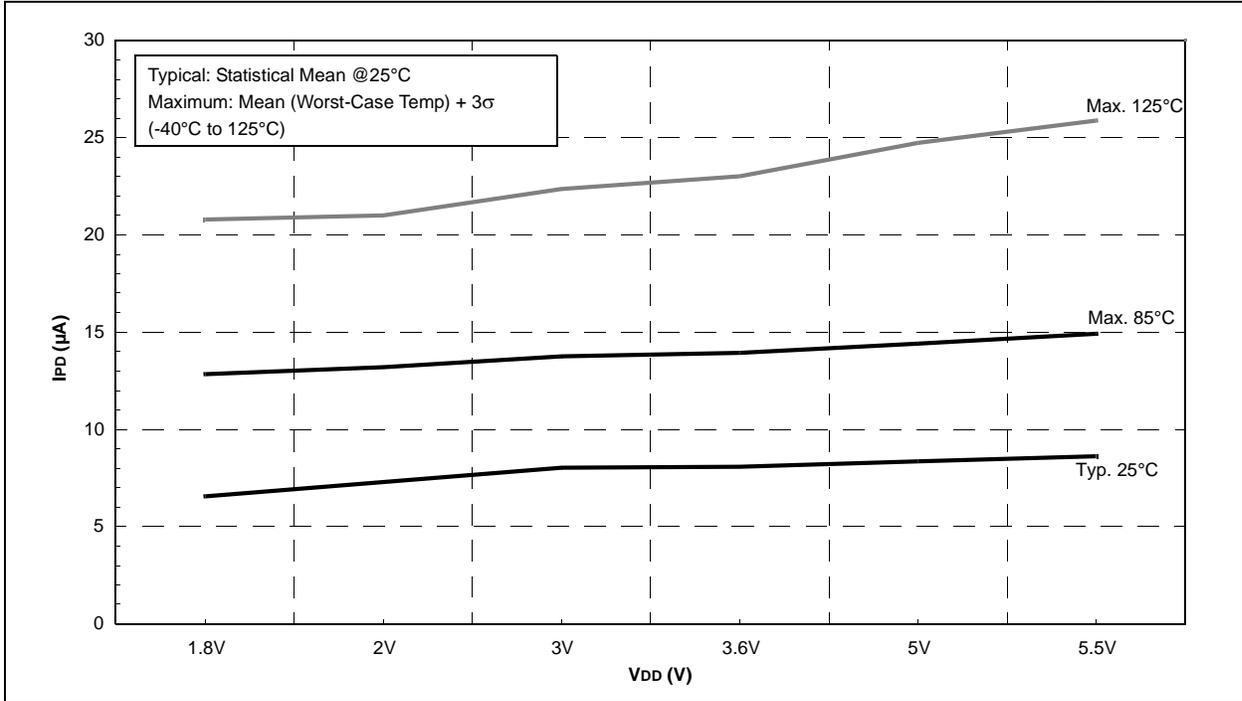


FIGURE 24-40: PIC16LF722/3/4/6/7 CAP SENSE LOW POWER IPD vs. VDD

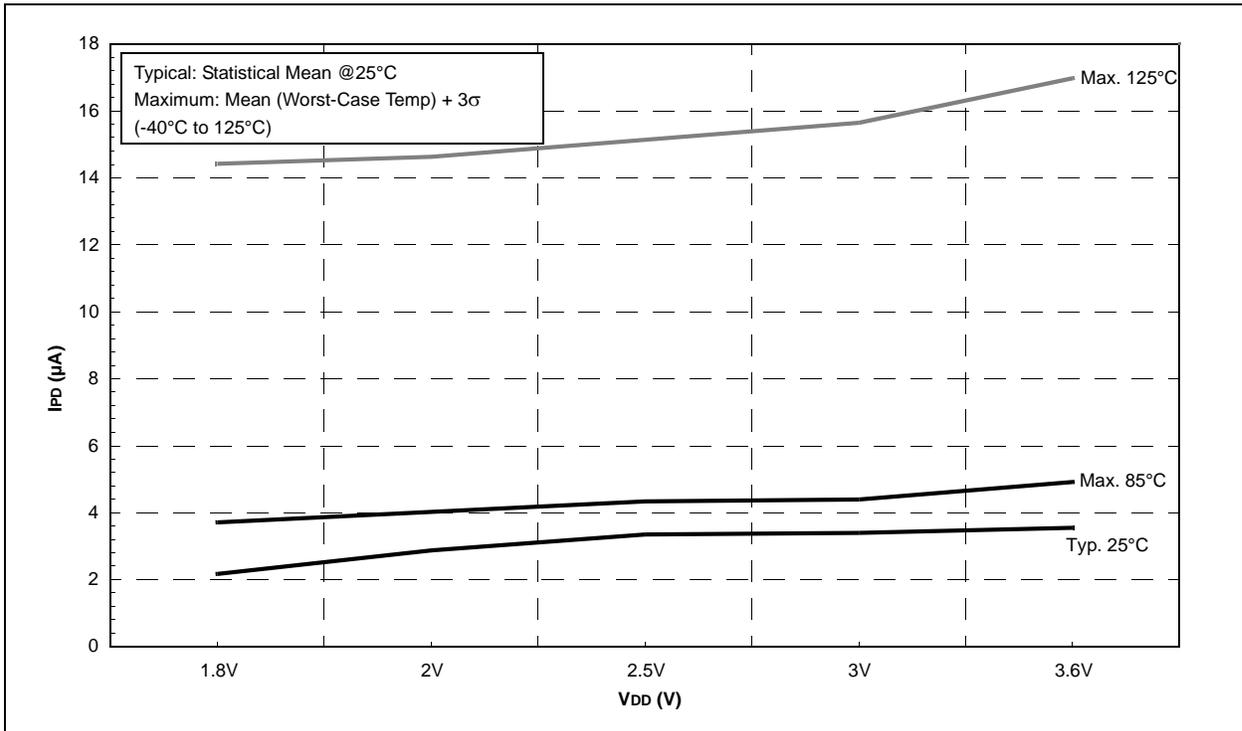


FIGURE 24-59: PIC16F722/3/4/6/7 WDT TIME-OUT PERIOD

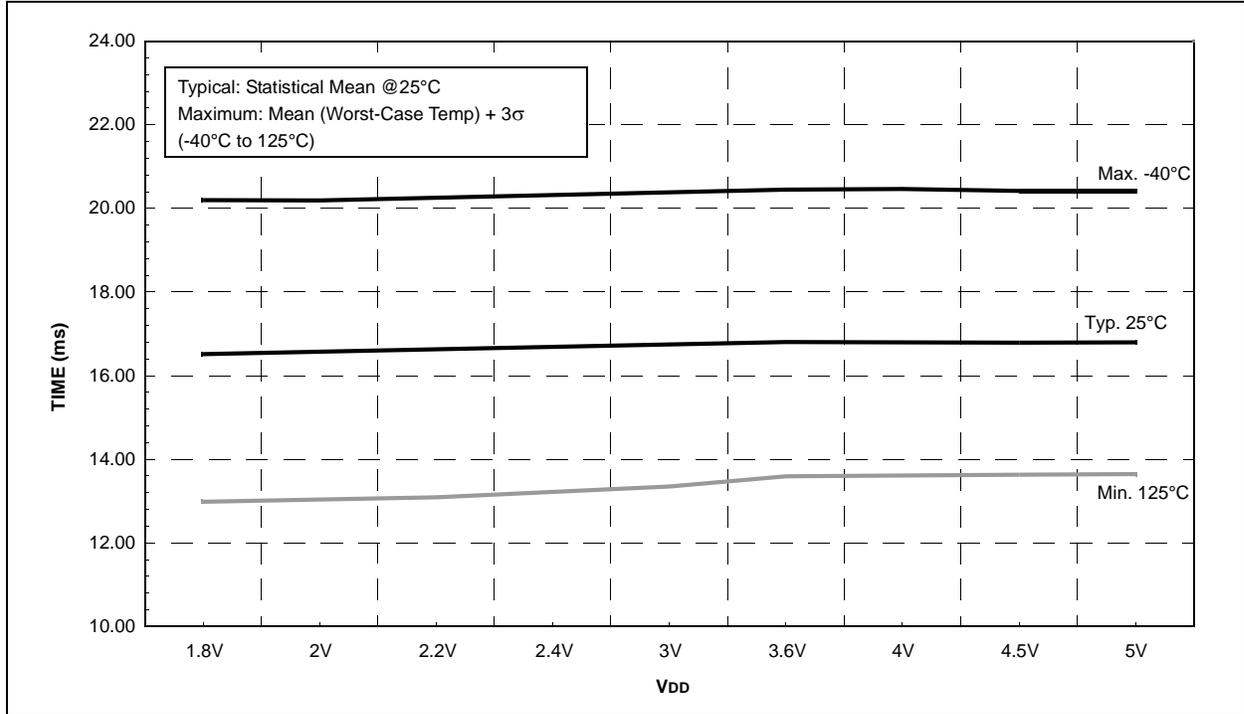
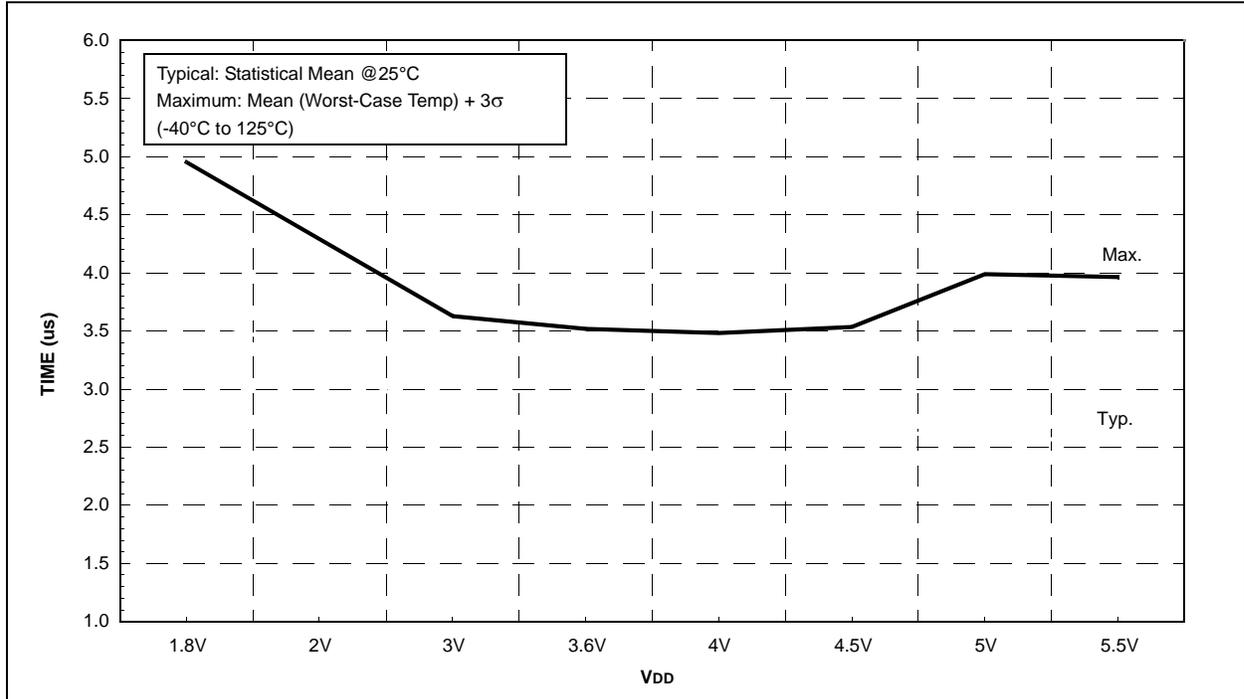
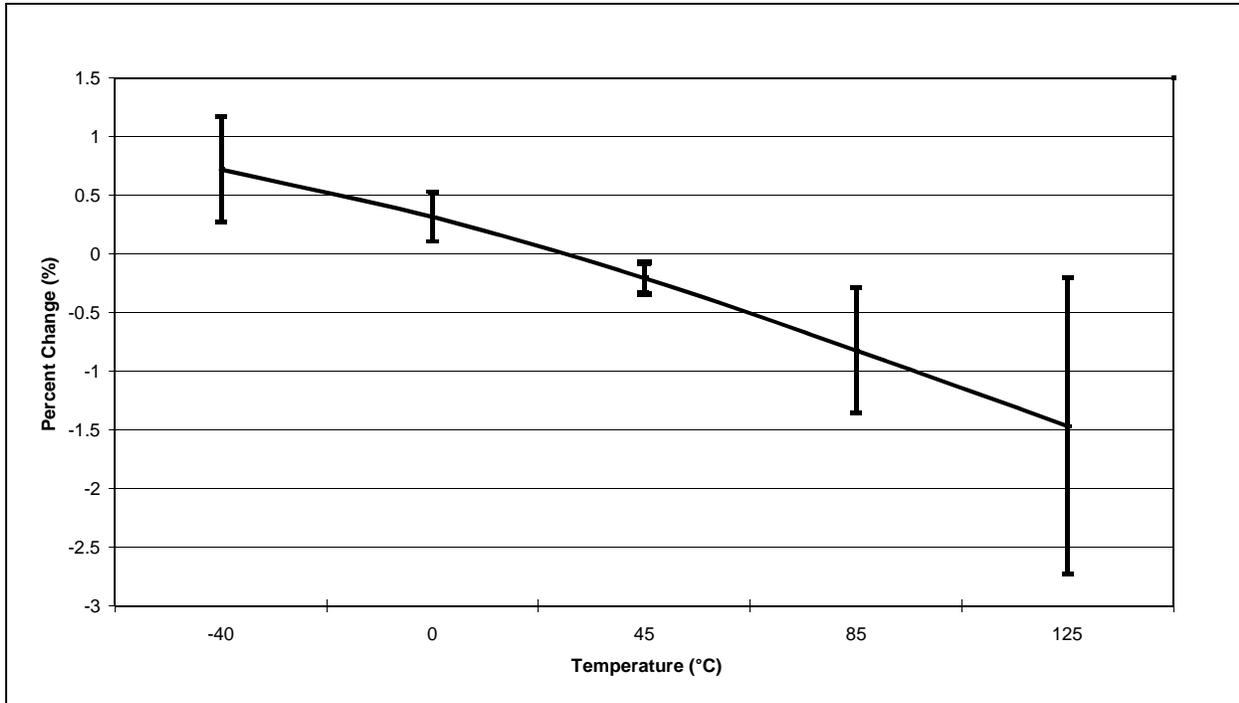


FIGURE 24-60: PIC16F722/3/4/6/7 HFINTOSC WAKE-UP FROM SLEEP START-UP TIME



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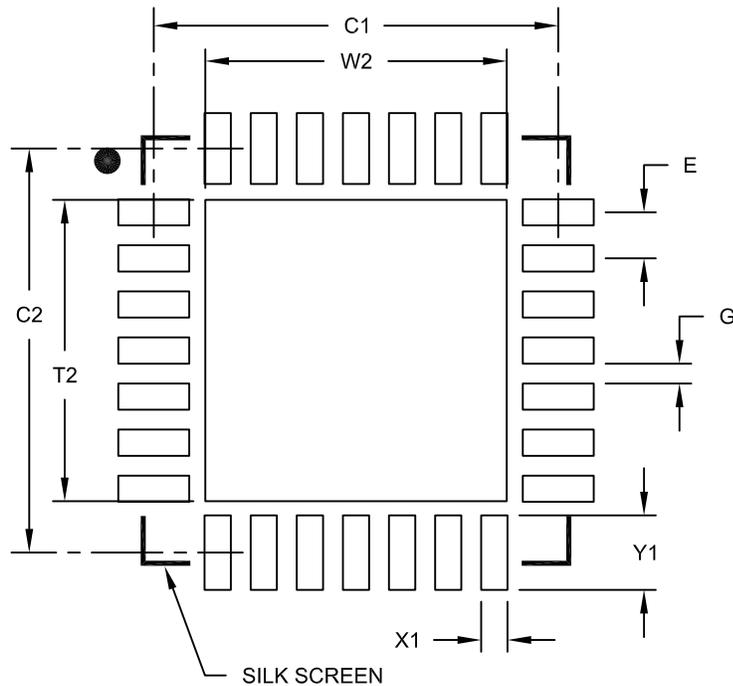
FIGURE 24-69: TYPICAL FVR CHANGE VS. TEMPERATURE NORMALIZED AT 25°C



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28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A