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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
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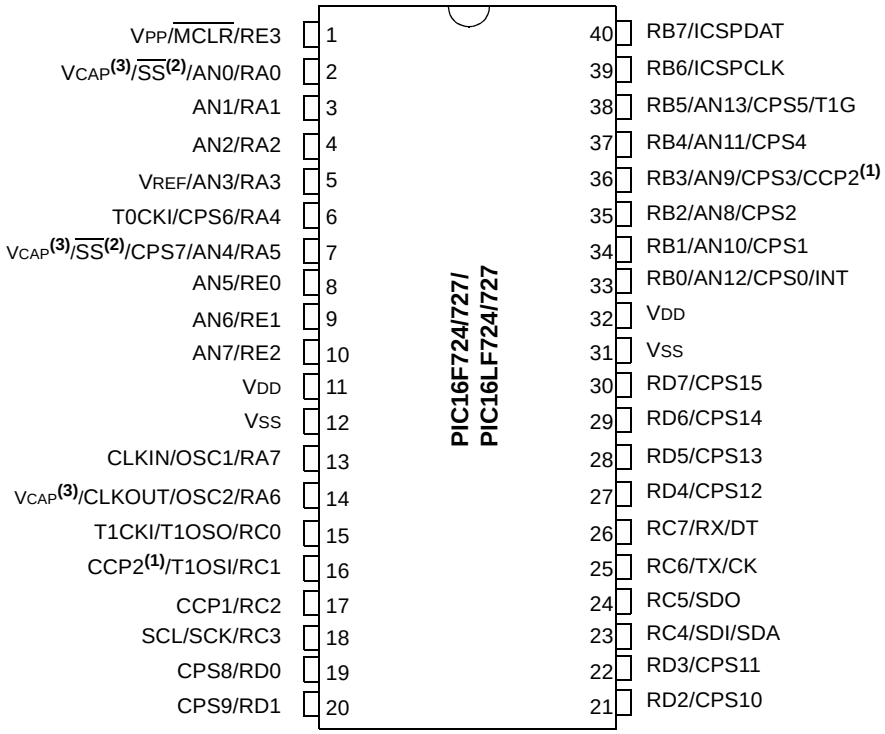
Number of I/O	25
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f722t-i-ss

Pin Diagrams – 40-PIN PDIP (PIC16F724/727/PIC16LF724/727)



Note 1: CCP2 pin location may be selected as RB3 or RC1.
2: SS pin location may be selected as RA5 or RA0.
3: PIC16F724/727 devices only.

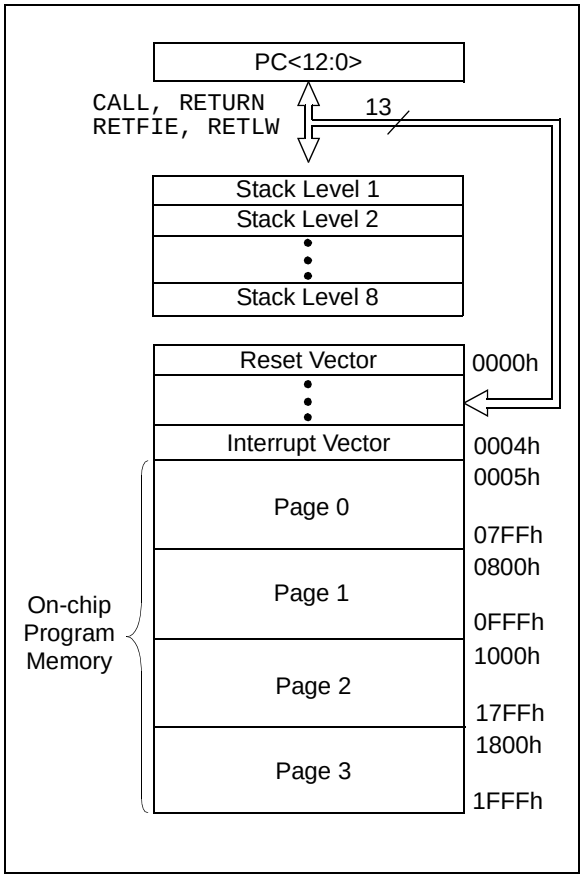
TABLE 2: 40/44-PIN PDIP/TQFP/QFN SUMMARY (PIC16F724/727/PIC16LF724/727)

I/O	40-Pin PDIP	44-Pin TQFP	44-Pin QFN	A/D	Cap Sensor	Timers	CCP	AUSART	SSP	Interrupt	Pull-Up	Basic
RA0	2	19	19	AN0	—	—	—	—	$\overline{SS}$(3)	—	—	V_{CAP}(4)
RA1	3	20	20	AN1	—	—	—	—	—	—	—	—
RA2	4	21	21	AN2	—	—	—	—	—	—	—	—
RA3	5	22	22	AN3/V_{REF}	—	—	—	—	—	—	—	—
RA4	6	23	23	—	CPS6	T0CKI	—	—	—	—	—	—
RA5	7	24	24	AN4	CPS7	—	—	—	$\overline{SS}$(3)	—	—	V_{CAP}(4)
RA6	14	31	33	—	—	—	—	—	—	—	—	OSC2/CLKOUT/V_{CAP}(4)
RA7	13	30	32	—	—	—	—	—	—	—	—	OSC1/CLKIN
RB0	33	8	9	AN12	CPS0	—	—	—	—	IOC/INT	Y	—
RB1	34	9	10	AN10	CPS1	—	—	—	—	IOC	Y	—
RB2	35	10	11	AN8	CPS2	—	—	—	—	IOC	Y	—
RB3	36	11	12	AN9	CPS3	—	CCP2(2)	—	—	IOC	Y	—
RB4	37	14	14	AN11	CPS4	—	—	—	—	IOC	Y	—
RB5	38	15	15	AN13	CPS5	T1G	—	—	—	IOC	Y	—
RB6	39	16	16	—	—	—	—	—	—	IOC	Y	ICSPCLK/ICDCLK
RB7	40	17	17	—	—	—	—	—	—	IOC	Y	ICSPDAT/ICDDAT
RC0	15	32	34	—	—	T1OSO/ T1CKI	—	—	—	—	—	—
RC1	16	35	35	—	—	T1OSI	CCP2(2)	—	—	—	—	—
RC2	17	36	36	—	—	—	CCP1	—	—	—	—	—
RC3	18	37	37	—	—	—	—	—	SCK/SCL	—	—	—
RC4	23	42	42	—	—		—	—	SDI/SDA	—	—	—
RC5	24	43	43	—	—		—	—	SDO	—	—	—
RC6	25	44	44	—	—	—	—	TX/CK	—	—	—	—
RC7	26	1	1	—	—	—	—	RX/DT	—	—	—	—
RD0	19	38	38	—	CPS8	—	—	—	—	—	—	—
RD1	20	39	39	—	CPS9	—	—	—	—	—	—	—
RD2	21	40	40	—	CPS10	—	—	—	—	—	—	—
RD3	22	41	41	—	CPS11	—	—	—	—	—	—	—
RD4	27	2	2	—	CPS12	—	—	—	—	—	—	—
RD5	28	3	3	—	CPS13	—	—	—	—	—	—	—
RD6	29	4	4	—	CPS14	—	—	—	—	—	—	—
RD7	30	5	5	—	CPS15	—	—	—	—	—	—	—
RE0	8	25	25	AN5	—	—	—	—	—	—	—	—
RE1	9	26	26	AN6	—	—	—	—	—	—	—	—
RE2	10	27	27	AN7	—	—	—	—	—	—	—	—
RE3	1	18	18	—	—	—	—	—	—	—	Y(1)	$\overline{MCLR}$/V_{PP}
—	11,32	7,28	7,8,28	—	—	—	—	—	—	—	—	V_{DD}
—	12,13	6,29	6,30,31	—	—	—	—	—	—	—	—	V_{SS}

Note 1: Pull-up enabled only with external $\overline{MCLR}$ configuration.
2: RC1 is the default pin location for CCP2. RB3 may be selected by changing the CCP2SEL bit in the APFCON register.
3: RA5 is the default pin location for $\overline{SS}$. RA0 may be selected by changing the SSSEL bit in the APFCON register.
4: PIC16F722/3/4/6/7 devices only.

Note: The PIC16F722/3/4/6/7 devices have an internal low dropout voltage regulator. An external capacitor must be connected to one of the available V_{CAP} pins to stabilize the regulator. For more information, see **Section 5.0 "Low Dropout (LDO) Voltage Regulator"**. The PIC16LF722/3/4/6/7 devices do not have the voltage regulator and therefore no external capacitor is required.

FIGURE 2-3: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F726/LF726 AND PIC16F727/LF727



2.2 Data Memory Organization

The data memory is partitioned into multiple banks which contain the General Purpose Registers (GPRs) and the Special Function Registers (SFRs). Bits RP0 and RP1 are bank select bits.

RP1	RP0		
0	0	→	Bank 0 is selected
0	1	→	Bank 1 is selected
1	0	→	Bank 2 is selected
1	1	→	Bank 3 is selected

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are the General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some frequently used Special Function Registers from one bank are mirrored in another bank for code reduction and quicker access.

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 128 x 8 bits in the PIC16F722/LF722, 192 x 8 bits in the PIC16F723/LF723 and PIC16F724/LF724, and 368 x 8 bits in the PIC16F726/LF726 and PIC16F727/LF727. Each register is accessed either directly or indirectly through the File Select Register (FSR), (Refer to **Section 2.5 "Indirect Addressing, INDF and FSR Registers"**).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (refer to Table 2-1). These registers are static RAM.

The Special Function Registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

FIGURE 2-6: PIC16F726/LF726 AND PIC16F727/LF727 SPECIAL FUNCTION REGISTERS

Bank 0	File Address	Bank 1	File Address	Bank 2	File Address	Bank 3	File Address
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION	81h	TMR0	101h	OPTION	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h	ANSELA	185h
PORTB	06h	TRISB	86h		106h	ANSELB	186h
PORTC	07h	TRISC	87h		107h		187h
PORTD(1)	08h	TRISD(1)	88h	CPSCON0	108h	ANSELD(1)	188h
PORTE	09h	TRISE	89h	CPSCON1	109h	ANSELE(1)	189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	PMDATL	10Ch	PMCON1	18Ch
PIR2	0Dh	PIE2	8Dh	PMADRL	10Dh	Reserved	18Dh
TMR1L	0Eh	PCON	8Eh	PMDATH	10Eh	Reserved	18Eh
TMR1H	0Fh	T1GCON	8Fh	PMADRH	10Fh	Reserved	18Fh
T1CON	10h	OSCCON	90h		110h		190h
TMR2	11h	OSCTUNE	91h		111h		191h
T2CON	12h	PR2	92h		112h		192h
SSPBUF	13h	SSPADD/SSPMSK	93h		113h		193h
SSPCON	14h	SSPSTAT	94h		114h		194h
CCPR1L	15h	WPUB	95h		115h		195h
CCPR1H	16h	IOCB	96h	General Purpose Register 16 Bytes	116h	General Purpose Register 16 Bytes	196h
CCP1CON	17h		97h		117h		197h
RCSTA	18h	TXSTA	98h		118h		198h
TXREG	19h	SPBRG	99h		119h		199h
RCREG	1Ah		9Ah		11Ah		19Ah
CCPR2L	1Bh		9Bh		11Bh		19Bh
CCPR2H	1Ch	APFCON	9Ch		11Ch		19Ch
CCP2CON	1Dh	FVRCON	9Dh		11Dh		19Dh
ADRES	1Eh		9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
	20h		A0h		120h		1A0h
General Purpose Register 96 Bytes	7Fh	General Purpose Register 80 Bytes	EFh	General Purpose Register 80 Bytes	16Fh	General Purpose Register 80 Bytes	1EFh
		Accesses 70h-7Fh	F0h	Accesses 70h-7Fh	170h	Accesses 70h-7Fh	1F0h
			FFh		17Fh		1FFh

Legend: = Unimplemented data memory locations, read as '0',
* = Not a physical register

Note 1: PORTD, TRISD, ANSELD and ANSELE are not implemented on the PIC16F726/LF726, read as '0'

TABLE 3-4: INITIALIZATION CONDITION FOR REGISTERS (CONTINUED)

Register	Address	Power-on Reset/ Brown-out Reset(1)	$\overline{\text{MCLR}}$ Reset/ WDT Reset	Wake-up from Sleep through Interrupt/Time out
PCON	8Eh	---- --qq	---- --uu(1,5)	---- --uu
T1GCON	8Fh	0000 0x00	uuuu uxuu	uuuu uxuu
OSCCON	90h	--10 qq--	--10 qq--	--uu qq--
OSCTUNE	91h	--00 0000	--uu uuuu	--uu uuuu
PR2	92h	1111 1111	1111 1111	uuuu uuuu
SSPADD	93h	0000 0000	0000 0000	uuuu uuuu
SSPMSK	93h	1111 1111	1111 1111	uuuu uuuu
SSPSTAT	94h	0000 0000	0000 0000	uuuu uuuu
WPUB	95h	1111 1111	1111 1111	uuuu uuuu
IOCB	96h	0000 0000	0000 0000	uuuu uuuu
TXSTA	98h	0000 -010	0000 -010	uuuu -uuu
SPBRG	99h	0000 0000	0000 0000	uuuu uuuu
APFCON	9Ch	---- --00	---- --00	---- --uu
FVRCON	9Dh	q000 --00	q000 --00	uuuu --uu
ADCON1	9Fh	-000 --00	-000 --00	-uuu --uu
CPSCON0	108h	0--- 0000	0--- 0000	u--- uuuu
CPSCON1	109h	---- 0000	---- 0000	---- uuuu
PMDATL	10Ch	xxxx xxxx	xxxx xxxx	uuuu uuuu
PMADRL	10Dh	xxxx xxxx	xxxx xxxx	uuuu uuuu
PMDATH	10Eh	--xx xxxx	--xx xxxx	--uu uuuu
PMADRH	10Fh	---x xxxx	---x xxxx	---u uuuu
ANSELA	185h	--11 1111	--11 1111	--uu uuuu
ANSELB	186h	--11 1111	--11 1111	--uu uuuu
ANSELD(6)	188h	1111 1111	1111 1111	uuuu uuuu
ANSELE	189h	---- -111	---- -111	---- -uuu
PMCON1	18Ch	1--- ---0	1--- ---0	u--- ---u

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 and PIR2 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 3-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

6: PIC16F724/727/PIC16LF724/727 only.

REGISTER 4-1: INTCON: INTERRUPT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T0IE	INTE	RBIE(1)	T0IF(2)	INTF	RBIF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **T0IE:** Timer0 Overflow Interrupt Enable bit
1 = Enables the Timer0 interrupt
0 = Disables the Timer0 interrupt

bit 4 **INTE:** RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3 **RBIE:** PORTB Change Interrupt Enable bit(1)
1 = Enables the PORTB change interrupt
0 = Disables the PORTB change interrupt

bit 2 **T0IF:** Timer0 Overflow Interrupt Flag bit(2)
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INTF:** RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0 **RBIF:** PORTB Change Interrupt Flag bit
1 = When at least one of the PORTB general purpose I/O pins changed state (must be cleared in software)
0 = None of the PORTB general purpose I/O pins have changed state

Note 1: The appropriate bits in the IOCB register must also be set.
2: T0IF bit is set when Timer0 rolls over. Timer0 is unchanged on Reset and should be initialized before clearing T0IF bit.

6.0 I/O PORTS

There are as many as 35 general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

6.1 Alternate Pin Function

The Alternate Pin Function Control (APFCON) register is used to steer specific peripheral input and output functions between different pins. The APFCON register is shown in Register 6-1. For this device family, the following functions can be moved between different pins.

- $\overline{SS}$ (Slave Select)
- CCP2

REGISTER 6-1: APFCON: ALTERNATE PIN FUNCTION CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	SSSEL	CCP2SEL
bit 7							bit 0

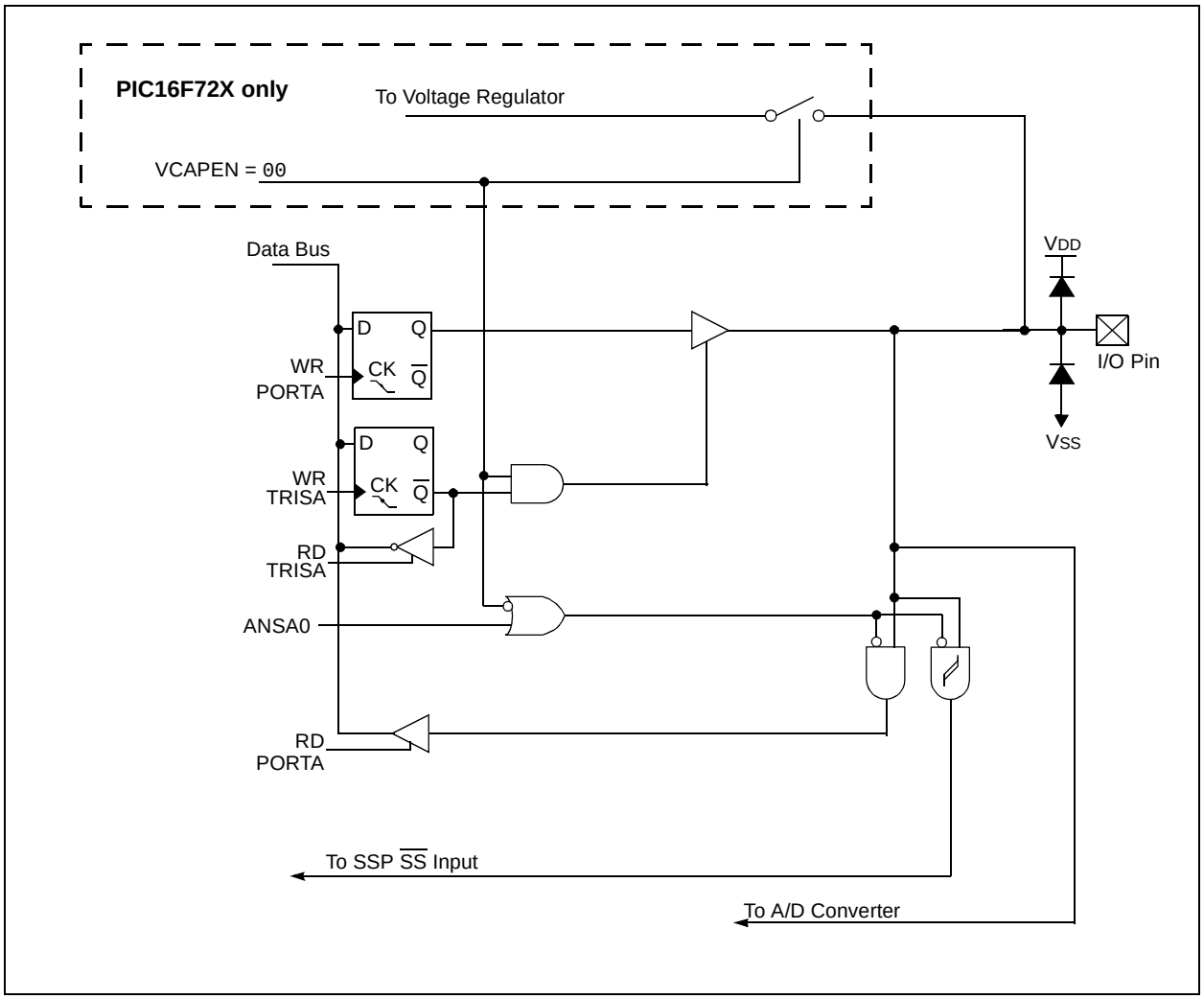
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as ‘0’.

bit 1 **SSSEL:** $\overline{SS}$ Input Pin Selection bit
0 = $\overline{SS}$ function is on RA5/AN4/CPS7/$\overline{SS}$/V_{CAP}
1 = $\overline{SS}$ function is on RA0/AN0/$\overline{SS}$/V_{CAP}

bit 0 **CCP2SEL:** CCP2 Input/Output Pin Selection bit
0 = CCP2 function is on RC1/T1OSI/CCP2
1 = CCP2 function is on RB3/CCP2

FIGURE 6-1: BLOCK DIAGRAM OF RA0



14.1 Analog MUX

The capacitive sensing module can monitor up to 16 inputs. The capacitive sensing inputs are defined as CPS<15:0>. To determine if a frequency change has occurred the user must:

- Select the appropriate CPS pin by setting the CPSCH<3:0> bits of the CPSCON1 register
- Set the corresponding ANSEL bit
- Set the corresponding TRIS bit
- Run the software algorithm

Selection of the CPSx pin while the module is enabled will cause the capacitive sensing oscillator to be on the CPSx pin. Failure to set the corresponding ANSEL and TRIS bits can cause the capacitive sensing oscillator to stop, leading to false frequency readings.

14.2 Capacitive Sensing Oscillator

The capacitive sensing oscillator consists of a constant current source and a constant current sink, to produce a triangle waveform. The CPSOUT bit of the CPSCON0 register shows the status of the capacitive sensing oscillator, whether it is a sinking or sourcing current. The oscillator is designed to drive a capacitive load (single PCB pad) and at the same time, be a clock source to either Timer0 or Timer1. The oscillator has three different current settings as defined by CPSRNG<1:0> of the CPSCON0 register. The different current settings for the oscillator serve two purposes:

- Maximize the number of counts in a timer for a fixed time base
- Maximize the count differential in the timer during a change in frequency

14.3 Timer resources

To measure the change in frequency of the capacitive sensing oscillator, a fixed time base is required. For the period of the fixed time base, the capacitive sensing oscillator is used to clock either Timer0 or Timer1. The frequency of the capacitive sensing oscillator is equal to the number of counts in the timer divided by the period of the fixed time base.

14.4 Fixed Time Base

To measure the frequency of the capacitive sensing oscillator, a fixed time base is required. Any timer resource or software loop can be used to establish the fixed time base. It is up to the end user to determine the method in which the fixed time base is generated.

Note:	The fixed time base can not be generated by timer resource the capacitive sensing oscillator is clocking.

14.4.1 TIMER0

To select Timer0 as the timer resource for the capacitive sensing module:

- Set the T0XCS bit of the CPSCON0 register
- Clear the T0CS bit of the OPTION register

When Timer0 is chosen as the timer resource, the capacitive sensing oscillator will be the clock source for Timer0. Refer to **Section 11.0 “Timer0 Module”** for additional information.

14.4.2 TIMER1

To select Timer1 as the timer resource for the capacitive sensing module, set the TMR1CS<1:0> of the T1CON register to ‘11’. When Timer1 is chosen as the timer resource, the capacitive sensing oscillator will be the clock source for Timer1. Because the Timer1 module has a gate control, developing a time base for the frequency measurement can be simplified using either:

- The Timer0 overflow flag
- The Timer2 overflow flag
- The WDT overflow flag

It is recommend that one of these flags, in conjunction with the toggle mode of the Timer1 Gate, is used to develop the fixed time base required by the software portion of the capacitive sensing module. Refer to **Section 12.0 “Timer1 Module with Gate Control”** for additional information.

TABLE 14-1: TIMER1 ENABLE FUNCTION

TMR1ON	TMR1GE	Timer1 Operation
0	0	Off
0	1	Off
1	0	On
1	1	Count Enabled by input

15.2 Compare Mode

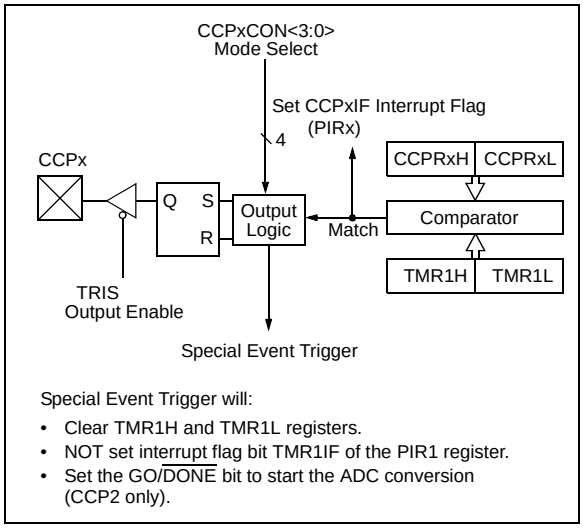
In Compare mode, the 16-bit CCPRx register value is constantly compared against the TMR1 register pair value. When a match occurs, the CCPx module may:

- Toggle the CCPx output
- Set the CCPx output
- Clear the CCPx output
- Generate a Special Event Trigger
- Generate a Software Interrupt

The action on the pin is based on the value of the CCPxM<3:0> control bits of the CCPxCON register.

All Compare modes can generate an interrupt.

FIGURE 15-2: COMPARE MODE OPERATION BLOCK DIAGRAM



15.2.1 CCPx PIN CONFIGURATION

The user must configure the CCPx pin as an output by clearing the associated TRIS bit.

Either RC1 or RB3 can be selected as the CCP2 pin. Refer to **Section 6.1 "Alternate Pin Function"** for more information.

Note:	Clearing the CCPxCON register will force the CCPx compare output latch to the default low level. This is not the PORT I/O data latch.

15.2.2 TIMER1 MODE SELECTION

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

Note:	Clocking Timer1 from the system clock (FOSC) should not be used in Compare mode. For the Compare operation of the TMR1 register to the CCPRx register to occur, Timer1 must be clocked from the Instruction Clock (FOSC/4) or from an external clock source.

15.2.3 SOFTWARE INTERRUPT MODE

When Software Interrupt mode is chosen (CCPxM<3:0> = 1010), the CCPxIF bit in the PIRx register is set and the CCPx module does not assert control of the CCPx pin (refer to the CCPxCON register).

15.2.4 SPECIAL EVENT TRIGGER

When Special Event Trigger mode is chosen (CCPxM<3:0> = 1011), the CCPx module does the following:

- Resets Timer1
- Starts an ADC conversion if ADC is enabled (CCP2 only)

The CCPx module does not assert control of the CCPx pin in this mode (refer to the CCPxCON register).

The Special Event Trigger output of the CCP occurs immediately upon a match between the TMR1H, TMR1L register pair and the CCPRxH, CCPRxL register pair. The TMR1H, TMR1L register pair is not reset until the next rising edge of the Timer1 clock. This allows the CCPRxH, CCPRxL register pair to effectively provide a 16-bit programmable period register for Timer1.

Note 1:	The Special Event Trigger from the CCP module does not set interrupt flag bit TMR1IF of the PIR1 register.
2:	Removing the match condition by changing the contents of the CCPRxH and CCPRxL register pair, between the clock edge that generates the Special Event Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring.

15.2.5 COMPARE DURING SLEEP

The Compare Mode is dependent upon the system clock (FOSC) for proper operation. Since FOSC is shut down during Sleep mode, the Compare mode will not function properly during Sleep.

TABLE 15-7: SUMMARY OF REGISTERS ASSOCIATED WITH PWM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	--11 1111	--11 1111
APFCON	—	—	—	—	—	—	SSSEL	CCP2SEL	---- --00	---- --00
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000
CCPRxL	Capture/Compare/PWM Register X Low Byte								xxxx xxxx	uuuu uuuu
CCPRxH	Capture/Compare/PWM Register X High Byte								xxxx xxxx	uuuu uuuu
PR2	Timer2 Period Register								1111 1111	1111 1111
T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
TMR2	Timer2 Module Register								0000 0000	0000 0000
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

Legend: - = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the PWM.

16.3 AUSART Synchronous Mode

Synchronous serial communications are typically used in systems with a single master and one or more slaves. The master device contains the necessary circuitry for baud rate generation and supplies the clock for all devices in the system. Slave devices can take advantage of the master clock by eliminating the internal clock generation circuitry.

There are two signal lines in Synchronous mode: a bidirectional data line and a clock line. Slaves use the external clock supplied by the master to shift the serial data into and out of their respective receive and transmit shift registers. Since the data line is bidirectional, synchronous operation is half-duplex only. Half-duplex refers to the fact that master and slave devices can receive and transmit data but not both simultaneously. The AUSART can operate as either a master or slave device.

Start and Stop bits are not used in synchronous transmissions.

16.3.1 SYNCHRONOUS MASTER MODE

The following bits are used to configure the AUSART for Synchronous Master operation:

- SYNC = 1
- CSRC = 1
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXSTA register configures the device for synchronous operation. Setting the CSRC bit of the TXSTA register configures the device as a master. Clearing the SREN and CREN bits of the RCSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCSTA register enables the AUSART.

16.3.1.1 Master Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a master transmits the clock on the TX/CK line. The TX/CK pin output driver is automatically enabled when the AUSART is configured for synchronous transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One clock cycle is generated for each data bit. Only as many clock cycles are generated as there are data bits.

16.3.1.2 Synchronous Master Transmission

Data is transferred out of the device on the RX/DT pin. The RX/DT and TX/CK pin output drivers are automatically enabled when the AUSART is configured for synchronous master transmit operation.

A transmission is initiated by writing a character to the TXREG register. If the TSR still contains all or part of a previous character, the new character data is held in the TXREG until the last bit of the previous character has been transmitted. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR. The transmission of the character commences immediately following the transfer of the data to the TSR from the TXREG.

Each data bit changes on the leading edge of the master clock and remains valid until the subsequent leading clock edge.

Note:	The TSR register is not mapped in data memory, so it is not available to the user.

16.3.1.3 Synchronous Master Transmission Setup:

1. Initialize the SPBRG register and the BRGH bit to achieve the desired baud rate (refer to **Section 16.2 “AUSART Baud Rate Generator (BRG)”**).
2. Enable the synchronous master serial port by setting bits SYNC, SPEN, and CSRC.
3. Disable Receive mode by clearing bits SREN and CREN.
4. Enable Transmit mode by setting the TXEN bit.
5. If 9-bit transmission is desired, set the TX9 bit.
6. If interrupts are desired, set the TXIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
7. If 9-bit transmission is selected, the ninth bit should be loaded in the TX9D bit.
8. Start transmission by loading data to the TXREG register.

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - (W) → (destination)

Status Affected: C, DC, Z

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f.

C = 0	W > f
C = 1	W ≤ f
DC = 0	W<3:0> > f<3:0>
DC = 1	W<3:0> ≤ f<3:0>

SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f<3:0>) → (destination<7:4>),
(f<7:4>) → (destination<3:0>)

Status Affected: None

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

XORLW **Exclusive OR literal with W**

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Description: The contents of the W register are XOR'ed with the 8-bit literal 'k'. The result is placed in the W register.

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (destination)

Status Affected: Z

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

23.2 DC Characteristics: PIC16(L)F722/3/4/6/7-I/E (Industrial, Extended)

PIC16LF722/3/4/6/7			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
PIC16F722/3/4/6/7			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Device Characteristics**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**	
						VDD	**Note**
	Supply Current (IDD)(1, 2)						
D009	LDO Regulator	—	350	—	µA	—	HS, EC OR INTOSC/INTOSCIO (8-16 MHz) Clock modes with all VCAP pins disabled
		—	50	—	µA	—	All VCAP pins disabled
		—	30	—	µA	—	VCAP enabled on RA0, RA5 or RA6
		—	5	—	µA	—	LP Clock mode and Sleep (requires FVR and BOR to be disabled)
D010		—	7.0	12	µA	1.8	FOSC = 32 kHz LP Oscillator mode **(Note 4)**, -40°C ≤ TA ≤ +85°C
		—	9.0	14	µA	3.0	
D010		—	11	20	µA	1.8	FOSC = 32 kHz LP Oscillator mode **(Note 4)**, -40°C ≤ TA ≤ +85°C
		—	14	22	µA	3.0	
		—	15	24	µA	5.0	
D011		—	7.0	12	µA	1.8	FOSC = 32 kHz LP Oscillator mode -40°C ≤ TA ≤ +125°C
		—	9.0	18	µA	3.0	
D011		—	11	21	µA	1.8	FOSC = 32 kHz LP Oscillator mode **(Note 4)** -40°C ≤ TA ≤ +125°C
		—	14	25	µA	3.0	
		—	15	27	µA	5.0	
D011		—	110	150	µA	1.8	FOSC = 1 MHz XT Oscillator mode
		—	150	215	µA	3.0	
D011		—	120	175	µA	1.8	FOSC = 1 MHz XT Oscillator mode **(Note 5)**
		—	180	250	µA	3.0	
		—	240	300	µA	5.0	
D012		—	230	300	µA	1.8	FOSC = 4 MHz XT Oscillator mode
		—	400	600	µA	3.0	
D012		—	250	350	µA	1.8	FOSC = 4 MHz XT Oscillator mode **(Note 5)**
		—	420	650	µA	3.0	
		—	500	750	µA	5.0	
D013		—	125	180	µA	1.8	FOSC = 1 MHz EC Oscillator mode
		—	230	270	µA	3.0	
D013		—	150	205	µA	1.8	FOSC = 1 MHz EC Oscillator mode **(Note 5)**
		—	225	320	µA	3.0	
		—	250	410	µA	5.0	

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ.

4: FVR and BOR are disabled.

5: 0.1 µF capacitor on VCAP (RA0).

FIGURE 23-16: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)

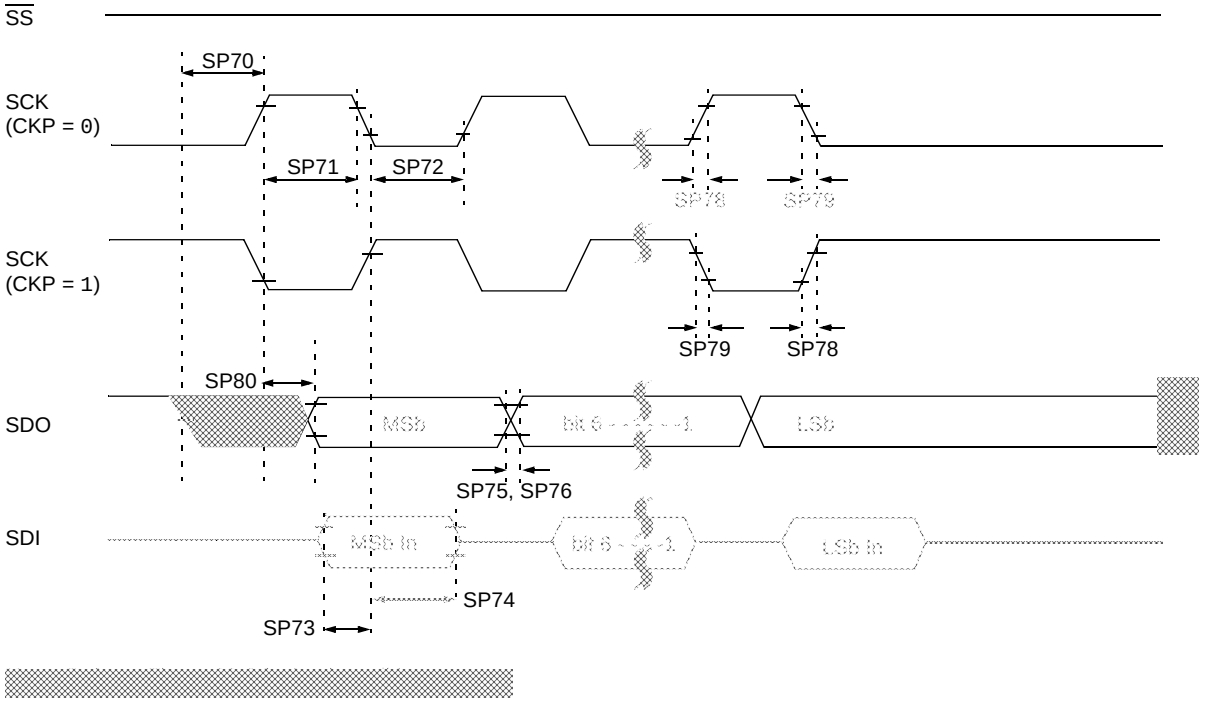
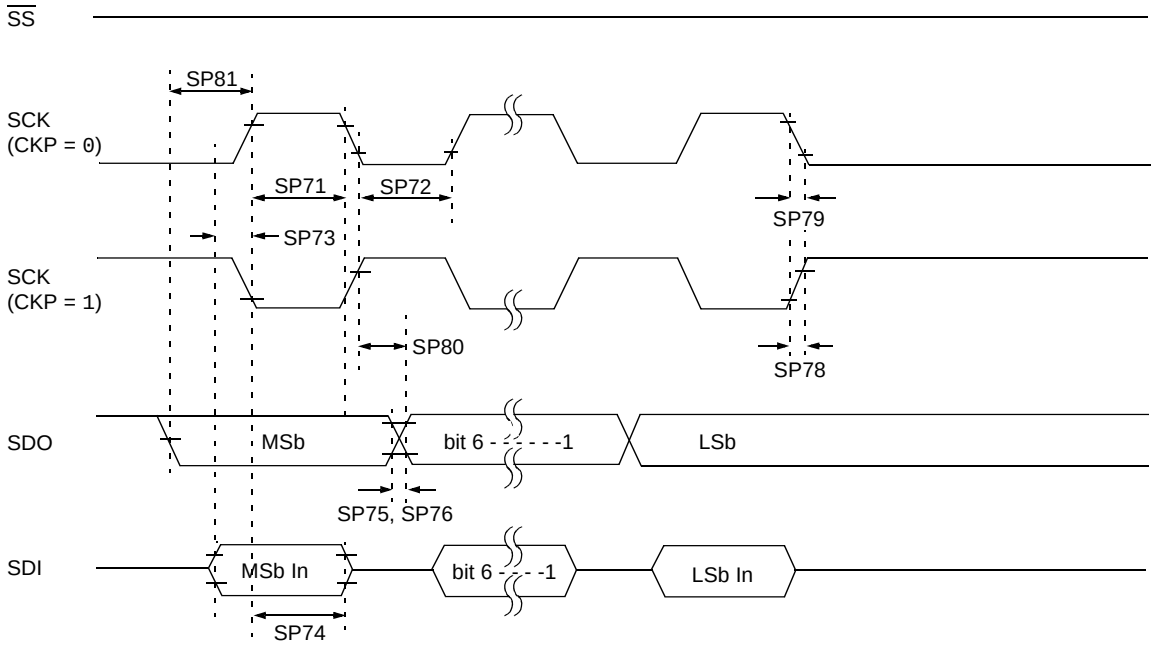


FIGURE 23-17: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)



Note: Refer to Figure 23-2 for load conditions.

FIGURE 23-18: SPI SLAVE MODE TIMING (CKE = 0)

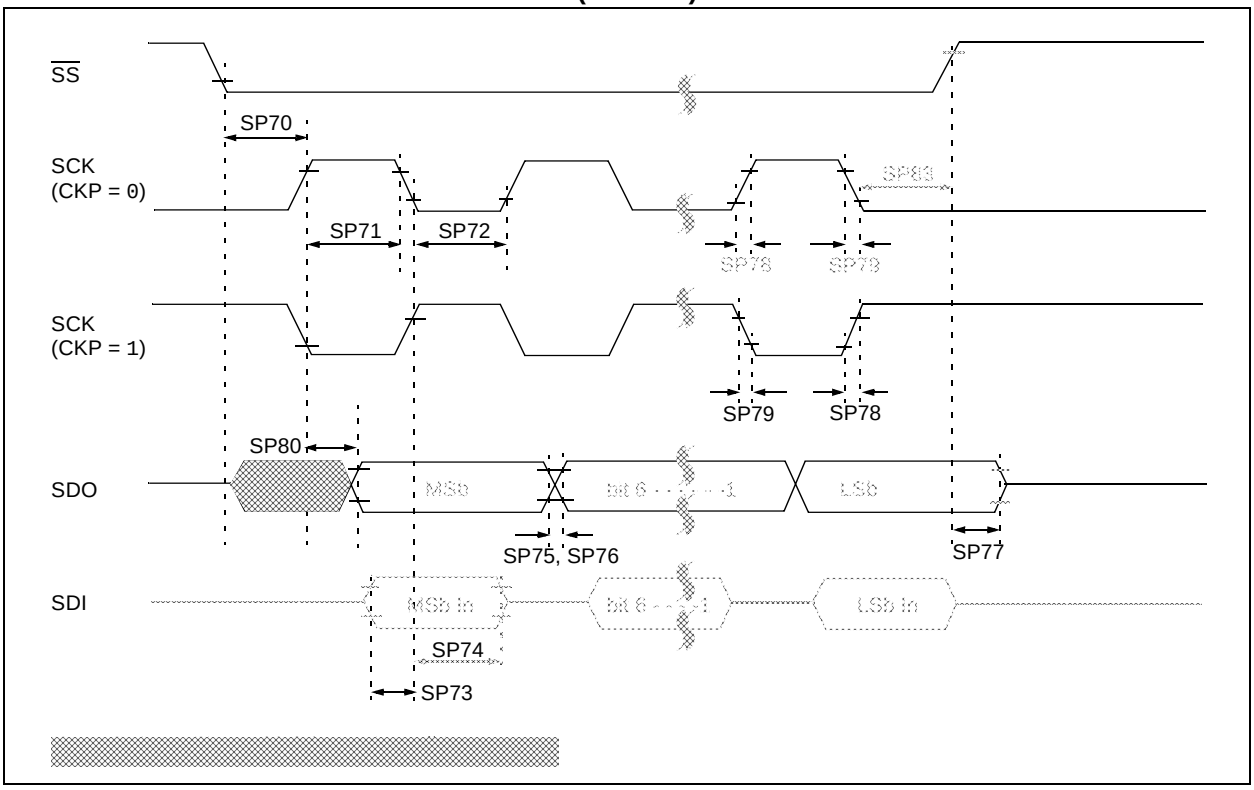


FIGURE 23-19: SPI SLAVE MODE TIMING (CKE = 1)

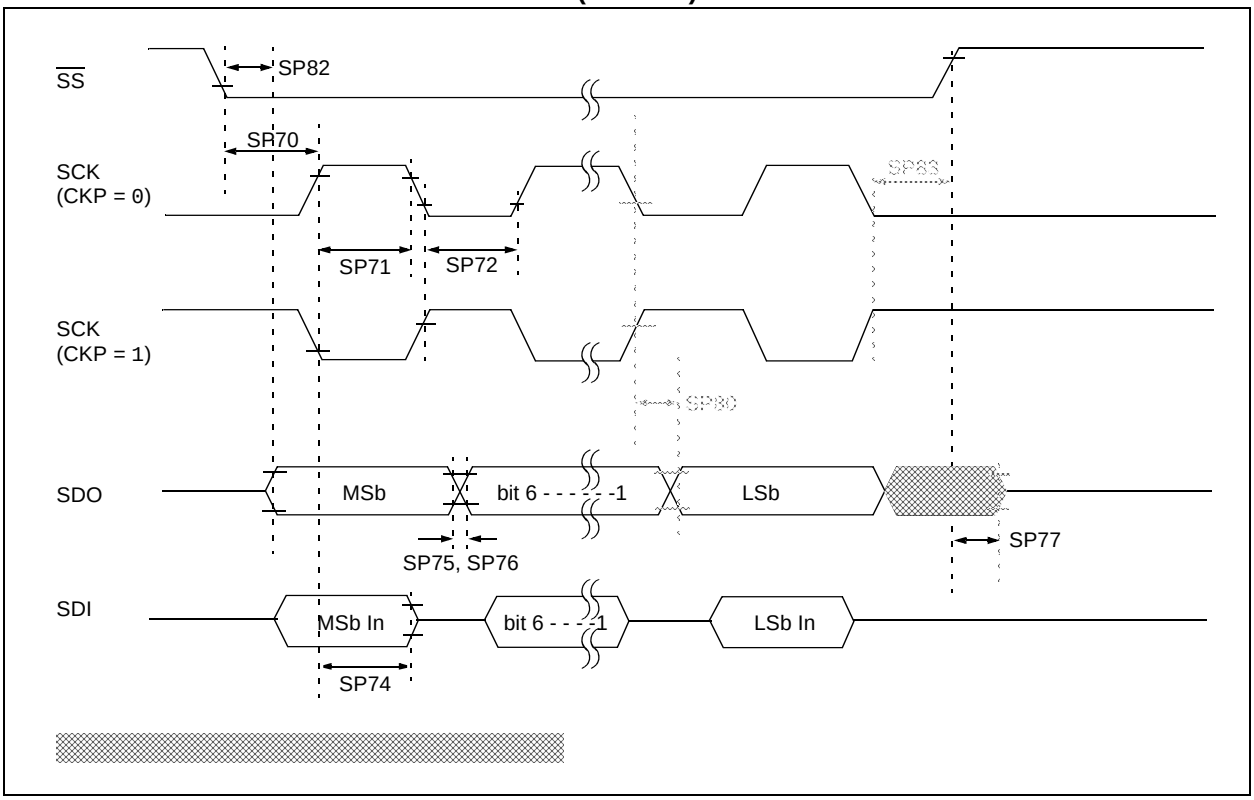


TABLE 23-14: CAP SENSE OSCILLATOR SPECIFICATIONS

Param. No.	Symbol	Characteristic		Min.	Typ†	Max.	Units	Conditions
CS01	ISRC	Current Source	High	—	-5.8	-6	µA	-40, -85°C
			Medium	—	-1.1	-3.2	µA	
			Low	—	-0.2	-0.9	µA	
CS02	ISNK	Current Sink	High	—	6.6	6	µA	-40, -85°C
			Medium	—	1.3	3.2	µA	
			Low	—	0.24	0.9	µA	
CS03	VCHYST	Cap Hysteresis	High	—	525	—	mV	VCTH-VCTL
			Medium	—	375	—	mV	
			Low	—	280	—	mV	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 23-22: CAP SENSE OSCILLATOR

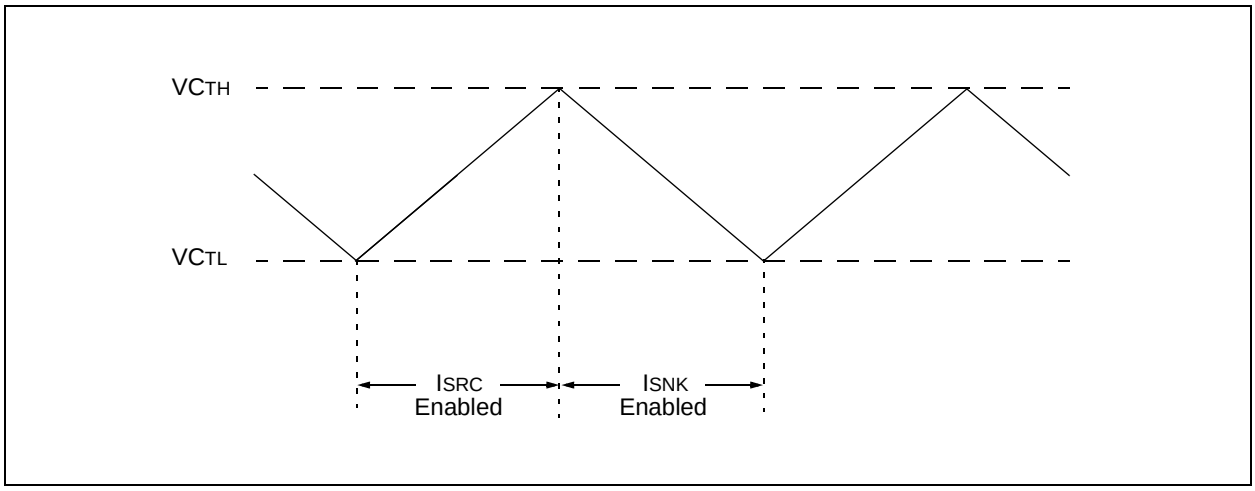


FIGURE 24-33: PIC16F722/3/4/6/7 BOR IPD vs. VDD, VCAP = 0.1 µF

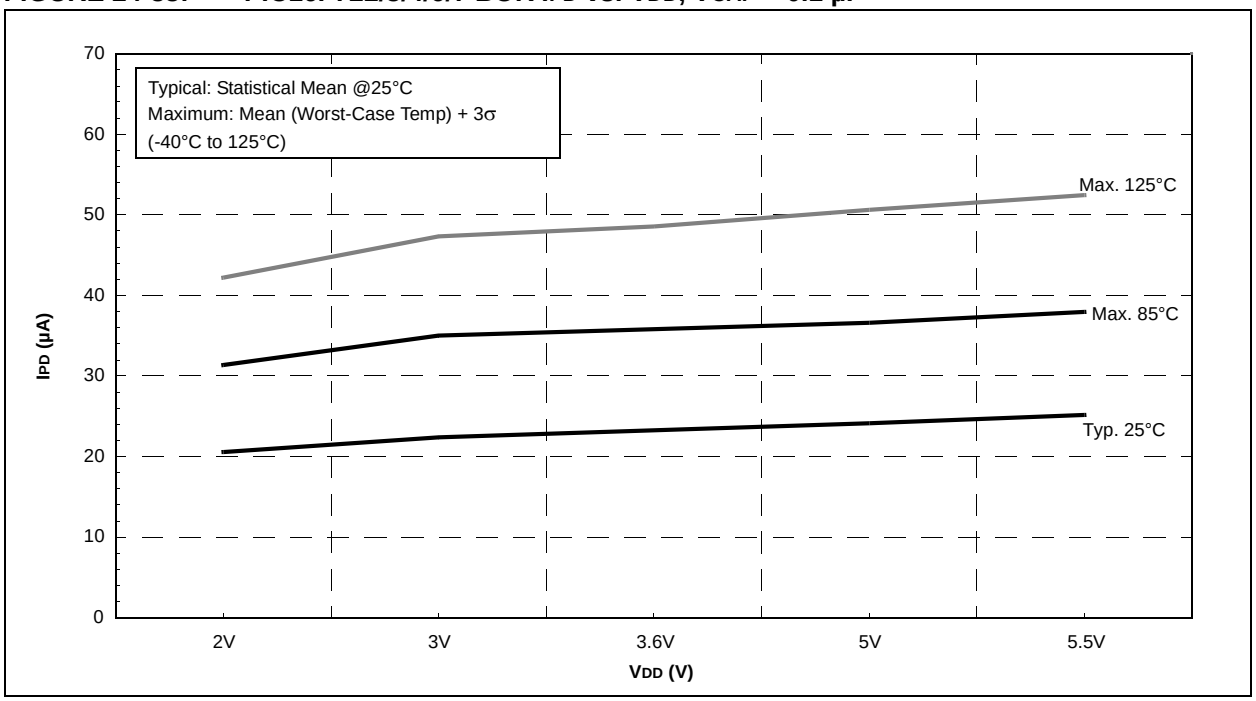


FIGURE 24-34: PIC16LF722/3/4/6/7 BOR IPD vs. VDD

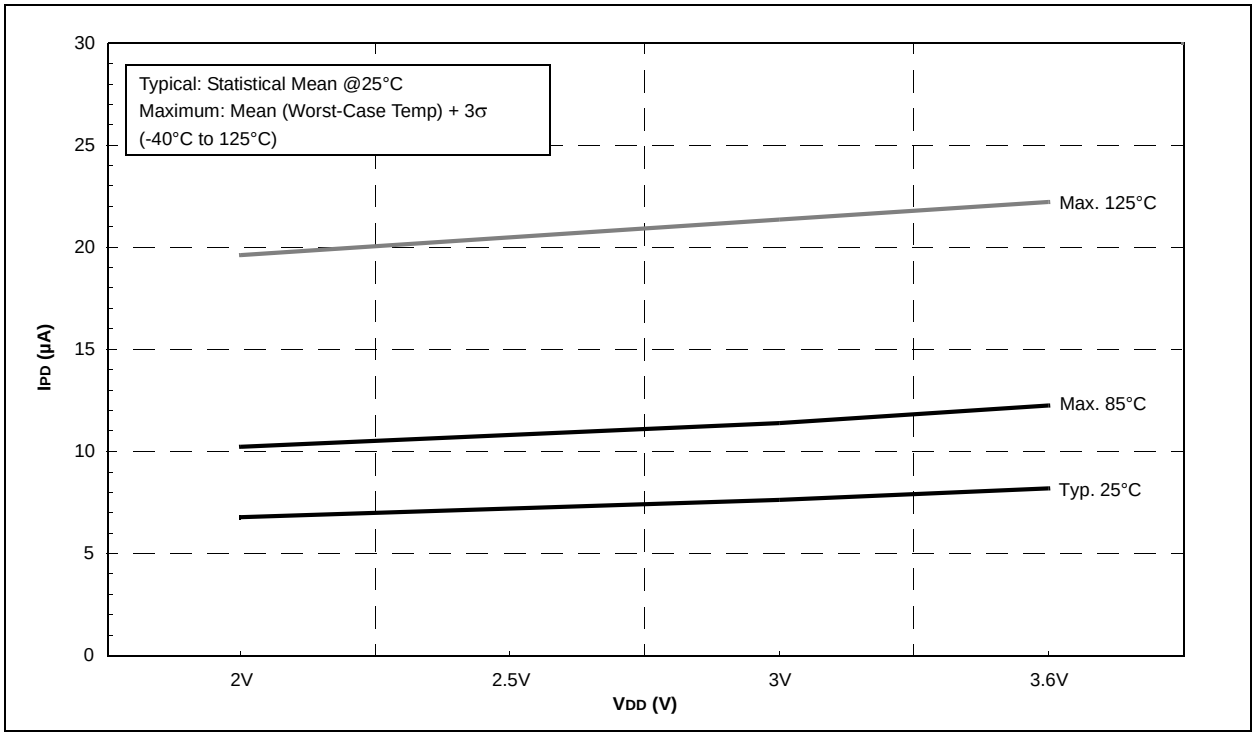


FIGURE 24-51: SCHMITT TRIGGER INPUT THRESHOLD VIN vs. VDD OVER TEMPERATURE

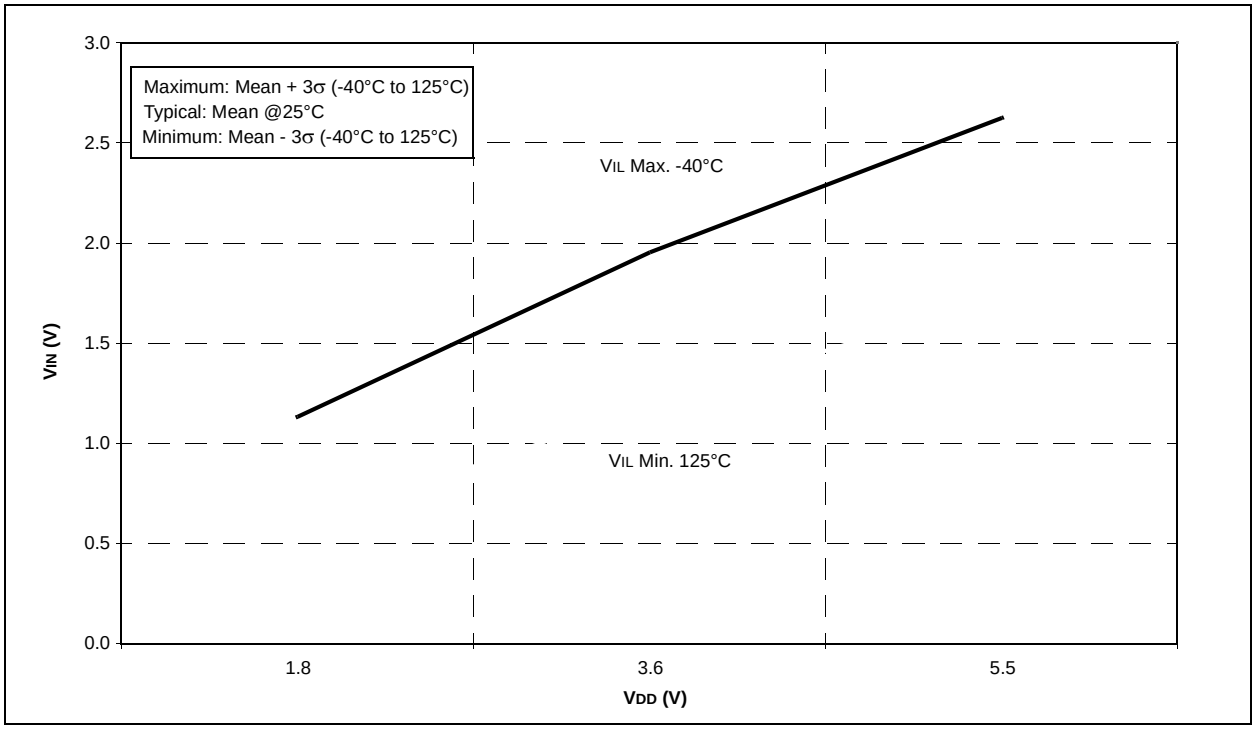
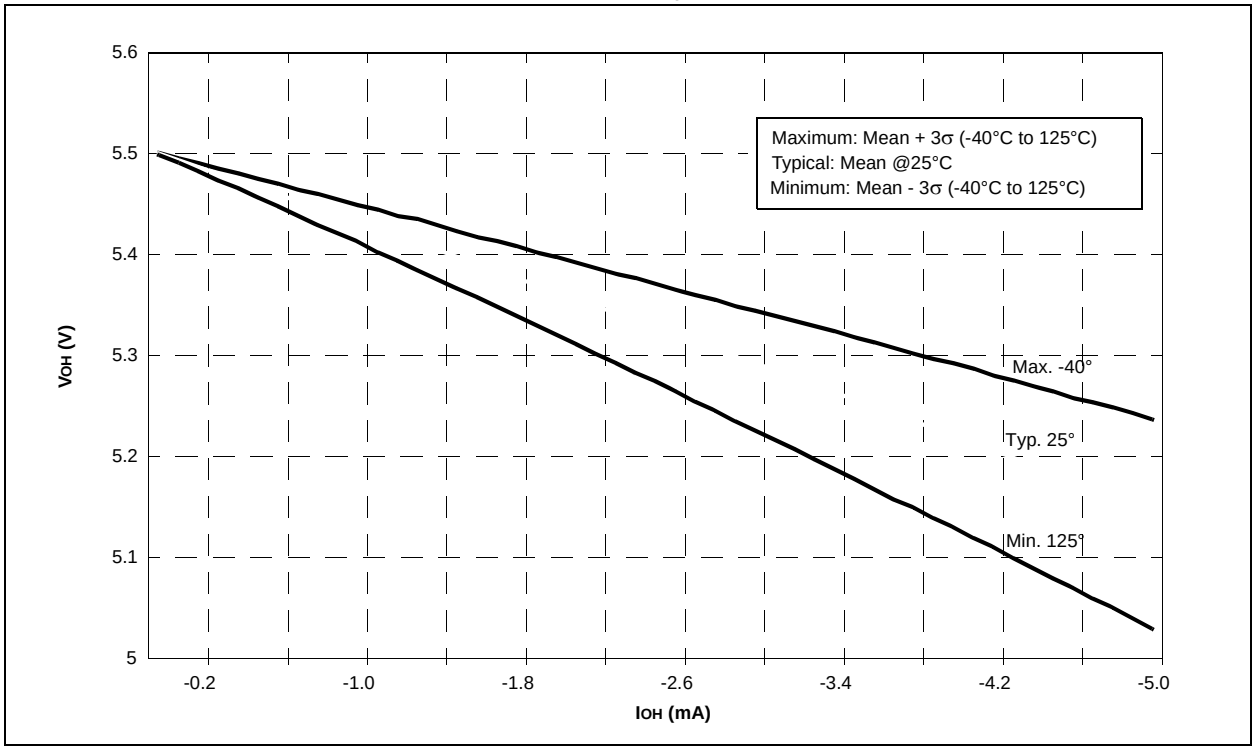
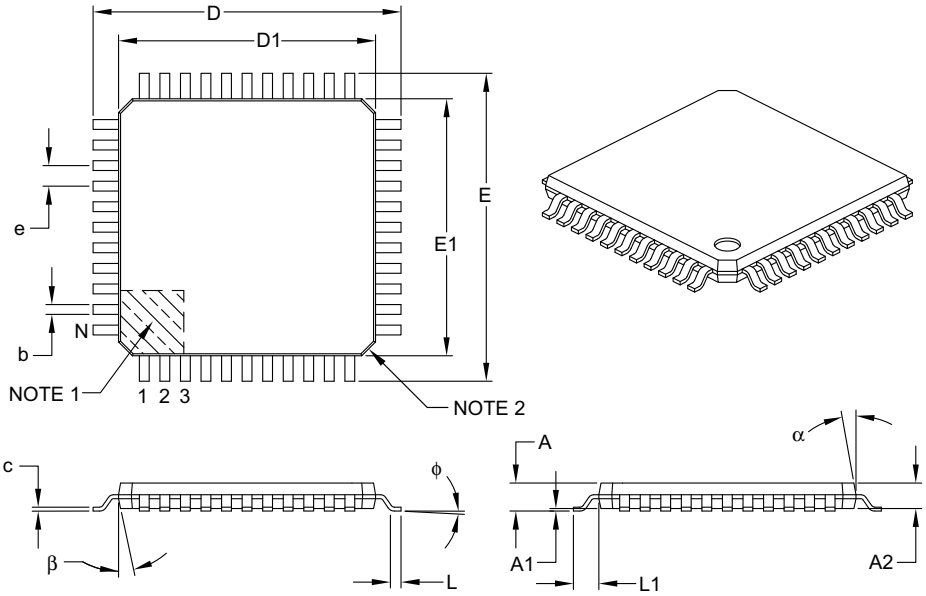


FIGURE 24-52: VOH vs. IOH OVER TEMPERATURE, VDD = 5.5V



44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	e		0.80 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B