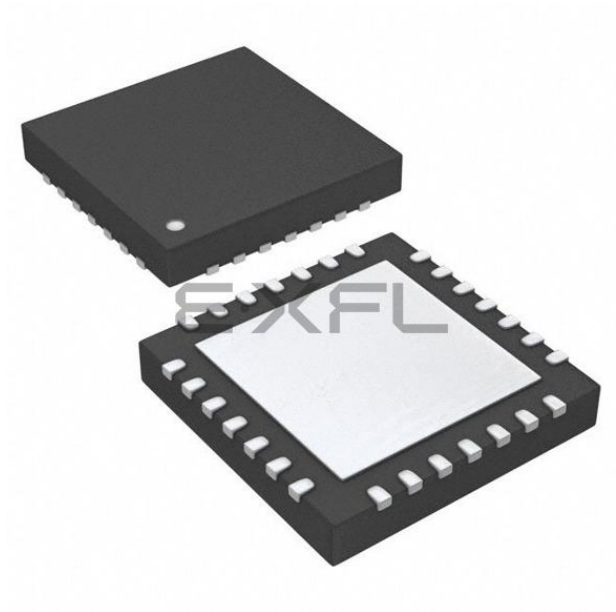

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f723-i-mv

TABLE 1: 28-PIN PDIP/SOIC/SSOP/QFN/UQFN SUMMARY (PIC16F722/723/726/PIC16LF722/723/726)

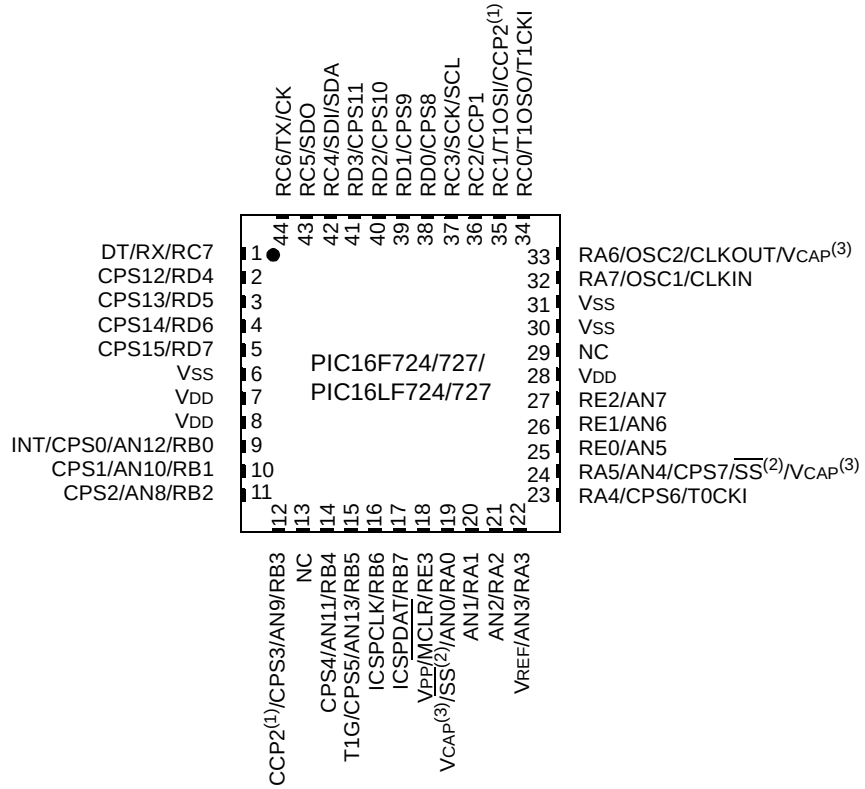
I/O	28-Pin PDIP, SOIC, SSOP	28-Pin QFN, UQFN	A/D	Cap Sensor	Timers	CCP	AUSART	SSP	Interrupt	Pull-Up	Basic
RA0	2	27	AN0	—	—	—	—	$\overline{SS}$(3)	—	—	V_{CAP}(4)
RA1	3	28	AN1	—	—	—	—	—	—	—	—
RA2	4	1	AN2	—	—	—	—	[redacted]	—	—	—
RA3	5	2	AN3/V_{REF}	—	—	—	—	—	—	—	—
RA4	6	3	—	CPS6	T0CKI	—	—	—	—	—	—
RA5	7	4	AN4	CPS7	—	—	—	$\overline{SS}$(3)	—	—	V_{CAP}(4)
RA6	10	7	—	—	—	—	—	—	—	—	OSC2/CLKOUT/V_{CAP}(4)
RA7	9	6	—	—	—	—	—	—	—	—	OSC1/CLKIN
RB0	21	18	AN12	CPS0	—	—	—	—	IOC/INT	Y	—
RB1	22	19	AN10	CPS1	—	—	—	—	IOC	Y	—
RB2	23	20	AN8	CPS2	—	—	—	—	IOC	Y	—
RB3	24	21	AN9	CPS3	—	CCP2(2)	—	—	IOC	Y	—
RB4	25	22	AN11	CPS4	—	—	—	—	IOC	Y	—
RB5	26	23	AN13	CPS5	T1G	—	—	—	IOC	Y	—
RB6	27	24	—	—	—	—	—	—	IOC	Y	ICSPCLK/ICDCLK
RB7	28	25	—	—	—	—	—	—	IOC	Y	ICSPDAT/ICDDAT
RC0	11	8	—	—	T1OSO/T1CKI	—	—	—	—	—	—
RC1	12	9	—	—	T1OSI	CCP2(2)	—	—	—	—	—
RC2	13	10	—	—	—	CCP1	—	—	—	—	—
RC3	14	11	—	—	—	—	—	SCK/SCL	—	—	—
RC4	15	12	—	—		—	—	SDI/SDA	—	—	—
RC5	16	13	—	—	—	—	—	SDO	—	—	—
RC6	17	14	—	—	—	—	TX/CK	—	—	—	—
RC7	18	15	—	—	—	—	RX/DT	—	—	—	—
RE3	1	26	—	—	—	—	—	—	—	Y(1)	$\overline{MCLR}$/V_{PP}
—	20	17	—	—	—	—	—	—	—	—	V_{DD}
—	8,19	5,16	—	—	—	—	—	—	—	—	V_{SS}

Note 1: Pull-up enabled only with external $\overline{MCLR}$ Configuration.

2: RC1 is the default pin location for CCP2. RB3 may be selected by changing the CCP2SEL bit in the APFCON register.

987(3 0 6.Tw)-16.75Tm .989335134 [illegible] 0 0 6.9-5.9(e)-16.7(d).5(o)-16.7(n).5(l)-532.(y)-3.9(.Tw)-135 10396)-1-3.ll3 8l1:

Pin Diagrams – 44-PIN QFN (PIC16F724/727/PIC16LF724/727)



Note 1: CCP2 pin location may be selected as RB3 or RC1.
2: $\overline{SS}$ pin location may be selected as RA5 or RA0.
3: PIC16F724/727 devices only.

TABLE 6-3: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
APFCON	—	—	—	—	—	—	SSSEL	CCP2SEL	---- --00	---- --00
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	xxxx xxxx
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
SSPSTAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000 0000	0000 0000
T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	—	TMR1ON	0000 00-0	uuuu uu-u
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Port C.

6.5 PORTD and TRISD Registers

PORTD is a 8-bit wide, bidirectional port. The corresponding data direction register is TRISD (Register 6-13). Setting a TRISD bit (= 1) will make the corresponding PORTD pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISD bit (= 0) will make the corresponding PORTD pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 6-4 shows how to initialize PORTD.

Reading the PORTD register (Register 6-12) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch.

The TRISD register (Register 6-13) controls the PORTD pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISD register are maintained set when using them as analog inputs. I/O pins configured as analog input always read ‘0’.

EXAMPLE 6-4: INITIALIZING PORTD

6.5.1 ANSELD REGISTER

The ANSELD register (Register 6-9) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELD bit high will cause all digital reads on the pin to be read as ‘0’ and allow analog functions on the pin to operate correctly.

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