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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f723-i-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Name	Function	Input Type	Output Type	Description
RD3/CPS11	RD3	ST	CMOS	General purpose I/O.
	CPS11	AN	—	Capacitive sensing input 11.
RD4/CPS12	RD4	ST	CMOS	General purpose I/O.
	CPS12	AN	—	Capacitive sensing input 12.
RD5/CPS13	RD5	ST	CMOS	General purpose I/O.
	CPS13	AN	—	Capacitive sensing input 13.
RD6/CPS14	RD6	ST	CMOS	General purpose I/O.
	CPS14	AN	_	Capacitive sensing input 14.
RD7/CPS15	RD7	ST	CMOS	General purpose I/O.
	CPS15	AN	_	Capacitive sensing input 15.
RE0/AN5	RE0	ST	CMOS	General purpose I/O.
	AN5	AN	—	A/D Channel 5 input.
RE1/AN6	RE1	ST	CMOS	General purpose I/O.
	AN6	AN	—	A/D Channel 6 input.
RE2/AN7	RE2	ST	CMOS	General purpose I/O.
	AN7	AN		A/D Channel 7 input.
RE3/MCLR/VPP	RE3	TTL	—	General purpose input.
	MCLR	ST	—	Master Clear with internal pull-up.
	Vpp	HV	—	Programming voltage.
VDD	Vdd	Power	—	Positive supply.
Vss	Vss	Power	—	Ground reference.
Legend: AN = Analog input or o TTL = TTL compatible in HV = High Voltage	utput CMO nput ST XTAL	S = CMO = Schm = Cryst	S compati iitt Trigger al levels	ible input or output OD = Open Drain input with CMOS levels I^2C = Schmitt Trigger input with I^2C

TABLE 1-1: PIC16(L)F722/3/4/6/7 PINOUT DESCRIPTION (CONTINUED)

Note: The PIC16F722/3/4/6/7 devices have an internal low dropout voltage regulator. An external capacitor must be connected to one of the available VCAP pins to stabilize the regulator. For more information, see **Section 5.0 "Low Dropout (LDO) Voltage Regulator**". The PIC16LF722/3/4/6/7 devices do not have the voltage regulator and therefore no external capacitor is required.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Page
Bank 1	k1										
80h ⁽²⁾	INDF	Addressing	this location	uses conten	ts of FSR to a	address data	memory (not	a physical re	gister)	xxxx xxxx	29,37
81h	OPTION_REG	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	26,37
82h ⁽²⁾	PCL	Program Co	ounter (PC) L	east Signific	ant Byte					0000 0000	28,37
83h ⁽²⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	25,37
84h ⁽²⁾	FSR	Indirect Data	a Memory Ad	ddress Point	er					xxxx xxxx	29,37
85h	TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111	51,37
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	60,37
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	70,37
88h ⁽³⁾	TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	1111 1111	78,37
89h	TRISE	_	—	_	_	TRISE3 ⁽⁶⁾	TRISE2 ⁽³⁾	TRISE1 ⁽³⁾	TRISE0 ⁽³⁾	1111	81,37
8Ah ^(1, 2)	PCLATH	_	_	_	Write Buffer	for the upper	5 bits of the F	Program Cou	nter	0 0000	28,37
8Bh ⁽²⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	44,37
8Ch	PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	45,37
8Dh	PIE2	_	—	—	_	_	_	_	CCP2IE	0	46,37
8Eh	PCON	_	_	_	_	_	_	POR	BOR	qq	27,38
8Fh	T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T <u>1GGO</u> / DONE	T1GVAL	T1GSS1	T1GSS0	0000 0x00	118,38
90h	OSCCON	_	_	IRCF1	IRCF0	ICSL	ICSS	_	_	10 qq	87,38
91h	OSCTUNE	_	_	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0	00 0000	88,38
92h	PR2	Timer2 Peri	od Register							1111 1111	120,38
93h	SSPADD ⁽⁵⁾	Synchronou	s Serial Port	(I ² C mode)	Address Regi	ister				0000 0000	169,38
93h	SSPMSK ⁽⁴⁾	Synchronou	s Serial Port	(I ² C mode)	Address Mas	k Register				1111 1111	180,38
94h	SSPSTAT	SMP	CKE	D/A	Р	S	R/W	UA	BF	0000 0000	179,38
95h	WPUB	WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0	1111 1111	61,38
96h	IOCB	IOCB7	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0	0000 0000	61,38
97h	—	Unimpleme	nted							_	—
98h	TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	147,38
99h	SPBRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	0000 0000	149,38
9Ah	-	Unimpleme	nted							_	—
9Bh	-	Unimpleme	nted							_	—
9Ch	APFCON	_	_	_	_	_	_	SSSEL	CCP2SEL	00	50,38
9Dh	FVRCON	FVRRDY	FVREN	_	_	_	_	ADFVR1	ADFVR0	d000	104,38
9Eh	_	Unimpleme	nted							—	—
9Fh	ADCON1	_	ADCS2	ADCS1	ADCS0	_	—	ADREF1	ADREF0	000000	100,38

TABLE 2-1: PIC16(L)F722/3/4/6/7 SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.

Shaded locations are unimplemented, read as '0'.

Note The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are 1: transferred to the upper byte of the program counter.

2:

These registers/bits are not implemented on PIC16F722/723/726/PIC16LF722/723/726 devices, read as '0'. 3:

Accessible only when SSPM<3:0> \pm 1001. Accessible only when SSPM<3:0> \pm 1001. This bit is always '1' as RE3 is input-only. 4:

5: 6:

Register	Address	Power-on Reset/ Brown-out Reset ⁽¹⁾	MCLR Reset/ WDT Reset	Wake-up from Sleep through Interrupt/Time out
PCON	8Eh	dd	(1,5)	uu
T1GCON	8Fh	0000 0x00	uuuu uxuu	uuuu uxuu
OSCCON	90h	10 qq	10 qq	uu qq
OSCTUNE	91h	00 0000	uu uuuu	uu uuuu
PR2	92h	1111 1111	1111 1111	uuuu uuuu
SSPADD	93h	0000 0000	0000 0000	uuuu uuuu
SSPMSK	93h	1111 1111	1111 1111	uuuu uuuu
SSPSTAT	94h	0000 0000	0000 0000	uuuu uuuu
WPUB	95h	1111 1111	1111 1111	uuuu uuuu
IOCB	96h	0000 0000	0000 0000	uuuu uuuu
TXSTA	98h	0000 -010	0000 -010	uuuu -uuu
SPBRG	99h	0000 0000	0000 0000	uuuu uuuu
APFCON	9Ch	00	00	uu
FVRCON	9Dh	q00000	q00000	uuuuuu
ADCON1	9Fh	-00000	-00000	-uuuuu
CPSCON0	108h	0 0000	0 0000	u uuuu
CPSCON1	109h	0000	0000	uuuu
PMDATL	10Ch	xxxx xxxx	xxxx xxxx	uuuu uuuu
PMADRL	10Dh	xxxx xxxx	xxxx xxxx	uuuu uuuu
PMDATH	10Eh	xx xxxx	xx xxxx	uu uuuu
PMADRH	10Fh	x xxxx	x xxxx	u uuuu
ANSELA	185h	11 1111	11 1111	uu uuuu
ANSELB	186h	11 1111	11 1111	uu uuuu
ANSELD ⁽⁶⁾	188h	1111 1111	1111 1111	uuuu uuuu
ANSELE	189h	111	111	uuu
PMCON1	18Ch	10	10	u u

TABLE 3-4: INITIALIZATION CONDITION FOR REGISTERS (CONTINUED)

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 and PIR2 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 3-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

6: PIC16F724/727/PIC16LF724/727 only.

Note

4.5.3 PIE2 REGISTER

Γ.

bit 0

The PIE2 register contains the interrupt enable bits, as shown in Register 4-3.

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 4-3: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	CCP2IE
bit 7							bit 0

Legena:			
R = Readable bit W	= Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR '1'	= Bit is set	0' = Bit is cleared	x = Bit is unknown

bit 7-1 Unimplemented: Read as '0'

CCP2IE: CCP2 Interrupt Enable bit

1 = Enables the CCP2 interrupt

0 = Disables the CCP2 interrupt

6.4 PORTC and TRISC Registers

PORTC is a 8-bit wide, bidirectional port. The corresponding data direction register is TRISC (Register 6-11). Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 6-3 shows how to initialize PORTC.

Reading the PORTC register (Register 6-10) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch.

The TRISC register (Register 6-11) controls the PORTC pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISC register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

EXAMPLE 6-3: INITIALIZING PORTC

BANKSEL	PORTC	;
CLRF	PORTC	;Init PORTC
BANKSEL	TRISC	;
MOVLW	B'00001100'	;Set RC<3:2> as inputs
MOVWF	TRISC	;and set RC<7:4,1:0>
		;as outputs

The location of the CCP2 function is controlled by the CCP2SEL bit in the APFCON register (refer to Register 6-1)

| R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| RC7 | RC6 | RC5 | RC4 | RC3 | RC2 | RC1 | RC0 |
| bit 7 | | | | | | | bit 0 |

REGISTER 6-10: PORTC: PORTC REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 RC<7:0>: PORTC General Purpose I/O Pin bits

1 = Port pin is > VIH 0 = Port pin is < VIL

REGISTER 6-11: TRISC: PORTC TRI-STATE REGISTER

| R/W-1 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| TRISC7 | TRISC6 | TRISC5 | TRISC4 | TRISC3 | TRISC2 | TRISC1 | TRISC0 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **TRISC<7:0>:** PORTC Tri-State Control bits 1 = PORTC pin configured as an input (tri-stated) 0 = PORTC pin configured as an output









REGISTER	9-2. ADCO		IT NOL KEGI	SIEKI							
U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0				
_	ADCS2	ADCS1	ADCS0	—	_	ADREF1	ADREF0				
bit 7							bit 0				
Legend:											
R = Readable	bit	W = Writable bi	t	U = Unimplem	ented bit, read as	s 'O'					
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is clea	red	x = Bit is unkno	own				
bit 7	Unimplemente	ed: Read as '0'									
bit 6-4	ADCS<2:0>: A	ADCS<2:0>: A/D Conversion Clock Select bits									
	000 = Fosc/2	000 = Fosc/2									
	001 = Fosc/8	001 = Fosc/8									
	010 = Fosc/32	010 = Fosc/32									
	011 = FRC (clo	011 = FRC (clock supplied from a dedicated RC oscillator)									
	100 = Fosc/4	100 = Fosc/4									
	101 = FOSC/16	101 = FOSC/16									
	110 = FOSC/64	110 = FOSC/64									
		ock supplied nom	a dedicated RC	oscillator)							
bit 3-2	Unimplemente	ed: Read as '0'									
bit 1-0	ADREF<1:0>:	ADREF<1:0>: Voltage Reference Configuration bits									
	0x = VREF is c	connected to VDD	1								
	10 = VREF is c	connected to exte	rnal VREF (RA3/	(AN3)							
	11 = VREF is 0	connected to inte	rnal Fixed Voltag	ge Reference							

REGISTER 9-2: ADCON1: A/D CONTROL REGISTER 1

REGISTER 9-3: ADRES: ADC RESULT REGISTER

| R/W-x |
|--------|--------|--------|--------|--------|--------|--------|--------|
| ADRES7 | ADRES6 | ADRES5 | ADRES4 | ADRES3 | ADRES2 | ADRES1 | ADRES0 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ADRES<7:0>**: ADC Result Register bits 8-bit conversion result.

12.1 Timer1 Operation

The Timer1 module is a 16-bit incrementing counter which is accessed through the TMR1H:TMR1L register pair. Writes to TMR1H or TMR1L directly update the counter.

When used with an internal clock source, the module is a timer and increments on every instruction cycle. When used with an external clock source, the module can be used as either a timer or counter and increments on every selected edge of the external source.

Timer1 is enabled by configuring the TMR1ON and TMR1GE bits in the T1CON and T1GCON registers, respectively. Table 12-1 displays the Timer1 enable selections.

TABLE 12-1: TIMER1 ENABLE SELECTIONS

TMR10N	TMR1GE	Timer1 Operation
0	0	Off
0	1	Off
1	0	Always On
1	1	Count Enabled

12.2 Clock Source Selection

The TMR1CS<1:0> and T1OSCEN bits of the T1CON register are used to select the clock source for Timer1. Table 12-2 displays the clock source selections.

12.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected, the TMR1H:TMR1L register pair will increment on multiples of Fosc as determined by the Timer1 prescaler.

12.2.2 EXTERNAL CLOCK SOURCE

When the external clock source is selected, the Timer1 module may work as a timer or a counter.

When enabled to count, Timer1 is incremented on the rising edge of the external clock input T1CKI or the capacitive sensing oscillator signal. Either of these external clock sources can be synchronized to the microcontroller system clock or they can run asynchronously.

When used as a timer with a clock oscillator, an external 32.768 kHz crystal can be used in conjunction with the dedicated internal oscillator circuit.

Note:	In Counter mode, a falling edge must be
	registered by the counter prior to the first
	incrementing rising edge after any one or
	more of the following conditions:

- Timer1 enabled after POR reset
- Write to TMR1H or TMR1L
- Timer1 is disabled
- Timer1 is disabled (TMR1ON = 0) when T1CKI is high then Timer1 is enabled (TMR1ON= 1) when T1CKI is low.

TMR1CS1	TMR1CS0	T10SCEN	Clock Source
0	1	x	System Clock (FOSC)
0	0	x	Instruction Clock (Fosc/4)
1	1	x	Capacitive Sensing Oscillator
1	0	0	External Clocking on T1CKI Pin
1	0	1	Oscillator Circuit on T1OSI/T1OSO Pins

TABLE 12-2: CLOCK SOURCE SELECTIONS

16.1.2 AUSART ASYNCHRONOUS RECEIVER

The Asynchronous mode is typically used in RS-232 systems. The receiver block diagram is shown in Figure 16-2. The data is received on the RX/DT pin and drives the data recovery block. The data recovery block is actually a high-speed shifter operating at 16 times the baud rate, whereas the serial Receive Shift Register (RSR) operates at the bit rate. When all eight or nine bits of the character have been shifted in, they are immediately transferred to a two character First-In First-Out (FIFO) memory. The FIFO buffering allows reception of two complete characters and the start of a third character before software must start servicing the AUSART receiver. The FIFO and RSR registers are not directly accessible by software. Access to the received data is via the RCREG register.

16.1.2.1 Enabling the Receiver

The AUSART receiver is enabled for asynchronous operation by configuring the following three control bits:

- CREN = 1
- SYNC = 0
- SPEN = 1

All other AUSART control bits are assumed to be in their default state.

Setting the CREN bit of the RCSTA register enables the receiver circuitry of the AUSART. Clearing the SYNC bit of the TXSTA register configures the AUSART for asynchronous operation. Setting the SPEN bit of the RCSTA register enables the AUSART and automatically configures the RX/DT I/O pin as an input.

Note:	When the SPEN bit is set the TX/CK I/O
	pin is automatically configured as an
	output, regardless of the state of the
	corresponding TRIS bit and whether or
	not the AUSART transmitter is enabled.
	The PORT latch is disconnected from the
	output driver so it is not possible to use the
	TX/CK pin as a general purpose output.

16.1.2.2 Receiving Data

The receiver data recovery circuit initiates character reception on the falling edge of the first bit. The first bit, also known as the Start bit, is always a zero. The data recovery circuit counts one-half bit time to the center of the Start bit and verifies that the bit is still a zero. If it is not a zero then the data recovery circuit aborts character reception, without generating an error, and resumes looking for the falling edge of the Start bit. If the Start bit zero verification succeeds then the data recovery circuit counts a full bit time to the center of the next bit. The bit is then sampled by a majority detect circuit and the resulting '0' or '1' is shifted into the RSR. This repeats until all data bits have been sampled and shifted into the RSR. One final bit time is measured and the level sampled. This is the Stop bit, which is always a '1'. If the data recovery circuit samples a '0' in the Stop bit position then a framing error is set for this character, otherwise the framing error is cleared for this character. Refer to Section 16.1.2.4 "Receive Framing Error" for more information on framing errors.

Immediately after all data bits and the Stop bit have been received, the character in the RSR is transferred to the AUSART receive FIFO and the RCIF interrupt flag bit of the PIR1 register is set. The top character in the FIFO is transferred out of the FIFO by reading the RCREG register.

Note: If the receive FIFO is overrun, no additional characters will be received until the overrun condition is cleared. Refer to Section 16.1.2.5 "Receive Overrun Error" for more information on overrun errors.

16.1.2.3 Receive Interrupts

The RCIF interrupt flag bit of the PIR1 register is set whenever the AUSART receiver is enabled and there is an unread character in the receive FIFO. The RCIF interrupt flag bit is read-only, it cannot be set or cleared by software.

RCIF interrupts are enabled by setting all of the following bits:

- RCIE interrupt enable bit of the PIE1 register
- PEIE peripheral interrupt enable bit of the INTCON register
- GIE global interrupt enable bit of the INTCON register

The RCIF interrupt flag bit of the PIR1 register will be set when there is an unread character in the FIFO, regardless of the state of interrupt enable bits.

16.1.2.4 Receive Framing Error

Each character in the receive FIFO buffer has a corresponding framing error Status bit. A framing error indicates that a Stop bit was not seen at the expected time. The framing error status is accessed via the FERR bit of the RCSTA register. The FERR bit represents the status of the top unread character in the receive FIFO. Therefore, the FERR bit must be read before reading the RCREG.

The FERR bit is read-only and only applies to the top unread character in the receive FIFO. A framing error (FERR = 1) does not preclude reception of additional characters. It is not necessary to clear the FERR bit. Reading the next character from the FIFO buffer will advance the FIFO to the next character and the next corresponding framing error.

The FERR bit can be forced clear by clearing the SPEN bit of the RCSTA register which resets the AUSART. Clearing the CREN bit of the RCSTA register does not affect the FERR bit. A framing error by itself does not generate an interrupt.

Note:	If all receive characters in the receive
	FIFO have framing errors, repeated reads
	of the RCREG will not clear the FERR bit.

16.1.2.5 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before the FIFO is accessed. When this happens the OERR bit of the RCSTA register is set. The characters already in the FIFO buffer can be read but no additional characters will be received until the error is cleared. The error must be cleared by either clearing the CREN bit of the RCSTA register or by setting the AUSART by clearing the SPEN bit of the RCSTA register.

16.1.2.6 Receiving 9-bit Characters

The AUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set the AUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREG.

16.1.2.7 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RCSTA register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the ninth data bit set will be transferred to the receive FIFO buffer, thereby setting the RCIF interrupt bit of the PIR1 register. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.

17.1.2.4 Slave Select Operation

The \overline{SS} pin allows Synchronous Slave mode operation. The SPI must be in Slave mode with \overline{SS} pin control enabled (SSPM<3:0> = 0100). The associated TRIS bit for the \overline{SS} pin must be set, making \overline{SS} an input.

In Slave Select mode, when:

- SS = 0, The device operates as specified in Section 17.1.2 "Slave Mode".
- $\overline{SS} = 1$, The SPI module is held in Reset and the SDO pin will be tri-stated.
 - Note 1: When the SPI is in Slave mode with \overline{SS} pin control enabled (SSPM<3:0> = 0100), the SPI module will reset if the \overline{SS} pin is driven high.
 - 2: If the SPI is used in Slave mode with CKE set, the SS pin control must be enabled.

When the SPI module resets, the bit counter is cleared to '0'. This can be done by either forcing the SS pin to a high level or clearing the SSPEN bit. Figure 17-6 shows the timing waveform for such a synchronization event.

Note:	SSPSR must be reinitialized by writing to
	the SSPBUF register before the data can
	be clocked out of the slave again.

17.1.2.5 Sleep in Slave Mode

While in Sleep mode, the slave can transmit/receive data. The SPI Transmit/Receive Shift register operates asynchronously to the device on the externally supplied clock source. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all eight bits have been received, the SSP Interrupt Flag bit will be set and if enabled, will wake the device from Sleep.



							c v
SCK (CKP = 0 (%8 x 8)							
SCK (CKP = 1							· · · · · · · · · · · · · · · · · · ·
VATALA 40 2658-2608			se the be	PSR must be rei SSPBUF registe plocked out of the	nitistized by a before the a slave again	i writing to data can	()))))))
S(X)							**************************************
SDI (88862 = 0)	bit 7				\rightarrow		
Input Sample (2002 = 0)	<u> </u>		2		<u> </u>		<u></u>
Sisteri Interrupt Pag	: :	8 8 		5 5 5 7	; 		
8557934.40 9599939 <u>5</u>					····· 🖗 ·····		//.





MOVF	Move f
Syntax:	[label] MOVF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	(f) \rightarrow (dest)
Status Affected:	Z
Description:	The contents of register f is moved to a destination dependent upon the status of d. If $d = 0$, destination is W register. If $d = 1$, the destination is file register f itself. $d = 1$ is useful to test a file register since status flag Z is affected.
Words:	1
Cycles:	1
Example:	MOVF FSR, 0
	After Instruction W = value in FSR register Z = 1

MOVWF	Move W to f
Syntax:	[<i>label</i>] MOVWF f
Operands:	$0 \leq f \leq 127$
Operation:	$(W) \rightarrow (f)$
Status Affected:	None
Description:	Move data from W register to register 'f'.
Words:	1
Cycles:	1
Example:	MOVW OPTION F
	Before Instruction
	OPTION = 0xFF
	W = 0x4F
	After Instruction
	OPTION = 0X4F
	vv = 0x4F

MOVLW	Move literal to W
Syntax:	[<i>label</i>] MOVLW k
Operands:	$0 \le k \le 255$
Operation:	$k \rightarrow (W)$
Status Affected:	None
Description:	The 8-bit literal 'k' is loaded into W register. The "don't cares" will assemble as '0's.
Words:	1
Cycles:	1
Example:	MOVLW 0x5A
	After Instruction W = 0x5A

NOP	No Operation					
Syntax:	[label] NOP					
Operands:	None					
Operation:	No operation					
Status Affected:	None					
Description:	No operation.					
Words:	1					
Cycles:	1					
Example:	NOP					

23.2 DC Characteristics: PIC16(L)F722/3/4/6/7-I/E (Industrial, Extended)

PIC16LF722/3/4/6/7		$\begin{array}{l} \mbox{Standard Operating Conditions (unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for extended} \end{array}$									
PIC16F7	22/3/4/6/7	$ \begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for industrial} \\ -40^\circ C \leq TA \leq +125^\circ C \mbox{ for extended} \end{array} $									
Param	Device	Min	Tynt	Max	Unite		Conditions				
No.	Characteristics		iypi	max.	Onto	Vdd	Note				
Supply Current (IDD) ^(1, 2)											
D009	LDO Regulator	-	350	_	μA	_	HS, EC OR INTOSC/INTOSCIO (8-16 MHz) Clock modes with all VCAP pins disabled				
			50		μA		All VCAP pins disabled				
		—	30		μA		VCAP enabled on RA0, RA5 or RA6				
		—	5	—	μΑ	—	LP Clock mode and Sleep (requires FVR and BOR to be disabled)				
D010		_	7.0	12	μA	1.8	Fosc = 32 kHz				
		—	9.0	14	μΑ	3.0	LP Oscillator mode (Note 4), -40°C \leq TA \leq +85°C				
D010		_	11	20	μΑ	1.8	Fosc = 32 kHz				
			14	22	μA	3.0	LP Oscillator mode (Note 4), $-40^{\circ}C < T_A < +85^{\circ}C$				
			15	24	μΑ	5.0					
D011		—	7.0	12	μA	1.8	Fosc = 32 kHz				
		_	9.0	18	μΑ	3.0	LP Oscillator mode -40°C \leq TA \leq +125°C				
D011			11	21	μA	1.8	Fosc = 32 kHz				
			14	25	μΑ	3.0	LP Oscillator mode (Note 4) $-40^{\circ}C < T_A < +125^{\circ}C$				
			15	27	μA	5.0					
D011		_	110	150	μΑ	1.8	Fosc = 1 MHz				
		-	150	215	μΑ	3.0	X1 Oscillator mode				
D011			120	175	μA	1.8	Fosc = 1 MHz				
			180	250	μΑ	3.0					
D 040		_	240	300	μA	5.0					
D012			230	300	μA	1.8	FOSC = 4 MHz XT Oscillator mode				
Data		-	400	600	μA	3.0					
D012			250	350	μΑ	1.8	XT Oscillator mode (Note 5)				
			420	750	μΑ	3.0	,				
D013		-	125	180	μΑ	1.9	Eose - 1 MHz				
0013			230	270	μΑ	3.0	EC Oscillator mode				
D013			150	205	μΑ	1.8	Fosc = 1 MHz				
2010			225	320	μΑ	3.0	EC Oscillator mode (Note 5)				
			250	410	μΑ	5.0					
			200	410	μΛ	0.0					

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ.

4: FVR and BOR are disabled.

5: 0.1 μF capacitor on VCAP (RA0).





FIGURE 24-33: PIC16F722/3/4/6/7 BOR IPD vs. VDD, VCAP = 0.1 µF















FIGURE 24-65: PIC16F722/3/4/6/7 CAP SENSOR HYSTERESIS, POWER MODE = HIGH





28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS				
Dim	ension Limits	MIN	NOM	MAX		
Number of Pins	N	28				
Pitch	е	0.40 BSC				
Overall Height	А	0.45	0.50	0.55		
Standoff	A1	0.00	0.02	0.05		
Contact Thickness	A3	0.127 REF				
Overall Width	E	4.00 BSC				
Exposed Pad Width	E2	2.55	2.65	2.75		
Overall Length	D	4.00 BSC				
Exposed Pad Length	D2	2.55	2.65	2.75		
Contact Width	b	0.15	0.20	0.25		
Contact Length	L	0.30	0.40	0.50		
Contact-to-Exposed Pad	K	0.20	-	-		

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated.
- 3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-152A Sheet 2 of 2