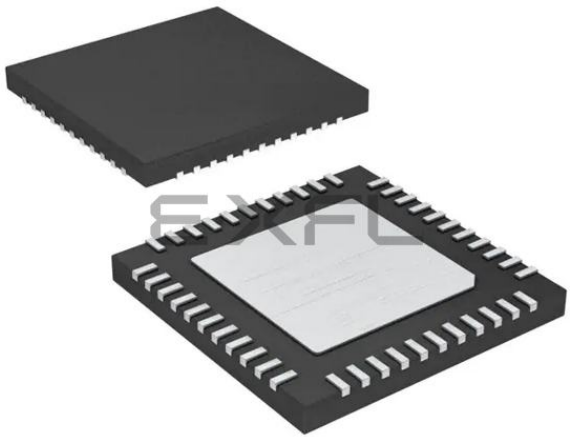

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Core Size	8-Bit
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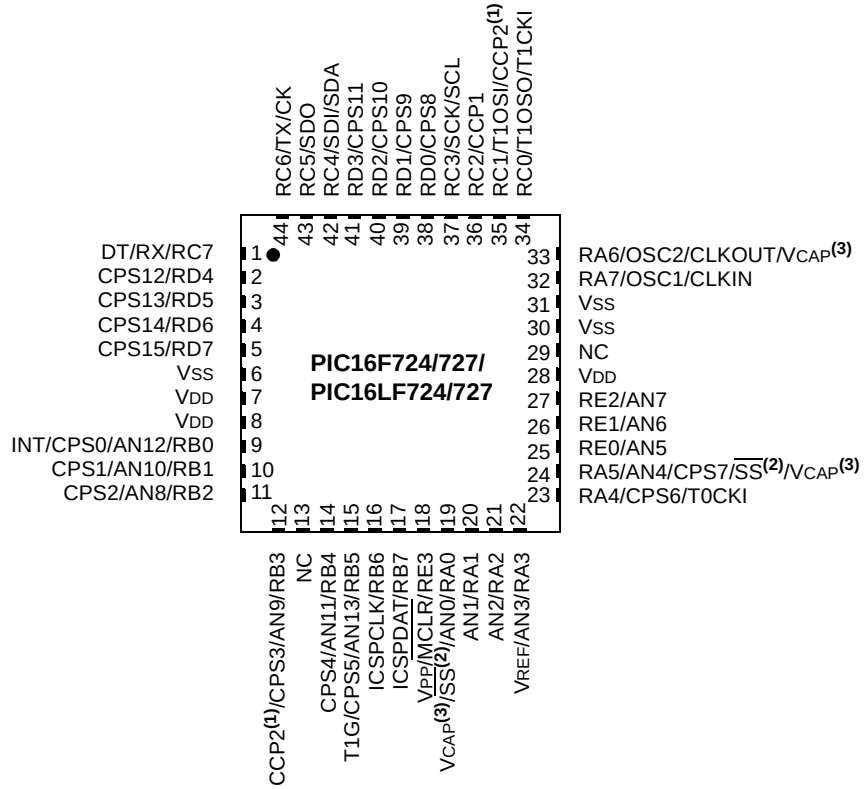
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 14x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f724-i-ml

Pin Diagrams – 44-PIN QFN (PIC16F724/727/PIC16LF724/727)



Note 1: CCP2 pin location may be selected as RB3 or RC1.
2: $\overline{SS}$ pin location may be selected as RA5 or RA0.
3: PIC16F724/727 devices only.

FIGURE 2-4: PIC16F722/LF722 SPECIAL FUNCTION REGISTERS

Bank 0	File Address	Bank 1	File Address	Bank 2	File Address	Bank 3	File Address
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION	81h	TMR0	101h	OPTION	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h	ANSELA	185h
PORTB	06h	TRISB	86h		106h	ANSELB	186h
PORTC	07h	TRISC	87h		107h		187h
	08h		88h	CPSCON0	108h		188h
PORTE	09h	TRISE	89h	CPSCON1	109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	PMDATL	10Ch	PMCON1	18Ch
PIR2	0Dh	PIE2	8Dh	PMADRL	10Dh	Reserved	18Dh
TMR1L	0Eh	PCON	8Eh	PMDATH	10Eh	Reserved	18Eh
TMR1H	0Fh	T1GCON	8Fh	PMADRH	10Fh	Reserved	18Fh
T1CON	10h	OSCCON	90h		110h		190h
TMR2	11h	OSCTUNE	91h		111h		191h
T2CON	12h	PR2	92h		112h		192h
SSPBUF	13h	SSPADD/SSPMSK	93h		113h		193h
SSPCON	14h	SSPSTAT	94h		114h		194h
CCPR1L	15h	WPUB	95h		115h		195h
CCPR1H	16h	IOCB	96h		116h		196h
CCP1CON	17h		97h		117h		197h
RCSTA	18h	TXSTA	98h		118h		198h
TXREG	19h	SPBRG	99h		119h		199h
RCREG	1Ah		9Ah		11Ah		19Ah
CCPR2L	1Bh		9Bh		11Bh		19Bh
CCPR2H	1Ch	APFCON	9Ch		11Ch		19Ch
CCP2CON	1Dh	FVRCON	9Dh		11Dh		19Dh
ADRES	1Eh		9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
	20h		A0h		120h		1A0h
General Purpose Register 96 Bytes		General Purpose Register 32 Bytes	BFh				
			C0h				
			EFh		16Fh		1EFh
			F0h		170h		1F0h
		Accesses 70h-7Fh		Accesses 70h-7Fh		Accesses 70h-7Fh	
	7Fh		FFh		17Fh		1FFh

Legend: = Unimplemented data memory locations, read as '0'.
* = Not a physical register.

FIGURE 2-5: PIC16F723/LF723 AND PIC16F724/LF724 SPECIAL FUNCTION REGISTERS

	Bank 0		Bank 1		Bank 2		Bank 3	
File Address								
	Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
	TMR0	01h	OPTION	81h	TMR0	101h	OPTION	181h
	PCL	02h	PCL	82h	PCL	102h	PCL	182h
	STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
	FSR	04h	FSR	84h	FSR	104h	FSR	184h
	PORTA	05h	TRISA	85h		105h	ANSELA	185h
	PORTB	06h	TRISB	86h		106h	ANSELB	186h
	PORTC	07h	TRISC	87h		107h		187h
	PORTD(1)	08h	TRISD(1)	88h	CPSCON0	108h	ANSELD(1)	188h
	PORTE	09h	TRISE	89h	CPSCON1	109h	ANSELE(1)	189h
	PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
	INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
	PIR1	0Ch	PIE1	8Ch	PMDATL	10Ch	PMCON1	18Ch
	PIR2	0Dh	PIE2	8Dh	PMADRL	10Dh	Reserved	18Dh
	TMR1L	0Eh	PCON	8Eh	PMDATH	10Eh	Reserved	18Eh
	TMR1H	0Fh	T1GCON	8Fh	PMADRH	10Fh	Reserved	18Fh
	T1CON	10h	OSCCON	90h		110h		190h
	TMR2	11h	OSCTUNE	91h		111h		191h
	T2CON	12h	PR2	92h		112h		192h
	SSPBUF	13h	SSPADD/SSPMSK	93h		113h		193h
	SSPCON	14h	SSPSTAT	94h		114h		194h
	CCPR1L	15h	WPUB	95h		115h		195h
	CCPR1H	16h	IOCB	96h		116h		196h
	CCP1CON	17h		97h		117h		197h
	RCSTA	18h	TXSTA	98h		118h		198h
	TXREG	19h	SPBRG	99h		119h		199h
	RCREG	1Ah		9Ah		11Ah		19Ah
	CCPR2L	1Bh		9Bh		11Bh		19Bh
	CCPR2H	1Ch	APFCON	9Ch		11Ch		19Ch
	CCP2CON	1Dh	FVRCON	9Dh		11Dh		19Dh
	ADRES	1Eh		9Eh		11Eh		19Eh
	ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
	General Purpose Register 96 Bytes	20h – 7Fh	General Purpose Register 80 Bytes	A0h – EFh	General Purpose Register 16 Bytes	120h – 12Fh		1A0h – 1EFh
						130h – 16Fh		
			Accesses 70h-7Fh	F0h – FFh	Accesses 70h-7Fh	170h – 17Fh	Accesses 70h-7Fh	1F0h – 1FFh

Legend: = Unimplemented data memory locations, read as '0'.
* = Not a physical register.

Note 1: PORTD, TRISD, ANSELD and ANSELE are not implemented on the PIC16F723/LF723, read as '0'

TABLE 2-1: PIC16(L)F722/3/4/6/7 SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Page
Bank 2											
100h(2)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	29,37
101h	TMR0	Timer0 Module Register								xxxx xxxx	105,37
102h(2)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	28,37
103h(2)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	25,37
104h(2)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	29,37
105h	—	Unimplemented								—	—
106h	—	Unimplemented								—	—
107h	—	Unimplemented								—	—
108h	CPSCON0	CPSON	—	—	—	CPSRNG1	CPSRNG0	CPSOUT	T0XCS	0--- 0000	126,38
109h	CPSCON1	—	—	—	—	CPSCH3	CPSCH2	CPSCH1	CPSCH0	---- 0000	127,38
10Ah(1, 2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	28,37
10Bh(2)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	44,37
10Ch	PMDATL	Program Memory Read Data Register Low Byte								xxxx xxxx	181,38
10Dh	PMADRL	Program Memory Read Address Register Low Byte								xxxx xxxx	181,38
10Eh	PMDATH	—	—	Program Memory Read Data Register High Byte						--xx xxxx	181,38
10Fh	PMADRH	—	—	—	Program Memory Read Address Register High Byte					---x xxxx	181,38
Bank 3											
180h(2)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	29,37
181h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	26,37
182h(2)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	28,37
183h(2)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	25,37
184h(2)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	29,37
185h	ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	--11 1111	52,38
186h	ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	--11 1111	61,38
187h	—	Unimplemented								—	—
188h	ANSELD	ANSD7	ANSD6	ANSD5	ANSD4	ANSD3	ANSD2	ANSD1	ANSD0	1111 1111	78,38
189h(3)	ANSELE	—	—	—	—	—	ANSE2	ANSE1	ANSE0	---- -111	82,38
18Ah(1, 2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	28,37
18Bh(2)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	44,37
18Ch	PMCON1	Reserved	—	—	—	—	—	—	RD	1--- ---0	182,38
18Dh	—	Unimplemented								—	—
18Eh	—	Unimplemented								—	—
18Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter.

2: These registers can be addressed from any bank.

3: These registers/bits are not implemented on PIC16F722/723/726/PIC16LF722/723/726 devices, read as '0'.

4: Accessible only when SSPM<3:0> = 1001.

5: Accessible only when SSPM<3:0> ≠ 1001.

6: This bit is always '1' as RE3 is input-only.

TABLE 3-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	0000h	0001 1xxx	---- --0x
$\overline{\text{MCLR}}$ Reset during normal operation	0000h	000u uuuu	---- --uu
$\overline{\text{MCLR}}$ Reset during Sleep	0000h	0001 0uuu	---- --uu
WDT Reset	0000h	0000 uuuu	---- --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu
Brown-out Reset	0000h	0001 1xxx	---- --10
Interrupt Wake-up from Sleep	PC + 1(1)	uuu1 0uuu	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and Global Interrupt Enable bit, GIE, is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

TABLE 3-6: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets(1)
STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu
PCON	—	—	—	—	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	---- --qq	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition. Shaded cells are not used by Resets.

Note 1: Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.

4.5.5 PIR2 REGISTER

The PIR2 register contains the interrupt flag bits, as shown in Register 4-5.

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 4-5: PIR2: PERIPHERAL INTERRUPT REQUEST REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	CCP2IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-1 **Unimplemented:** Read as '0'

bit 0 **CCP2IF:** CCP2 Interrupt Flag bit

Capture Mode:

1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred

Compare Mode:

1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred

PWM mode:

Unused in this mode

TABLE 4-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
OPTION_REG	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIE2	—	—	—	—	—	—	—	CCP2IE	---- ---0	---- ---0
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIR2	—	—	—	—	—	—	—	CCP2IF	---- ---0	---- ---0

Legend: - = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Capture, Compare and PWM.

6.3.4 PIN DESCRIPTIONS AND DIAGRAMS

Each PORTB pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the SSP, I^2C or interrupts, refer to the appropriate section in this data sheet.

6.3.4.1 RB0/AN12/CPS0/INT

Figure 6-7 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a capacitive sensing input
- an external edge triggered interrupt

6.3.4.2 RB1/AN10/CPS1

Figure 6-8 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a capacitive sensing input

6.3.4.3 RB2/AN8/CPS2

Figure 6-8 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a capacitive sensing input

6.3.4.4 RB3/AN9/CPS3/CCP2

Figure 6-9 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a capacitive sensing input
- a Capture 2 input, Compare 2 output, and PWM2 output

Note:	CCP2 pin location may be selected as RB3 or RC1.

6.3.4.5 RB4/AN11/CPS4

Figure 6-8 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a capacitive sensing input

6.3.4.6 RB5/AN13/CPS5/T1G

Figure 6-10 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a capacitive sensing input
- a Timer1 gate input

6.3.4.7 RB6/ICSPCLK

Figure 6-11 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- In-Circuit Serial Programming clock

6.3.4.8 RB7/ICSPDAT

Figure 6-12 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- In-Circuit Serial Programming data

FIGURE 6-19: BLOCK DIAGRAM OF RC6

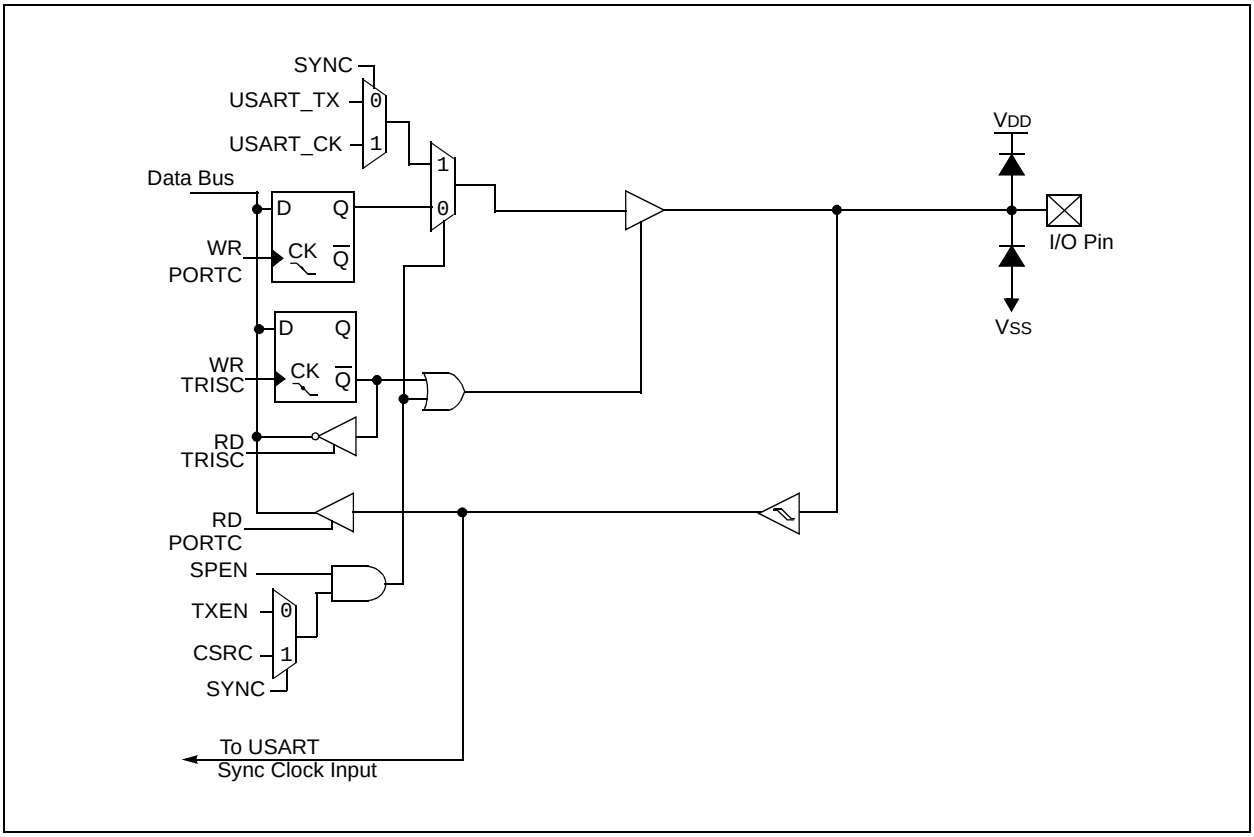
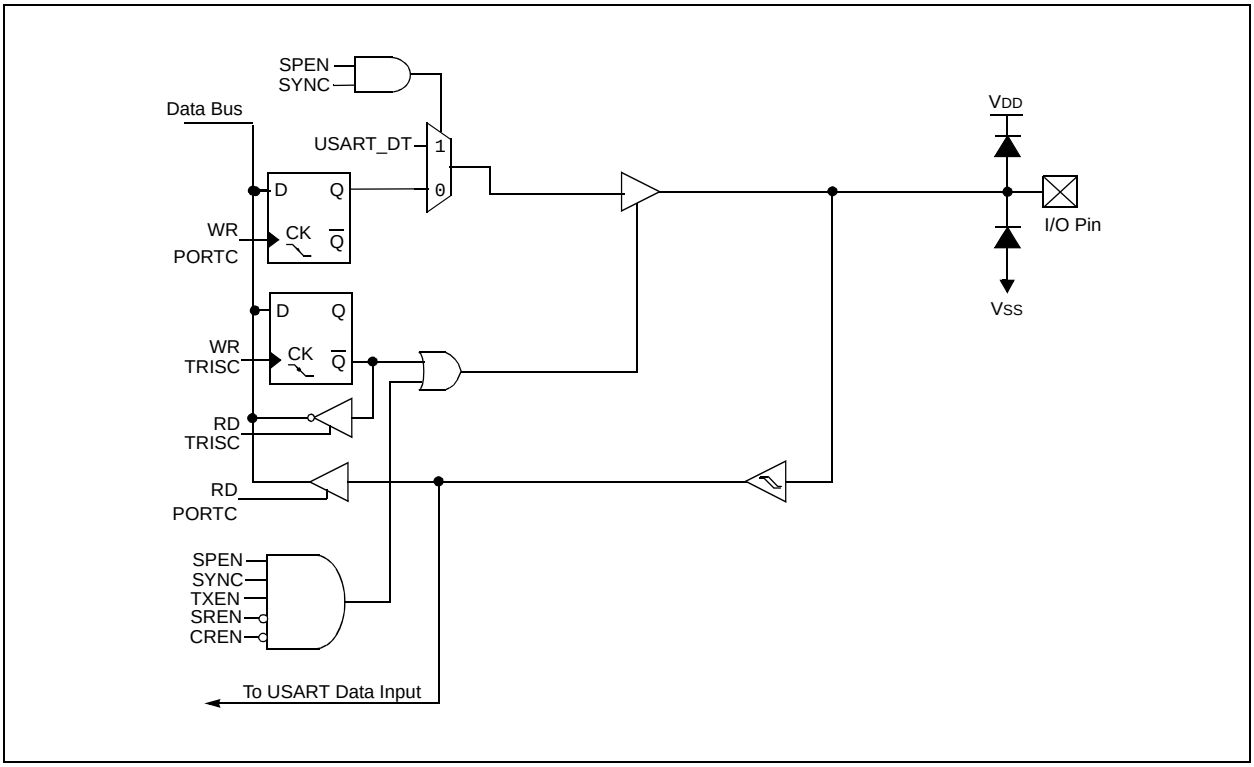


FIGURE 6-20: BLOCK DIAGRAM OF RC7



9.1 ADC Configuration

When configuring and using the ADC, the following functions must be considered:

- Port configuration
- Channel selection
- ADC voltage reference selection
- ADC conversion clock source
- Interrupt control
- Results formatting

9.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRIS and ANSEL bits. Refer to **Section 6.0 "I/O Ports"** for more information.

Note:	Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.

9.1.2 CHANNEL SELECTION

The CHS bits of the ADCON0 register determine which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion. Refer to **Section 9.2 "ADC Operation"** for more information.

9.1.3 ADC VOLTAGE REFERENCE

The ADREF bits of the ADCON1 register provides control of the positive voltage reference. The positive voltage reference can be either V_{DD}, an external voltage source or the internal Fixed Voltage Reference. The negative voltage reference is always connected to the ground reference. See **Section 10.0 "Fixed Voltage Reference"** for more details on the Fixed Voltage Reference.

9.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS bits of the ADCON1 register. There are seven possible clock options:

- $F_{OSC}/2$
- $F_{OSC}/4$
- $F_{OSC}/8$
- $F_{OSC}/16$
- $F_{OSC}/32$
- $F_{OSC}/64$
- F_{RC} (dedicated internal oscillator)

The time to complete one bit conversion is defined as T_{AD}. One full 8-bit conversion requires 10 T_{AD} periods as shown in Figure 9-2.

For correct conversion, the appropriate T_{AD} specification must be met. Refer to the A/D conversion requirements in **Section 23.0 "Electrical Specifications"** for more information. Table 9-1 gives examples of appropriate ADC clock selections.

Note:	Unless using the F_{RC}, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.

15.3 PWM Mode

The PWM mode generates a Pulse-Width Modulated signal on the CCPx pin. The duty cycle, period and resolution are determined by the following registers:

- PR2
- T2CON
- CCPRxL
- CCPxCON

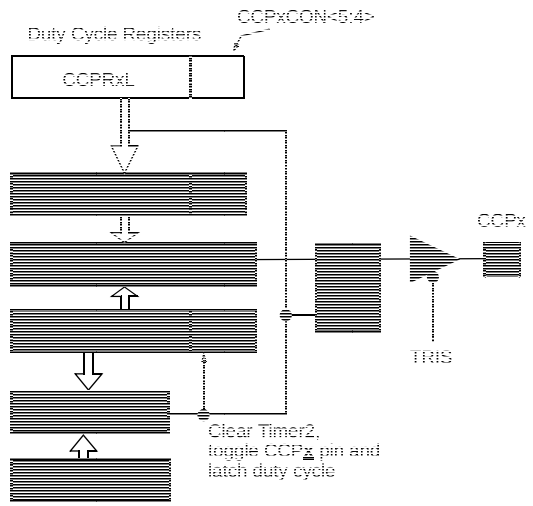
In Pulse-Width Modulation (PWM) mode, the CCP module produces up to a 10-bit resolution PWM output on the CCPx pin.

Figure 15-3 shows a simplified block diagram of PWM operation.

Figure 15-4 shows a typical waveform of the PWM signal.

For a step-by-step procedure on how to set up the CCP module for PWM operation, refer to **Section 15.3.8 "Setup for PWM Operation"**.

FIGURE 15-3: SIMPLIFIED PWM BLOCK DIAGRAM

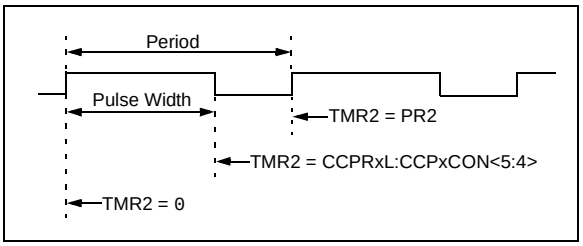


Note 1: The 8-bit timer TMR2 register is concatenated with the 2-bit internal system clock (Fosc), or 2 bits of the prescaler, to create the 10-bit time base.

2: In PWM mode, CCPRxH is a read-only register.

The PWM output (Figure 15-4) has a time base (period) and a time that the output stays high (duty cycle).

FIGURE 15-4: CCP PWM OUTPUT



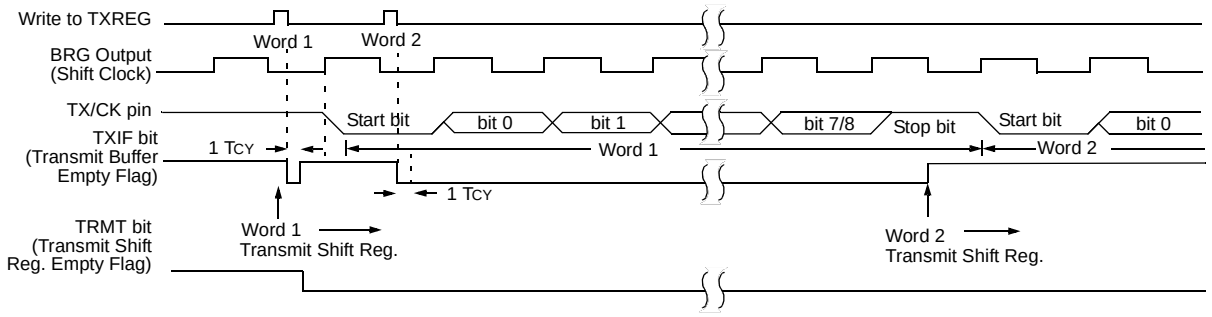
15.3.1 CCPx PIN CONFIGURATION

In PWM mode, the CCPx pin is multiplexed with the PORT data latch. The user must configure the CCPx pin as an output by clearing the associated TRIS bit.

Either RC1 or RB3 can be selected as the CCP2 pin. Refer to **Section 6.1 "Alternate Pin Function"** for more information.

Note:	Clearing the CCPxCON register will relinquish CCPx control of the CCPx pin.

FIGURE 16-4: ASYNCHRONOUS TRANSMISSION (BACK-TO-BACK)



Note: This timing diagram shows two consecutive transmissions.

TABLE 16-1: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SPBRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	0000 0000	0000 0000
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
TXREG	AUSART Transmit Data Register								0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Asynchronous Transmission.

REGISTER 17-1: SSPCON: SYNC SERIAL PORT CONTROL REGISTER (SPI MODE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **WCOL**: Write Collision Detect bit
- 1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)
- 0 = No collision

bit 6 **SSPOV**: Receive Overflow Indicator bit
- 1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in Slave mode. The user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register.
- 0 = No overflow

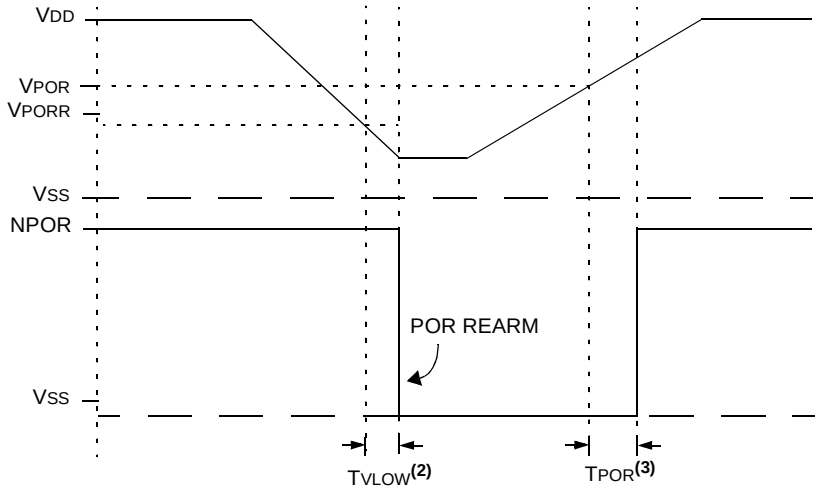
bit 5 **SSPEN**: Synchronous Serial Port Enable bit
- 1 = Enables serial port and configures SCK, SDO and SDI as serial port pins**(1)**
- 0 = Disables serial port and configures these pins as I/O port pins

bit 4 **CKP**: Clock Polarity Select bit
- 1 = Idle state for clock is a high level
- 0 = Idle state for clock is a low level

bit 3-0 **SSPM<3:0>**: Synchronous Serial Port Mode Select bits
- 0000 = SPI Master mode, clock = FOSC/4
- 0001 = SPI Master mode, clock = FOSC/16
- 0010 = SPI Master mode, clock = FOSC/64
- 0011 = SPI Master mode, clock = TMR2 output/2
- 0100 = SPI Slave mode, clock = SCK pin. $\overline{SS}$ pin control enabled.
- 0101 = SPI Slave mode, clock = SCK pin. $\overline{SS}$ pin control disabled. $\overline{SS}$ can be used as I/O pin.

Note 1: When enabled, these pins must be properly configured as input or output.

FIGURE 23-1: POR AND POR REARM WITH SLOW RISING VDD



Note 1: When NPOR is low, the device is held in Reset.
2: TPOR 1 μs typical.
3: TVLOW 2.7 μs typical.

FIGURE 24-15: PIC16F722/3/4/6/7 TYPICAL IDD vs. VDD OVER FOSC, XT MODE, VCAP = 0.1 µF

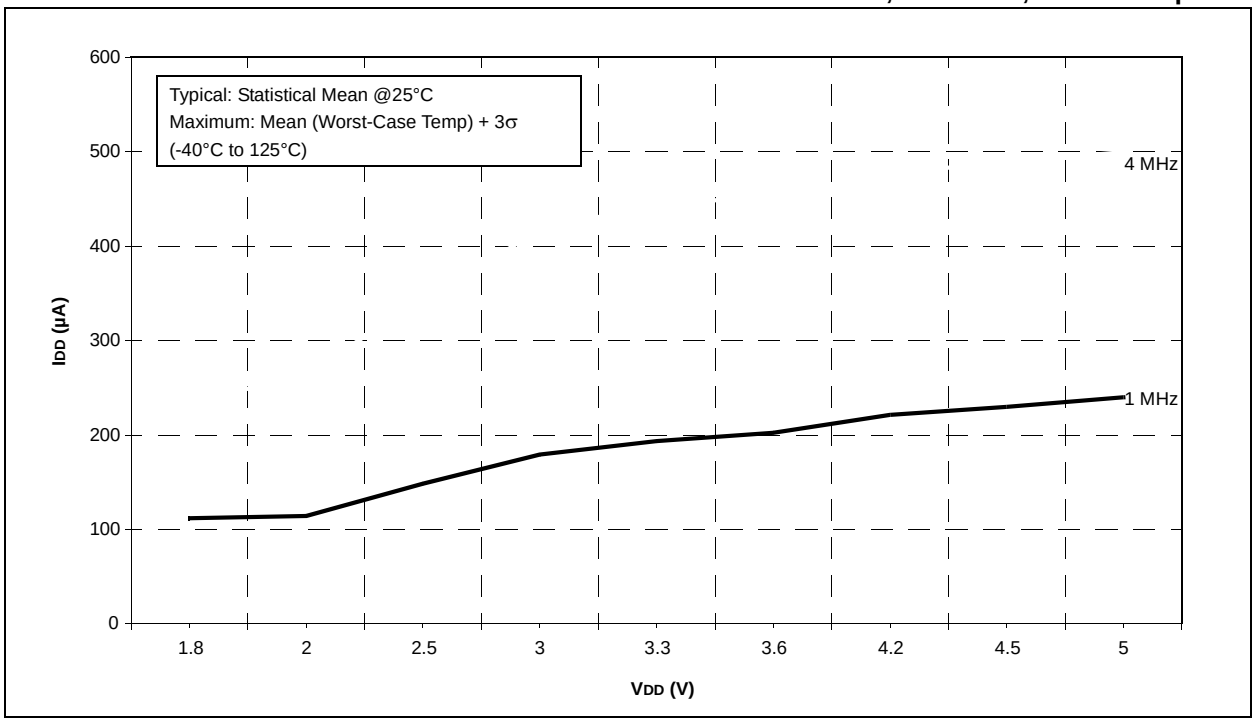


FIGURE 24-16: PIC16LF722/3/4/6/7 TYPICAL IDD vs. VDD OVER FOSC, XT MODE

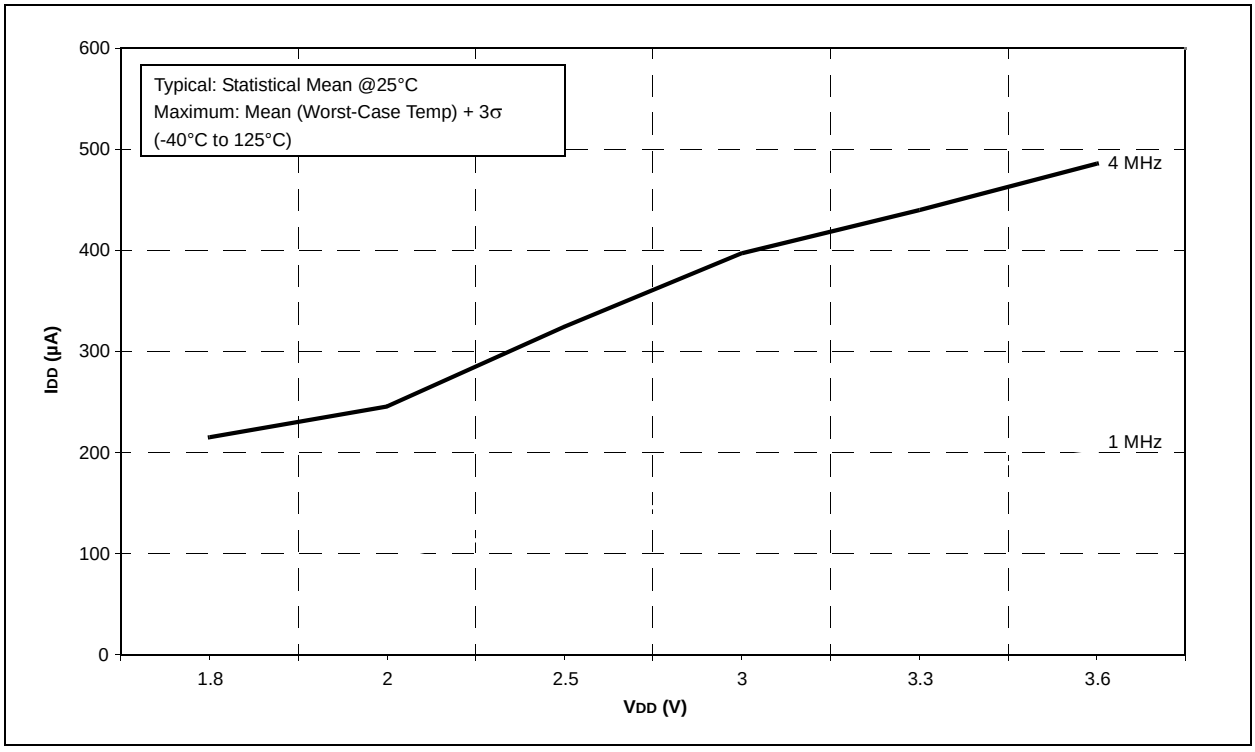


FIGURE 24-35: PIC16F722/3/4/6/7 CAP SENSE HIGH POWER IPD vs. VDD, VCAP = 0.1 µF

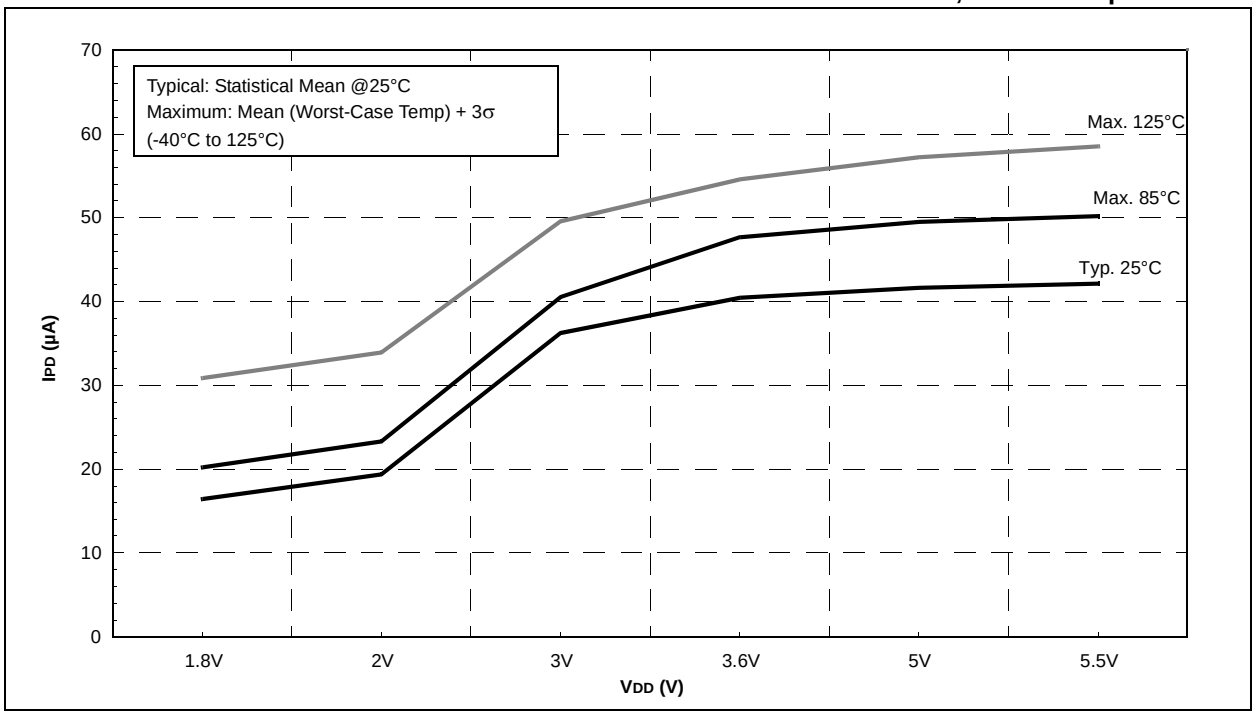


FIGURE 24-36: PIC16LF722/3/4/6/7 CAP SENSE HIGH POWER IPD vs. VDD

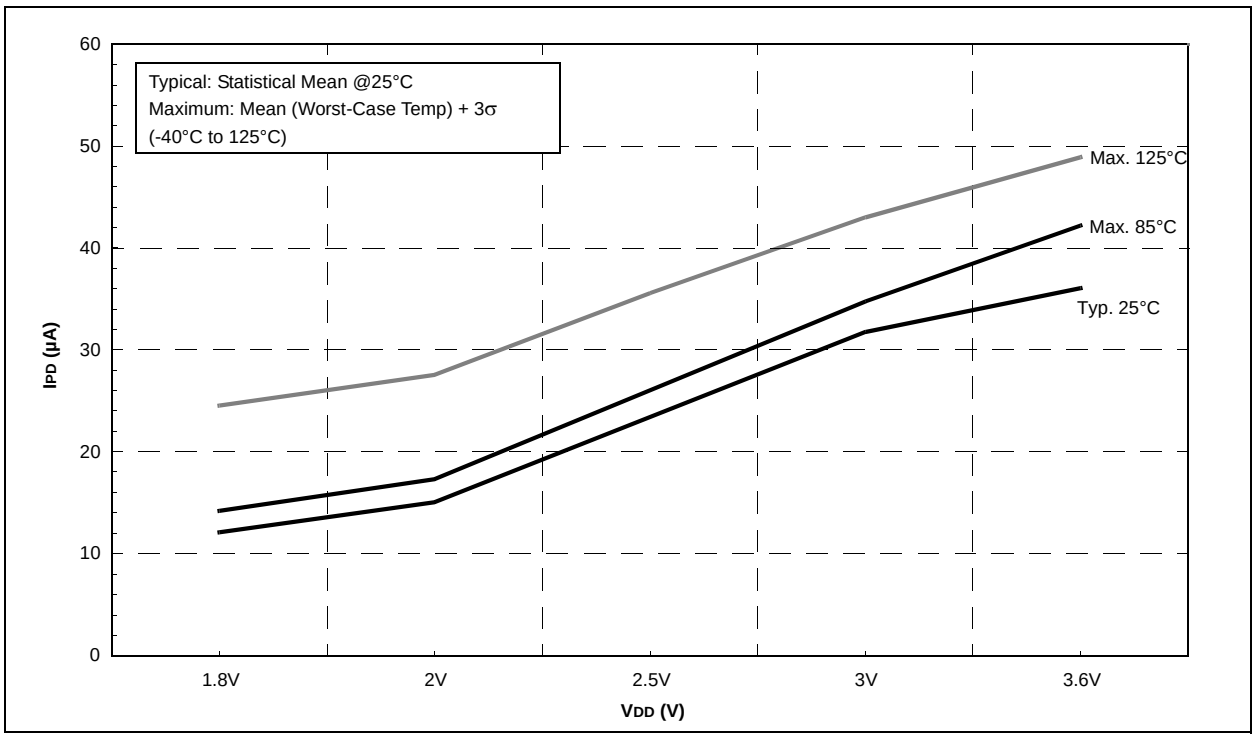


FIGURE 24-45: PIC16F722/3/4/6/7 ADC IPD vs. VDD, VCAP = 0.1 µF

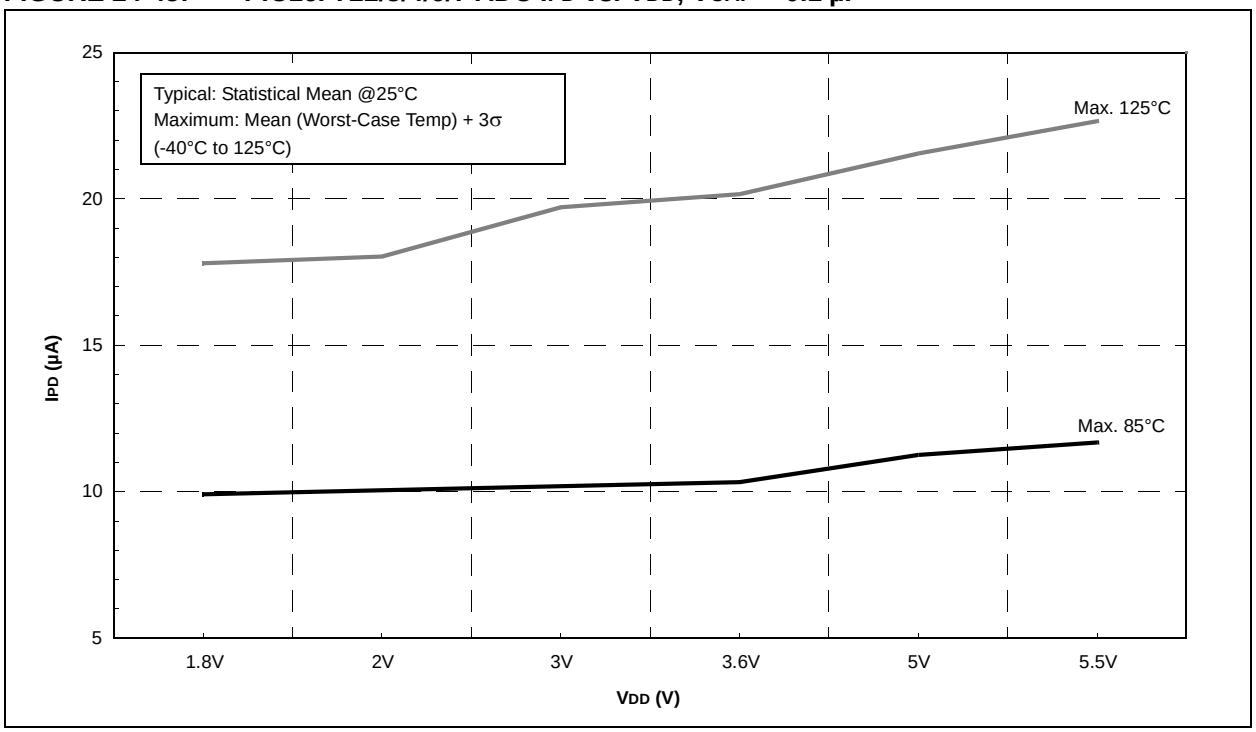


FIGURE 24-46: PIC16LF722/3/4/6/7 ADC IPD vs. VDD

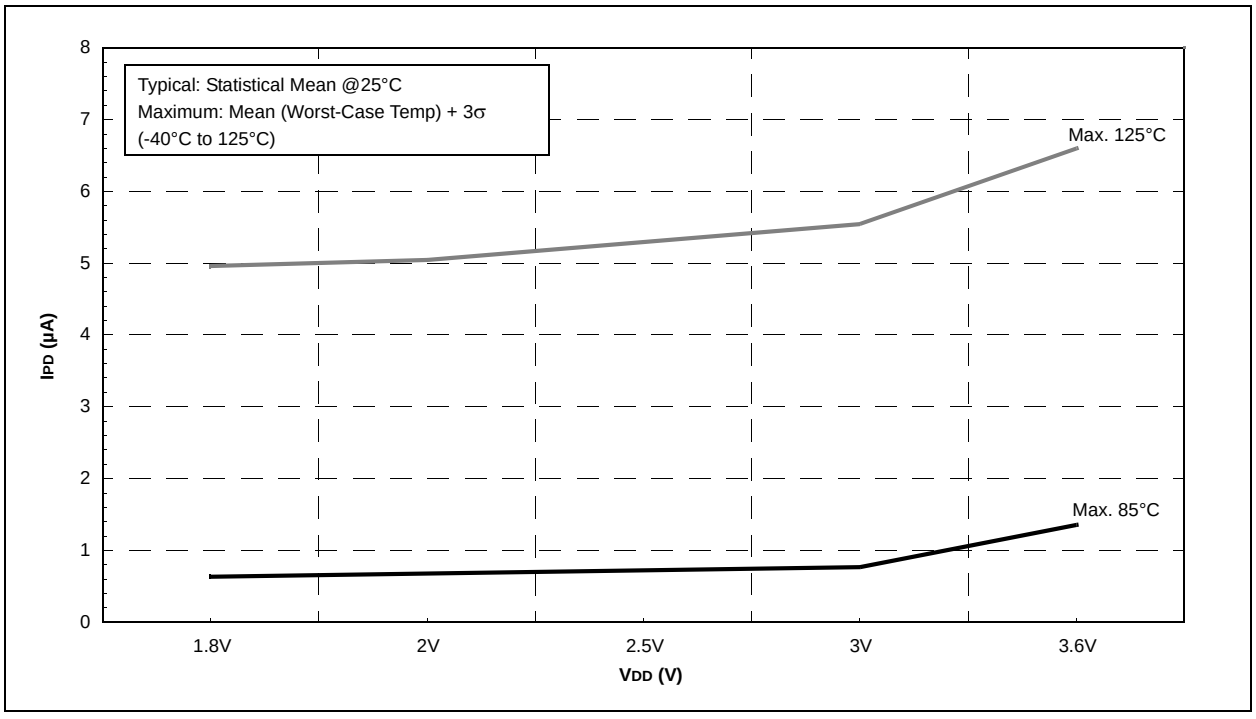


FIGURE 24-51: SCHMITT TRIGGER INPUT THRESHOLD VIN vs. VDD OVER TEMPERATURE

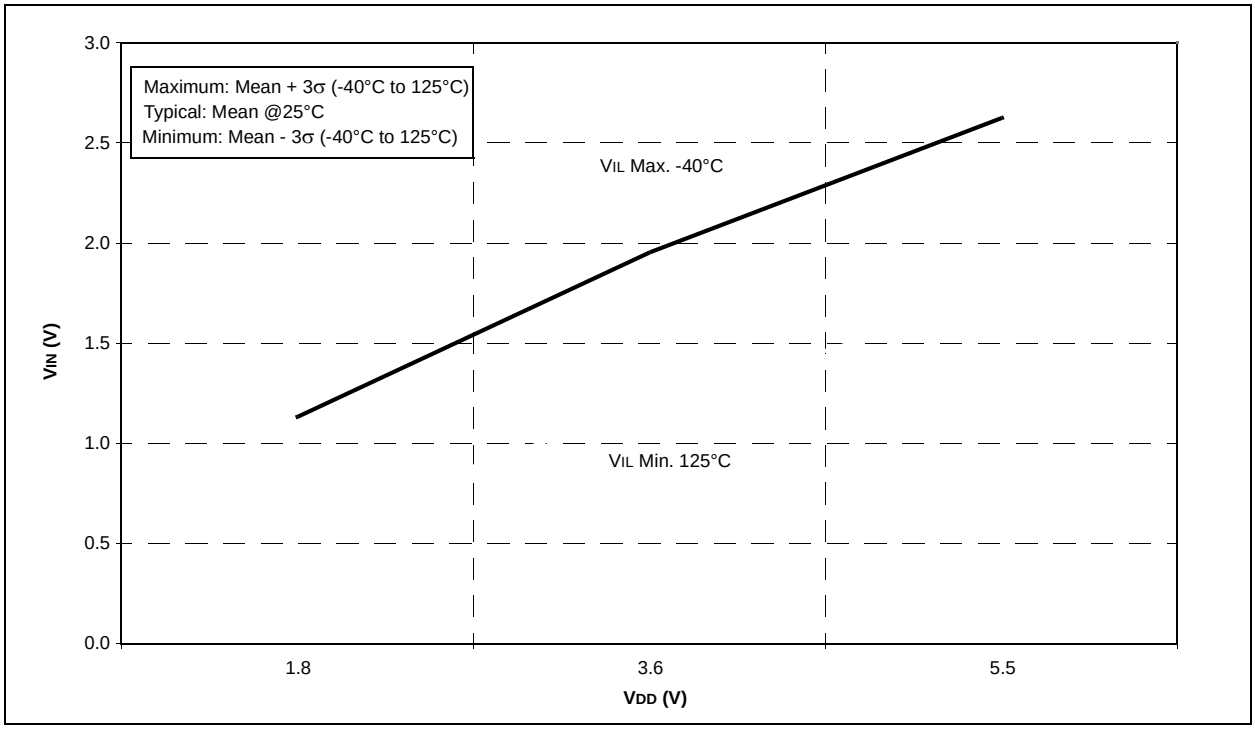


FIGURE 24-52: VOH vs. IOH OVER TEMPERATURE, VDD = 5.5V

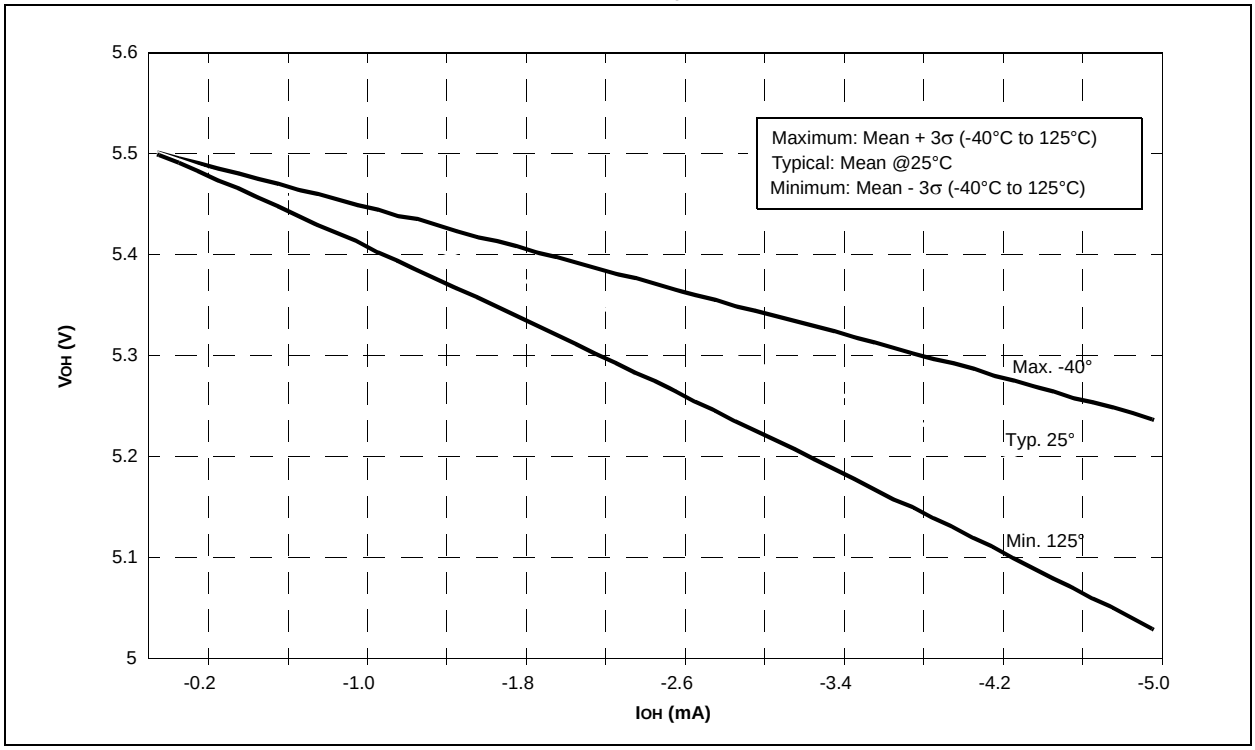


FIGURE 24-53: VOH vs. IOH OVER TEMPERATURE, VDD = 3.6V

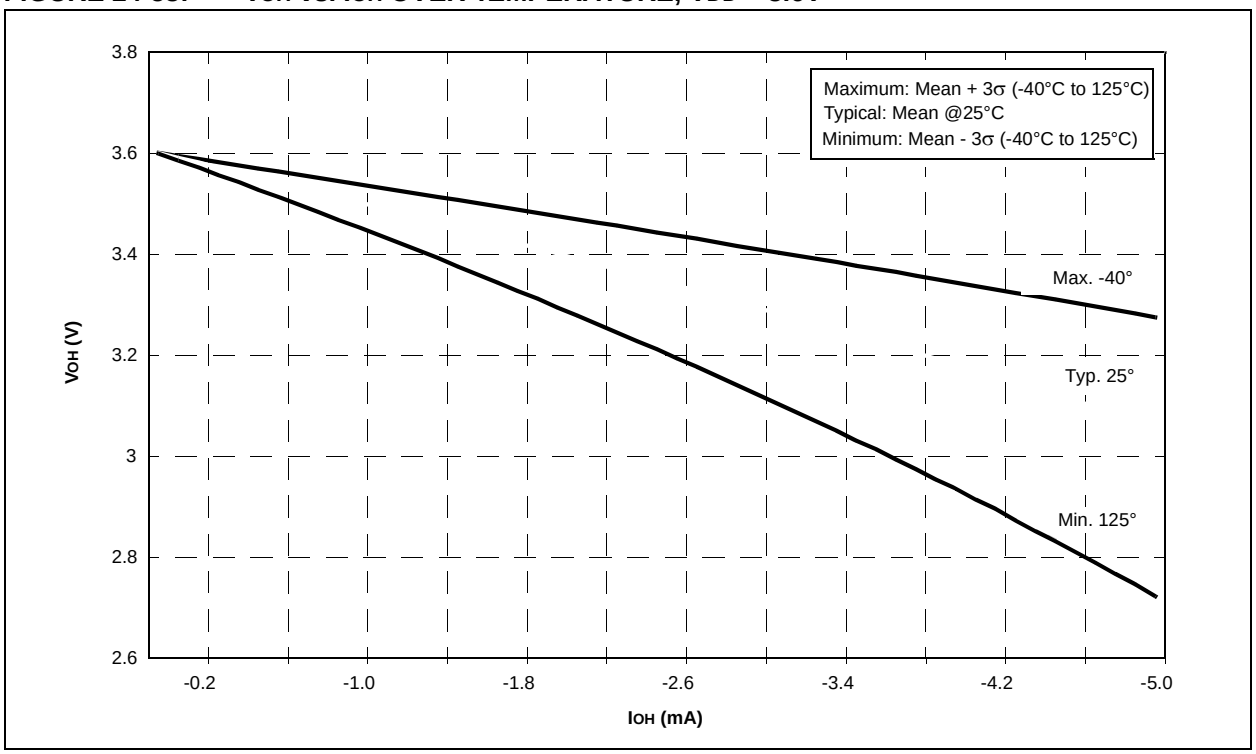


FIGURE 24-54: VOH vs. IOH OVER TEMPERATURE, VDD = 1.8V

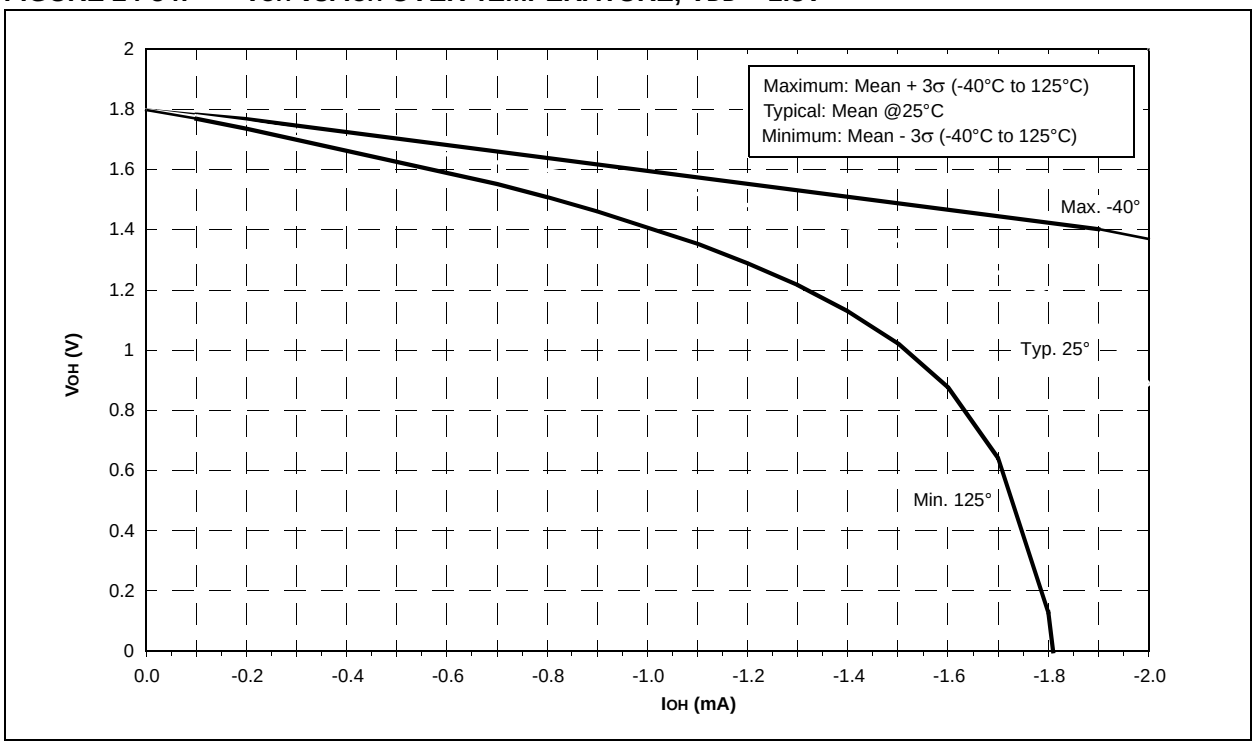


FIGURE 24-67: PIC16F722/3/4/6/7 CAP SENSOR HYSTERESIS, POWER MODE = LOW

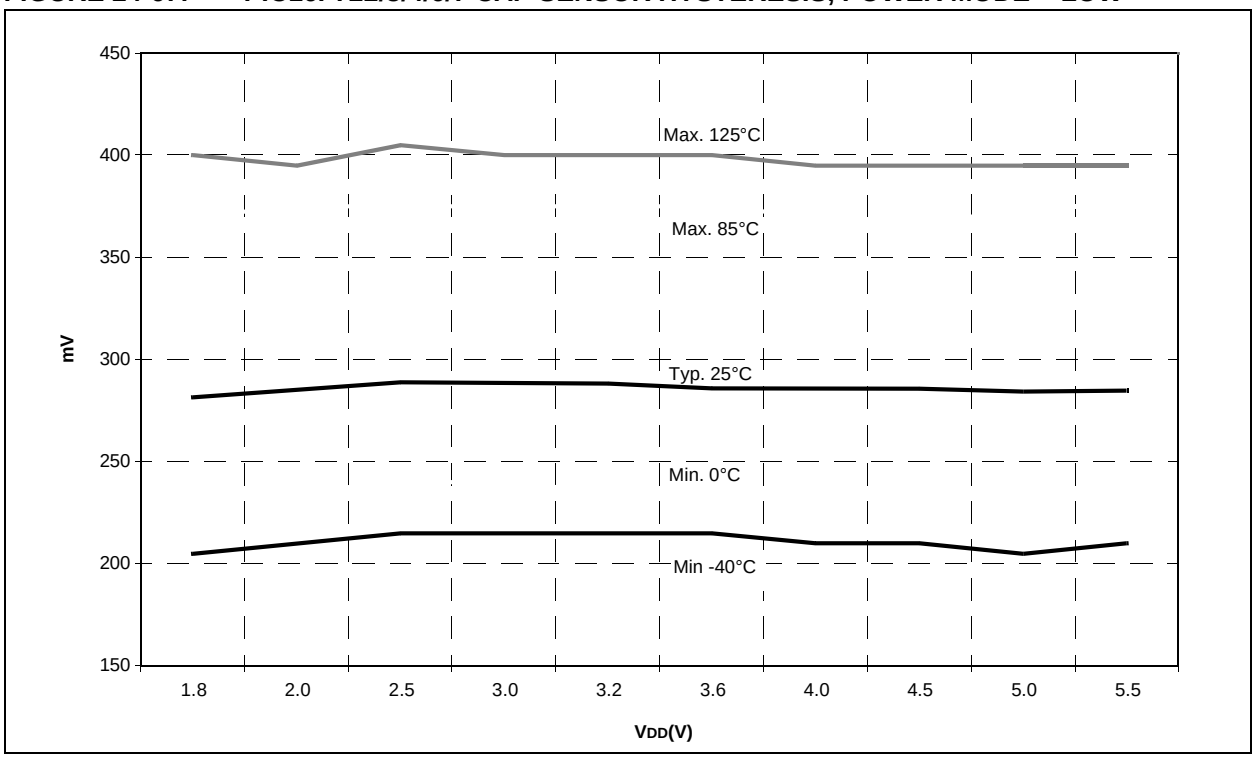
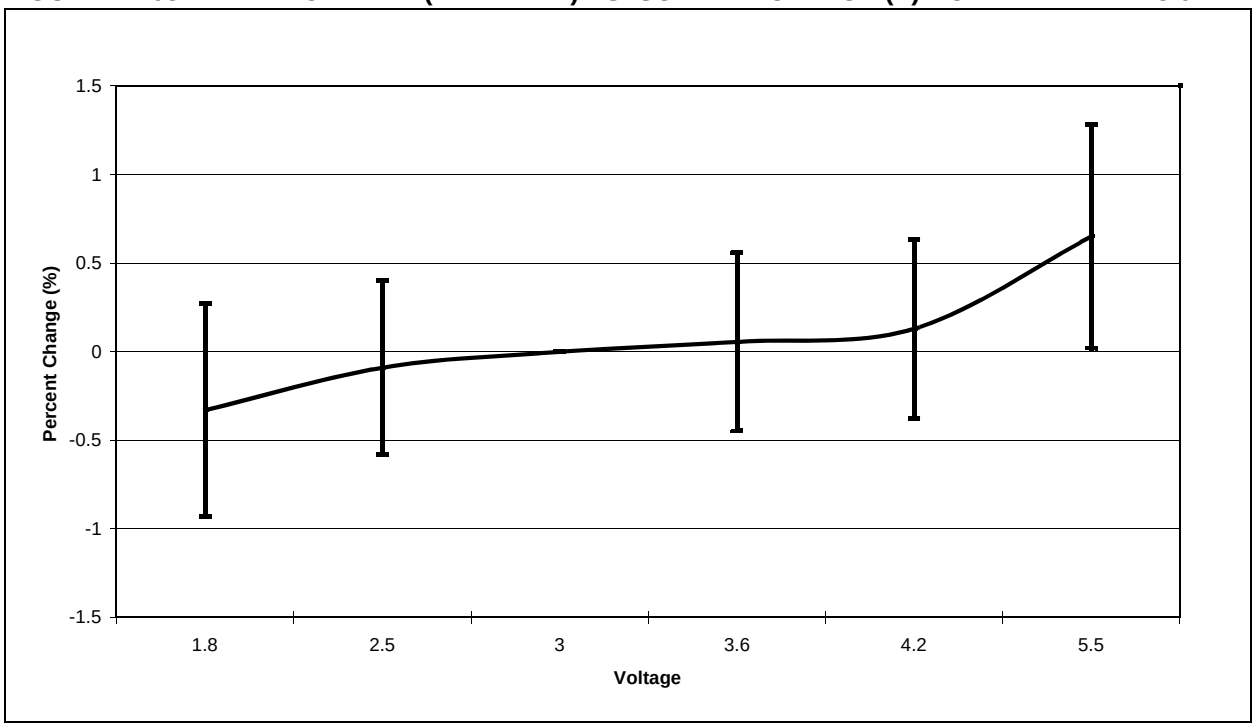
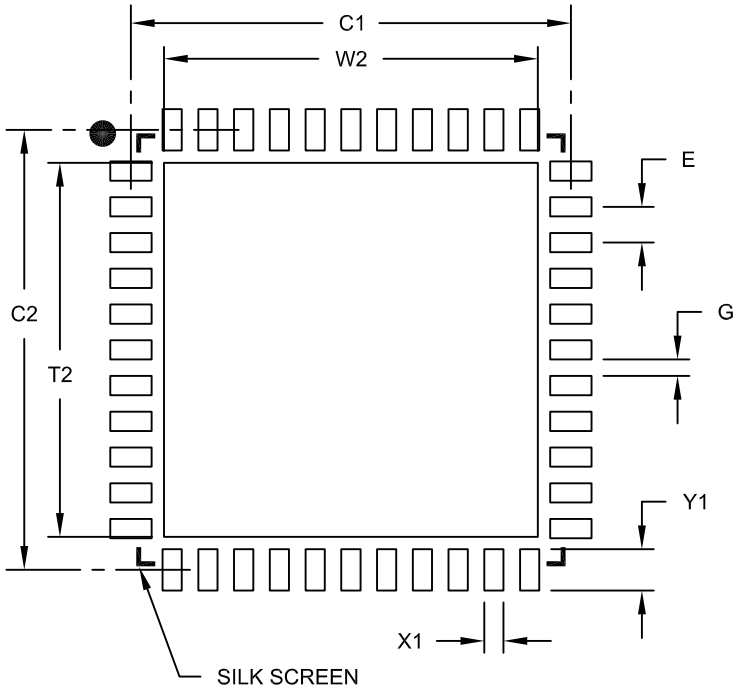


FIGURE 24-68: TYPICAL FVR (X1 AND X2) VS. SUPPLY VOLTAGE (V) NORMALIZED AT 3.0V



44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			6.80
Optional Center Pad Length	T2			6.80
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.80
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A