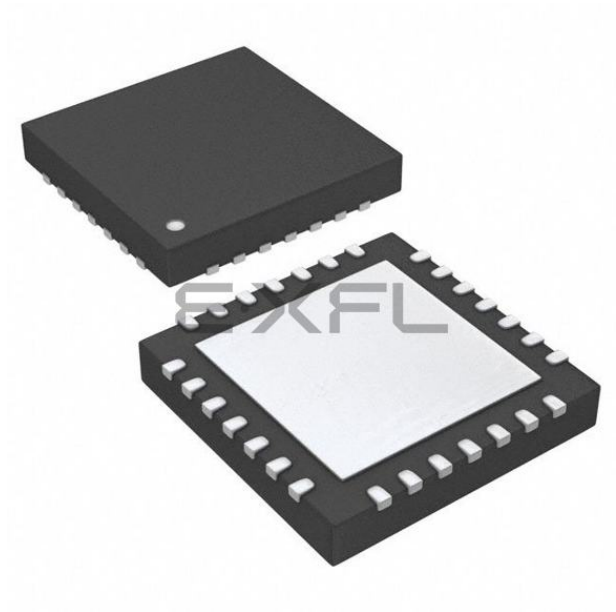

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Details	
Product Status	Active
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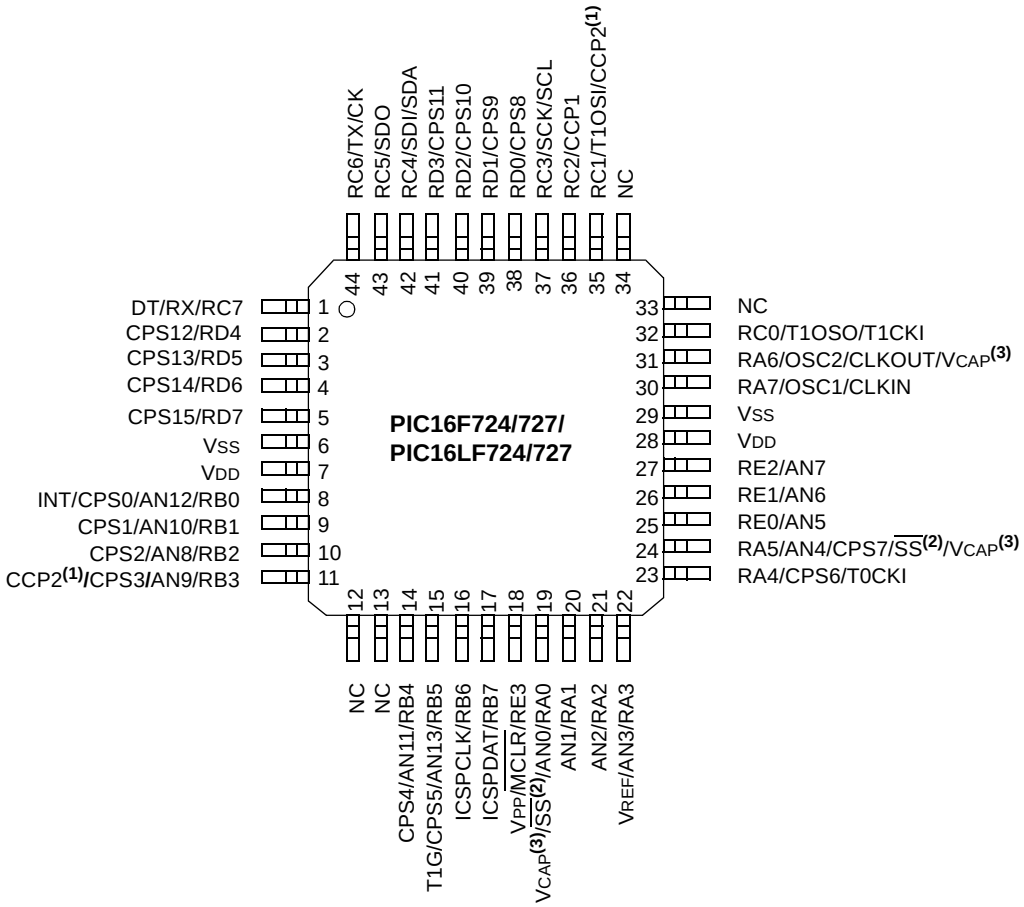
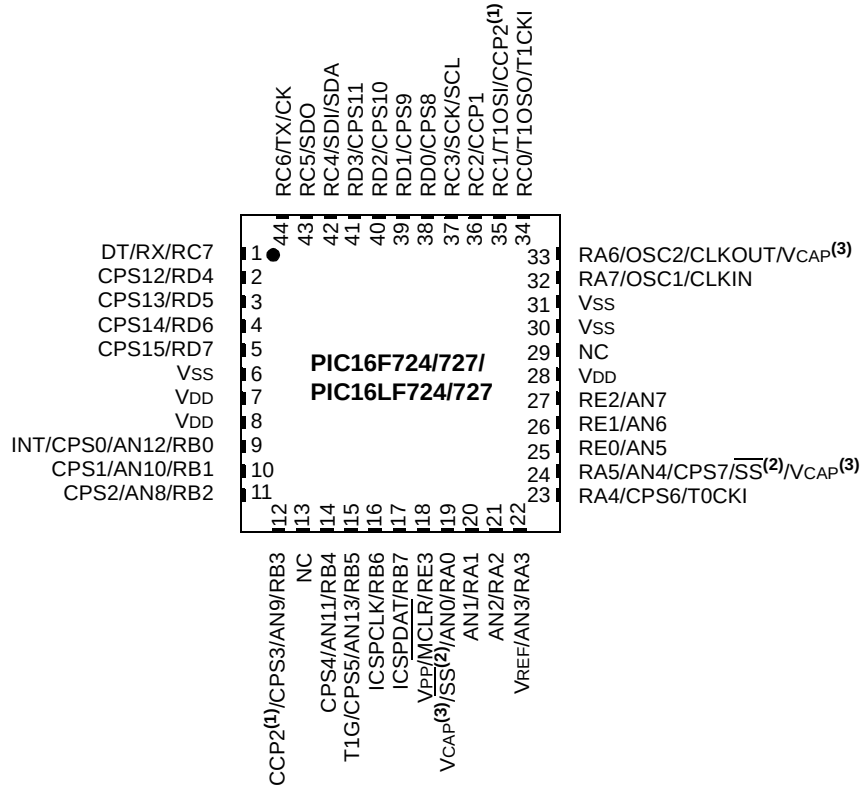
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f726-i-mv

Pin Diagrams – 44-PIN TQFP (PIC16F724/727/PIC16LF724/727)



Note 1: CCP2 pin location may be selected as RB3 or RC1.
2: $\overline{SS}$ pin location may be selected as RA5 or RA0.
3: PIC16F724/727 devices only.

Pin Diagrams – 44-PIN QFN (PIC16F724/727/PIC16LF724/727)



Note 1: CCP2 pin location may be selected as RB3 or RC1.
2: $\overline{SS}$ pin location may be selected as RA5 or RA0.
3: PIC16F724/727 devices only.

2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC16(L)F722/3/4/6/7 has a 13-bit program counter capable of addressing a 2K x 14 program memory space for the PIC16F722/LF722 (0000h-07FFh), a 4K x 14 program memory space for the PIC16F723/LF723 and PIC16F724/LF724 (0000h-0FFFh) and an 8K x 14 program memory space for the PIC16F726/LF726 and PIC16F727/LF727 (0000h-1FFFh). Accessing a location above the memory boundaries for the PIC16F722/LF722 will cause a wrap-around within the first 2K x 14 program memory space. Accessing a location above the memory boundaries for the PIC16F723/LF723 and PIC16F724/LF724 will cause a wrap-around within the first 4K x 14 program memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F722/LF722

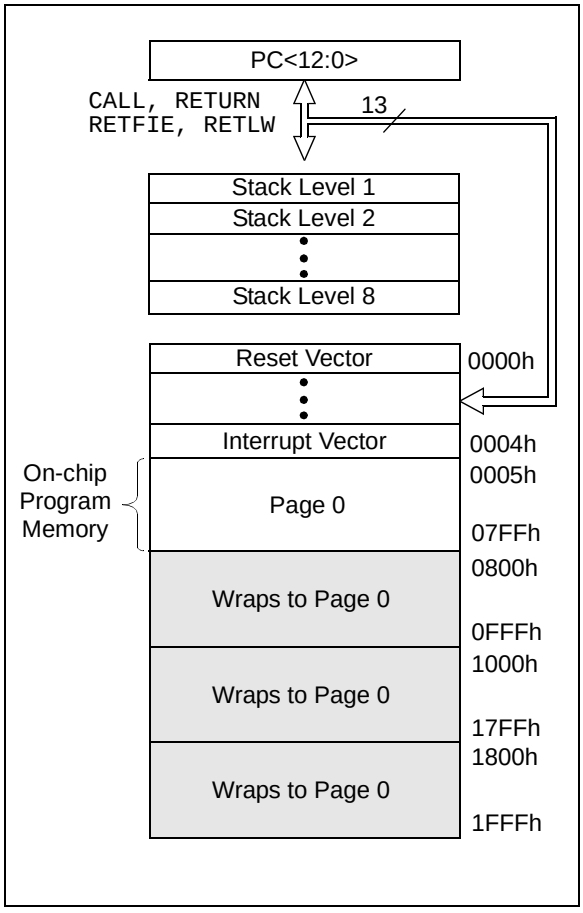


FIGURE 2-2: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F723/LF723 AND PIC16F724/LF724

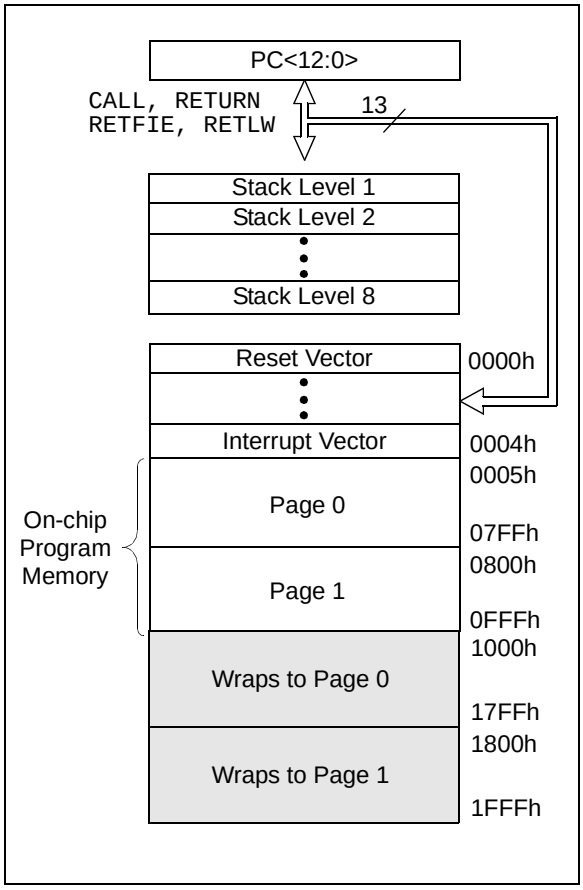


FIGURE 2-4: PIC16F722/LF722 SPECIAL FUNCTION REGISTERS

Bank 0	File Address	Bank 1	File Address	Bank 2	File Address	Bank 3	File Address
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION	81h	TMR0	101h	OPTION	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h	ANSELA	185h
PORTB	06h	TRISB	86h		106h	ANSELB	186h
PORTC	07h	TRISC	87h		107h		187h
	08h		88h	CPSCON0	108h		188h
PORTE	09h	TRISE	89h	CPSCON1	109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	PMDATL	10Ch	PMCON1	18Ch
PIR2	0Dh	PIE2	8Dh	PMADRL	10Dh	Reserved	18Dh
TMR1L	0Eh	PCON	8Eh	PMDATH	10Eh	Reserved	18Eh
TMR1H	0Fh	T1GCON	8Fh	PMADRH	10Fh	Reserved	18Fh
T1CON	10h	OSCCON	90h		110h		190h
TMR2	11h	OSCTUNE	91h		111h		191h
T2CON	12h	PR2	92h		112h		192h
SSPBUF	13h	SSPADD/SSPMSK	93h		113h		193h
SSPCON	14h	SSPSTAT	94h		114h		194h
CCPR1L	15h	WPUB	95h		115h		195h
CCPR1H	16h	IOCB	96h		116h		196h
CCP1CON	17h		97h		117h		197h
RCSTA	18h	TXSTA	98h		118h		198h
TXREG	19h	SPBRG	99h		119h		199h
RCREG	1Ah		9Ah		11Ah		19Ah
CCPR2L	1Bh		9Bh		11Bh		19Bh
CCPR2H	1Ch	APFCON	9Ch		11Ch		19Ch
CCP2CON	1Dh	FVRCON	9Dh		11Dh		19Dh
ADRES	1Eh		9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
	20h		A0h		120h		1A0h
General Purpose Register 96 Bytes		General Purpose Register 32 Bytes	BFh				
			C0h				
			EFh		16Fh		1EFh
			F0h		170h		1F0h
		Accesses 70h-7Fh		Accesses 70h-7Fh		Accesses 70h-7Fh	
	7Fh		FFh		17Fh		1FFh

Legend: = Unimplemented data memory locations, read as '0'.
* = Not a physical register.

6.0 I/O PORTS

There are as many as 35 general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

6.1 Alternate Pin Function

The Alternate Pin Function Control (APFCON) register is used to steer specific peripheral input and output functions between different pins. The APFCON register is shown in Register 6-1. For this device family, the following functions can be moved between different pins.

- $\overline{SS}$ (Slave Select)
- CCP2

REGISTER 6-1: APFCON: ALTERNATE PIN FUNCTION CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	SSSEL	CCP2SEL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as ‘0’.

bit 1 **SSSEL:** $\overline{SS}$ Input Pin Selection bit
0 = $\overline{SS}$ function is on RA5/AN4/CPS7/$\overline{SS}$/V_{CAP}
1 = $\overline{SS}$ function is on RA0/AN0/$\overline{SS}$/V_{CAP}

bit 0 **CCP2SEL:** CCP2 Input/Output Pin Selection bit
0 = CCP2 function is on RC1/T1OSI/CCP2
1 = CCP2 function is on RB3/CCP2

6.2 PORTA and the TRISA Registers

PORTA is a 8-bit wide, bidirectional port. The corresponding data direction register is TRISA (Register 6-3). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., disable the output driver). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). Example 6-1 shows how to initialize PORTA.

Reading the PORTA register (Register 6-2) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch.

The TRISA register (Register 6-3) controls the PORTA pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

Note:	The ANSELA register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

EXAMPLE 6-1: INITIALIZING PORTA

```
BANKSEL PORTA       ;
CLRF    PORTA       ;Init PORTA
BANKSEL ANSELA      ;
CLRF    ANSELA      ;digital I/O
BANKSEL TRISA       ;
MOVLW   0Ch         ;Set RA<3:2> as inputs
MOVWF   TRISA       ;and set RA<7:4,1:0>
                    ;as outputs
```

REGISTER 6-2: PORTA: PORTA REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **RA<7:0>**: PORTA I/O Pin bit
1 = Port pin is > V_{IH}
0 = Port pin is < V_{IL}

REGISTER 6-3: TRISA: PORTA TRI-STATE REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **TRISA<7:0>:** PORTA Tri-State Control bit
1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

FIGURE 6-12: BLOCK DIAGRAM OF RB7

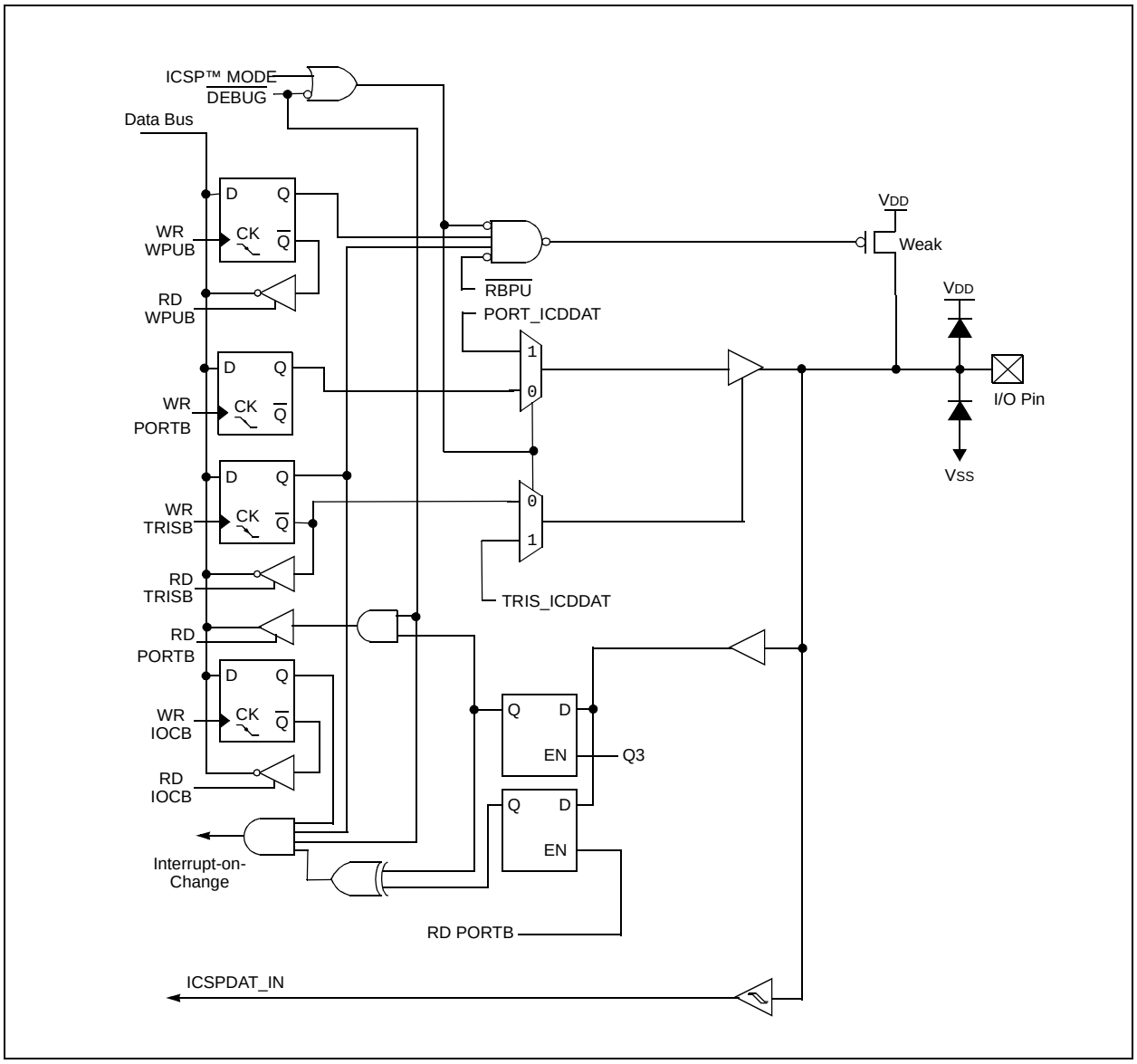


TABLE 6-3: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
APFCON	—	—	—	—	—	—	SSSEL	CCP2SEL	---- --00	---- --00
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	xxxx xxxx
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
SSPSTAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000 0000	0000 0000
T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	—	TMR1ON	0000 00-0	uuuu uu-u
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Port C.

10.0 FIXED VOLTAGE REFERENCE

This device contains an internal voltage regulator. To provide a reference for the regulator, a band gap reference is provided. This band gap is also user accessible via an A/D converter channel.

User level band gap functions are controlled by the FVRCON register, which is shown in Register 10-1.

REGISTER 10-1: FVRCON: FIXED VOLTAGE REFERENCE REGISTER

R-q	R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
FVRRDY	FVREN	—	—	—	—	ADFVR1	ADFVR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown
q = Value depends on condition			

bit 7 **FVRRDY(1):** Fixed Voltage Reference Ready Flag bit
- 0 = Fixed Voltage Reference output is not active or stable
- 1 = Fixed Voltage Reference output is ready for use

bit 6 **FVREN(2):** Fixed Voltage Reference Enable bit
- 0 = Fixed Voltage Reference is disabled
- 1 = Fixed Voltage Reference is enabled

bit 5-2 **Unimplemented:** Read as ‘0’

bit 1-0 **ADFVR<1:0>:** A/D Converter Fixed Voltage Reference Selection bits
- 00 = A/D Converter Fixed Voltage Reference Peripheral output is off.
- 01 = A/D Converter Fixed Voltage Reference Peripheral output is 1x (1.024V)
- 10 = A/D Converter Fixed Voltage Reference Peripheral output is 2x (2.048V)(2)
- 11 = A/D Converter Fixed Voltage Reference Peripheral output is 4x (4.096V)(2)

Note 1: FVRRDY is always ‘1’ for the PIC16F72X devices.

2: Fixed Voltage Reference output cannot exceed V_{DD}.

16.1 AUSART Asynchronous Mode

The AUSART transmits and receives data using the standard non-return-to-zero (NRZ) format. NRZ is implemented with two levels: a VOH Mark state which represents a '1' data bit, and a VOL Space state which represents a '0' data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port idles in the Mark state. Each character transmission consists of one Start bit followed by eight or nine data bits and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is 8 bits. Each transmitted bit persists for a period of 1/(Baud Rate). An on-chip dedicated 8-bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. Refer to Table 16-5 for examples of baud rate Configurations.

The AUSART transmits and receives the LSb first. The AUSART's transmitter and receiver are functionally independent, but share the same data format and baud rate. Parity is not supported by the hardware, but can be implemented in software and stored as the ninth data bit.

16.1.1 AUSART ASYNCHRONOUS TRANSMITTER

The AUSART transmitter block diagram is shown in Figure 16-1. The heart of the transmitter is the serial Transmit Shift Register (TSR), which is not directly accessible by software. The TSR obtains its data from the transmit buffer, which is the TXREG register.

16.1.1.1 Enabling the Transmitter

The AUSART transmitter is enabled for asynchronous operations by configuring the following three control bits:

- TXEN = 1
- SYNC = 0
- SPEN = 1

All other AUSART control bits are assumed to be in their default state.

Setting the TXEN bit of the TXSTA register enables the transmitter circuitry of the AUSART. Clearing the SYNC bit of the TXSTA register configures the AUSART for asynchronous operation. Setting the SPEN bit of the RCSTA register enables the AUSART and automatically configures the TX/CK I/O pin as an output.

Note 1: When the SPEN bit is set the RX/DT I/O pin is automatically configured as an input, regardless of the state of the corresponding TRIS bit and whether or not the AUSART receiver is enabled. The RX/DT pin data can be read via a normal PORT read but PORT latch data output is precluded.

2: The TXIF transmitter interrupt flag is set when the TXEN enable bit is set.

16.1.1.2 Transmitting Data

A transmission is initiated by writing a character to the TXREG register. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the TXREG until the Stop bit of the previous character has been transmitted. The pending character in the TXREG is then transferred to the TSR in one TCY immediately following the Stop bit transmission. The transmission of the Start bit, data bits and Stop bit sequence commences immediately following the transfer of the data to the TSR from the TXREG.

16.1.1.3 Transmit Interrupt Flag

The TXIF interrupt flag bit of the PIR1 register is set whenever the AUSART transmitter is enabled and no character is being held for transmission in the TXREG. In other words, the TXIF bit is only clear when the TSR is busy with a character and a new character has been queued for transmission in the TXREG. The TXIF flag bit is not cleared immediately upon writing TXREG. TXIF becomes valid in the second instruction cycle following the write execution. Polling TXIF immediately following the TXREG write will return invalid results. The TXIF bit is read-only, it cannot be set or cleared by software.

The TXIF interrupt can be enabled by setting the TXIE interrupt enable bit of the PIE1 register. However, the TXIF flag bit will be set whenever the TXREG is empty, regardless of the state of TXIE enable bit.

To use interrupts when transmitting data, set the TXIE bit only when there is more data to send. Clear the TXIE interrupt enable bit upon writing the last character of the transmission to the TXREG.

16.2 AUSART Baud Rate Generator (BRG)

The Baud Rate Generator (BRG) is an 8-bit timer that is dedicated to the support of both the asynchronous and synchronous AUSART operation.

The SPBRG register determines the period of the free running baud rate timer. In Asynchronous mode the multiplier of the baud rate period is determined by the BRGH bit of the TXSTA register. In Synchronous mode, the BRGH bit is ignored.

Table 16-3 contains the formulas for determining the baud rate. Example 16-1 provides a sample calculation for determining the baud rate and baud rate error.

Typical baud rates and error values for various asynchronous modes have been computed for your convenience and are shown in Table 16-3. It may be advantageous to use the high baud rate (BRGH = 1), to reduce the baud rate error.

Writing a new value to the SPBRG register causes the BRG timer to be reset (or cleared). This ensures that the BRG does not wait for a timer overflow before outputting the new baud rate.

EXAMPLE 16-1: CALCULATING BAUD RATE ERROR

For a device with FOSC of 16 MHz, desired baud rate of 9600, and Asynchronous mode with SYNC = 0 and BRGH = 0 (as seen in Table 16-3):

$$Desired\ Baud\ Rate = \frac{FOSC}{64(SPBRG + 1)}$$

Solving for SPBRG:

$$SPBRG = \left(\frac{FOSC}{64(Desired\ Baud\ Rate)}\right) - 1$$

$$= \left(\frac{16000000}{64(9600)}\right) - 1$$

$$= [25.042] = 25$$

$$Actual\ Baud\ Rate = \frac{16000000}{64(25 + 1)}$$

$$= 9615$$

$$\%\ Error = \left(\frac{Actual\ Baud\ Rate - Desired\ Baud\ Rate}{Desired\ Baud\ Rate}\right) 100$$

$$= \left(\frac{9615 - 9600}{9600}\right) 100 = 0.16\%$$

TABLE 16-3: BAUD RATE FORMULAS

Configuration Bits		AUSART Mode	Baud Rate Formula
SYNC	BRGH		
0	0	Asynchronous	FOSC/[64 (n+1)]
0	1	Asynchronous	FOSC/[16 (n+1)]
1	x	Synchronous	FOSC/[4 (n+1)]

Legend: x = Don't care, n = value of SPBRG register

TABLE 16-4: REGISTERS ASSOCIATED WITH THE BAUD RATE GENERATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SPBRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for the Baud Rate Generator.

21.0 INSTRUCTION SET SUMMARY

The PIC16(L)F722/3/4/6/7 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 14-bit word divided into an **opcode,** which specifies the instruction type and one or more **operands,** which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 21-1, while the various opcode fields are summarized in Table 21-1.

Table 21-2 lists the instructions recognized by the MPASM™ assembler.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a nominal instruction execution time of 1 µs. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

21.1 Read-Modify-Write Operations

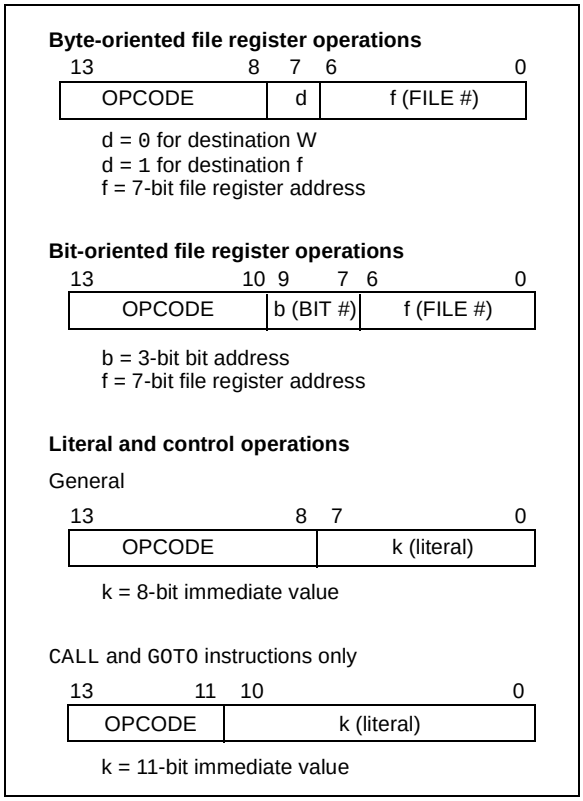
Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

For example, a CLRF PORTB instruction will read PORTB, clear all the data bits, then write the result back to PORTB. This example would have the unintended consequence of clearing the condition that set the RBIF flag.

TABLE 21-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
PC	Program Counter
$\overline{TO}$	Time-out bit
C	Carry bit
DC	Digit carry bit
Z	Zero bit
$\overline{PD}$	Power-down bit

FIGURE 21-1: GENERAL FORMAT FOR INSTRUCTIONS



23.2 DC Characteristics: PIC16(L)F722/3/4/6/7-I/E (Industrial, Extended) (Continued)

PIC16LF722/3/4/6/7	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended
PIC16F722/3/4/6/7	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended

Param No.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
						VDD	Note
	Supply Current (IDD)(1, 2)						
D014		—	290	330	µA	1.8	FOSC = 4 MHz EC Oscillator mode
		—	460	500	µA	3.0	
D014		—	300	430	µA	1.8	FOSC = 4 MHz EC Oscillator mode **(Note 5)**
		—	450	655	µA	3.0	
		—	500	730	µA	5.0	
D015		—	100	130	µA	1.8	FOSC = 500 kHz MFINTOSC mode
		—	120	150	µA	3.0	
D015		—	115	195	µA	1.8	FOSC = 500 kHz MFINTOSC mode **(Note 5)**
		—	135	200	µA	3.0	
		—	150	220	µA	5.0	
D016		—	650	800	µA	1.8	FOSC = 8 MHz HFINTOSC mode
		—	1000	1200	µA	3.0	
D016		—	625	850	µA	1.8	FOSC = 8 MHz HFINTOSC mode **(Note 5)**
		—	1000	1200	µA	3.0	
		—	1100	1500	µA	5.0	
D017		—	1.0	1.2	mA	1.8	FOSC = 16 MHz HFINTOSC mode
		—	1.5	1.85	mA	3.0	
D017		—	1	1.2	mA	1.8	FOSC = 16 MHz HFINTOSC mode **(Note 5)**
		—	1.5	1.7	mA	3.0	
		—	1.7	2.1	mA	5.0	
D018		—	210	240	µA	1.8	FOSC = 4 MHz EXTRC mode **(Note 3, Note 5)**
		—	340	380	µA	3.0	
D018		—	225	320	µA	1.8	FOSC = 4 MHz EXTRC mode **(Note 3, Note 5)**
		—	360	445	µA	3.0	
		—	410	650	µA	5.0	
D019		—	1.6	1.9	mA	3.0	FOSC = 20 MHz HS Oscillator mode
		—	2.0	2.8	mA	3.6	
D019		—	1.6	2	mA	3.0	FOSC = 20 MHz HS Oscillator mode **(Note 5)**
		—	1.9	3.2	mA	5.0	

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ.

4: FVR and BOR are disabled.

5: 0.1 µF capacitor on VCAP (RA0).

23.3 DC Characteristics: PIC16(L)F722/3/4/6/7-I/E (Power-Down) (Continued)

PIC16LF722/3/4/6/7			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
PIC16F722/3/4/6/7			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min.	Typ†	Max. +85°C	Max. +125°C	Units	Conditions	
							VDD	Note
	Power-down Base Current (IPD)(2)							
D027		—	0.06	0.7	5.0	µA	1.8	A/D Current **(Note 1, Note 4)**, no conversion in progress
		—	0.08	1.0	5.5	µA	3.0	
D027		—	6	10.7	18	µA	1.8	A/D Current **(Note 1, Note 4)**, no conversion in progress
		—	7	10.6	20	µA	3.0	
		—	7.2	11.9	22	µA	5.0	
D027A		—	250	400	—	µA	1.8	A/D Current **(Note 1, Note 4)**, conversion in progress
		—	250	400	—	µA	3.0	
D027A		—	280	430	—	µA	1.8	A/D Current **(Note 1, Note 4, Note 5)**, conversion in progress
		—	280	430	—	µA	3.0	
		—	280	430	—	µA	5.0	
D028		—	2.2	3.2	14.4	µA	1.8	Cap Sense Low Power Oscillator mode
		—	3.3	4.4	15.6	µA	3.0	
D028		—	6.5	13	21	µA	1.8	Cap Sense Low Power Oscillator mode
		—	8	14	23	µA	3.0	
		—	8	14	25	µA	5.0	
D028A		—	4.2	6	17	µA	1.8	Cap Sense Medium Power Oscillator mode
		—	6	7	18	µA	3.0	
D028A		—	8.5	15.5	23	µA	1.8	Cap Sense Medium Power Oscillator mode
		—	11	17	24	µA	3.0	
		—	11	18	27	µA	5.0	
D028B		—	12	14	25	µA	1.8	Cap Sense High Power Oscillator mode
		—	32	35	44	µA	3.0	
D028B		—	16	20	31	µA	1.8	Cap Sense High Power Oscillator mode
		—	36	41	50	µA	3.0	
		—	42	49	58	µA	5.0	

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

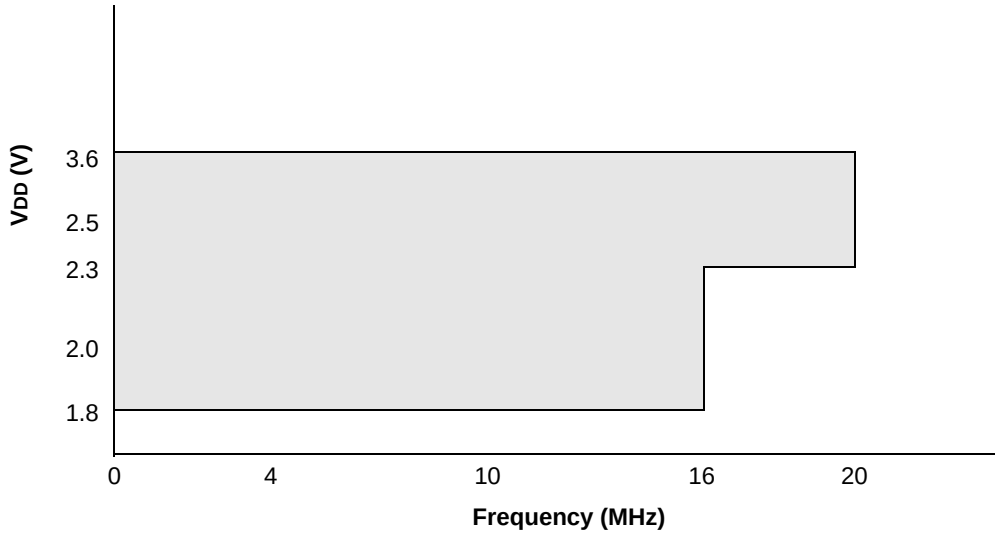
2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

3: Fixed Voltage Reference is automatically enabled whenever the BOR is enabled

4: A/D oscillator source is FRC

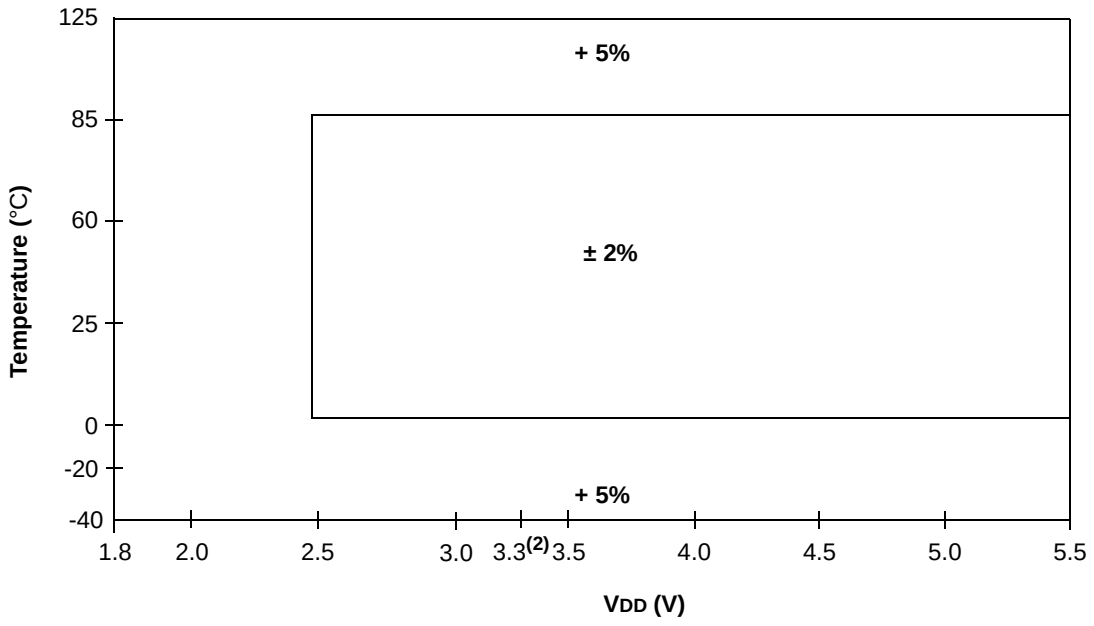
5: 0.1 µF capacitor on VCAP (RA0).

FIGURE 23-5: PIC16LF722/3/4/6/7 VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 23-1 for each Oscillator mode's supported frequencies.

FIGURE 23-6: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE



Note 1: This chart covers both regulator enabled and regulator disabled states.
2: Regulator Nominal voltage

FIGURE 24-13: PIC16F722/3/4/6/7 MAXIMUM IDD vs. VDD OVER FOSC, XT MODE, VCAP = 0.1 µF

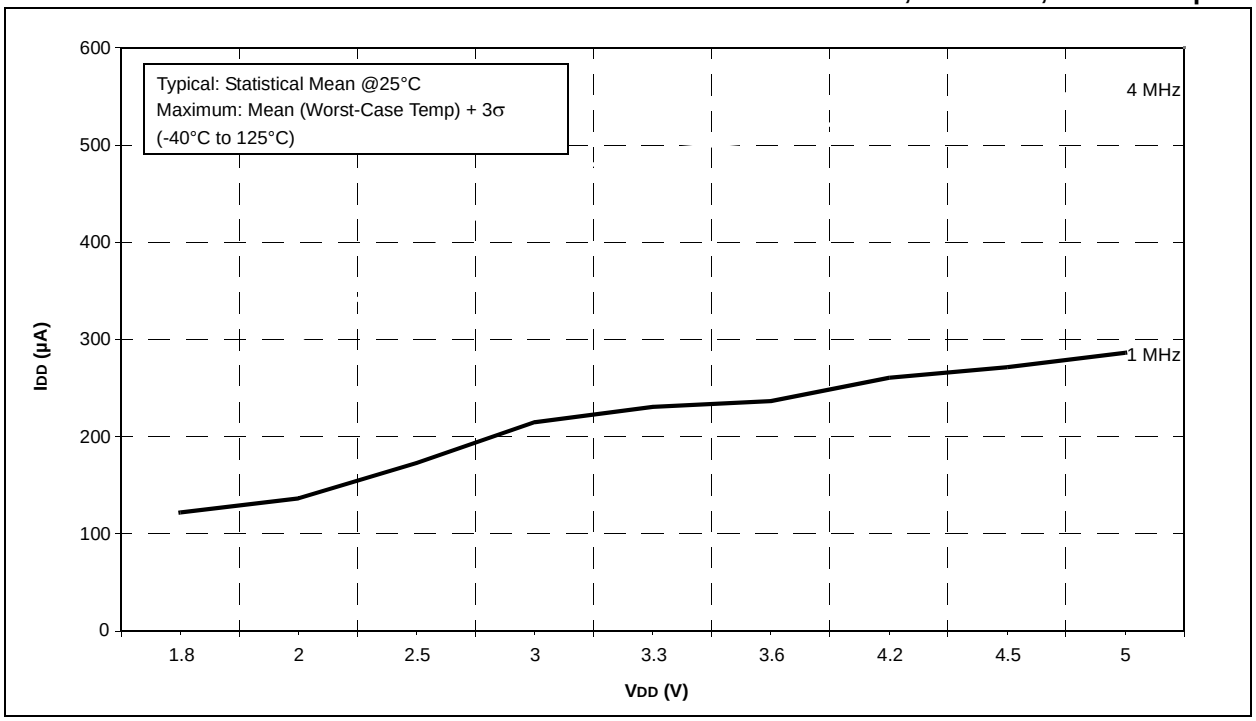


FIGURE 24-14: PIC16LF722/3/4/6/7 MAXIMUM IDD vs. VDD OVER FOSC, XT MODE

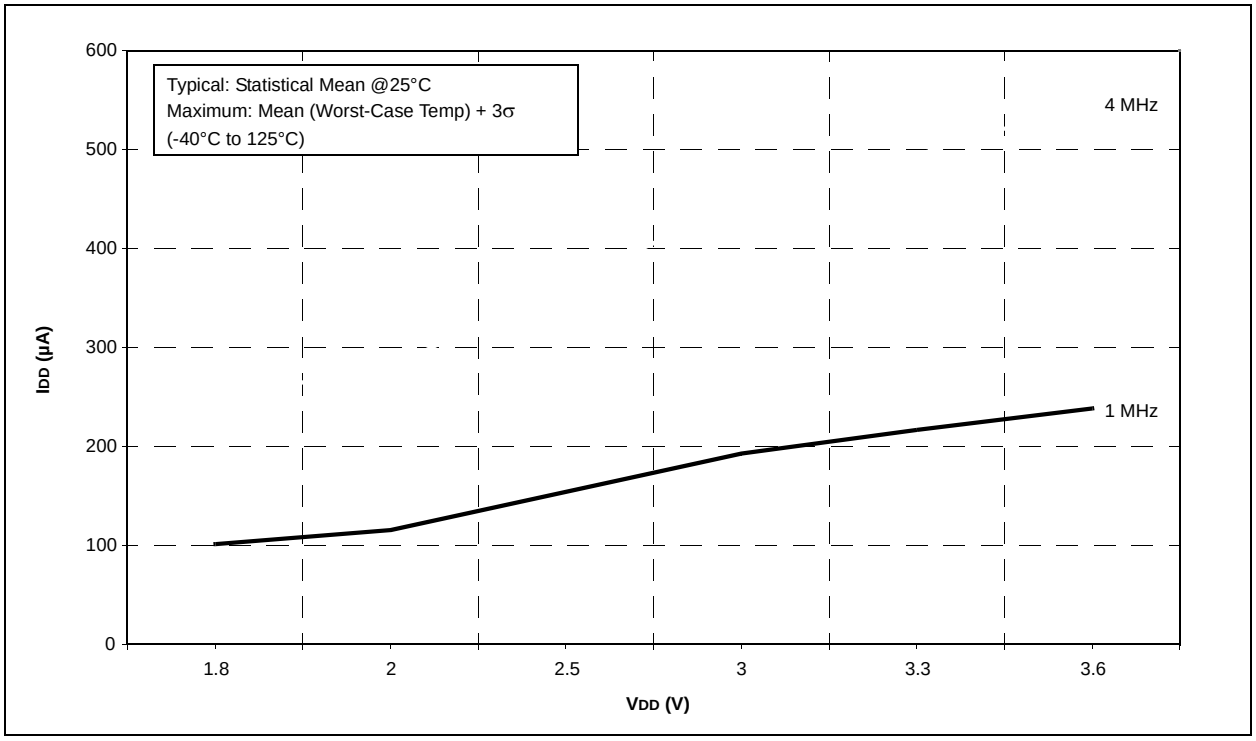


FIGURE 24-27: PIC16F722/3/4/6/7 MAXIMUM BASE I_{PD} vs. V_{DD}, V_{CAP} = 0.1 µF

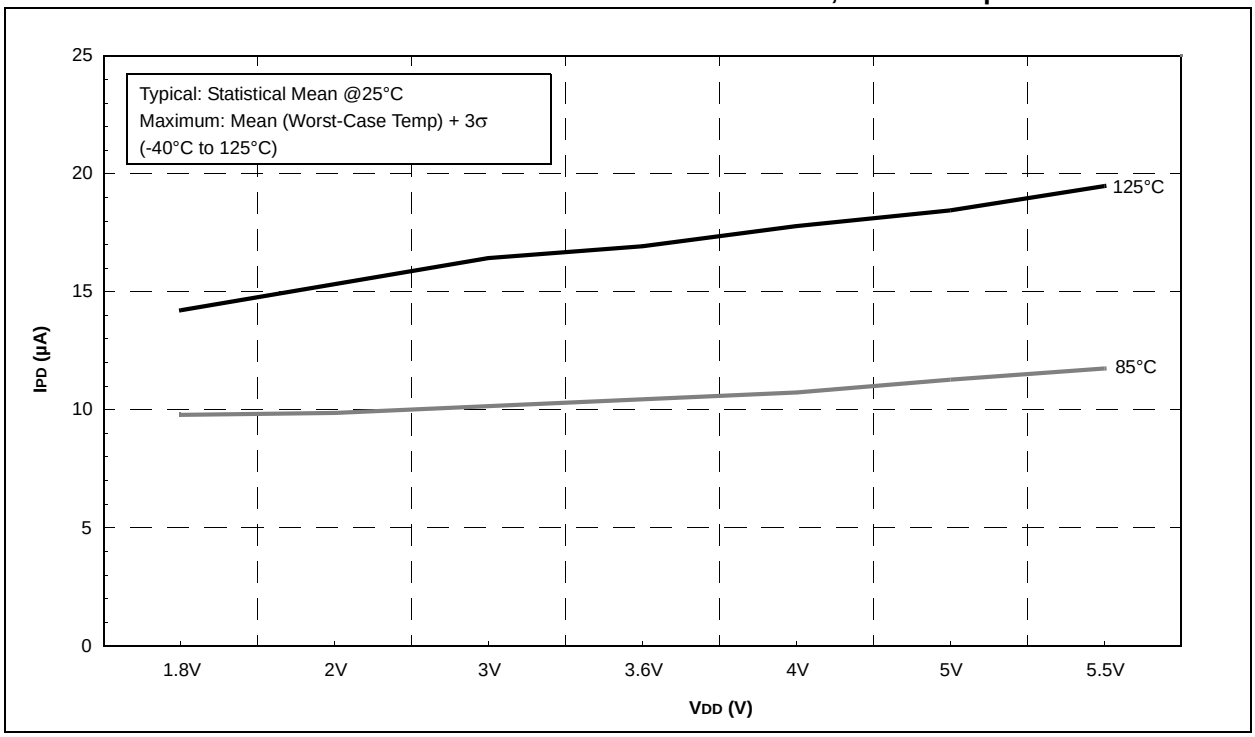


FIGURE 24-28: PIC16LF722/3/4/6/7 MAXIMUM BASE I_{PD} vs. V_{DD}

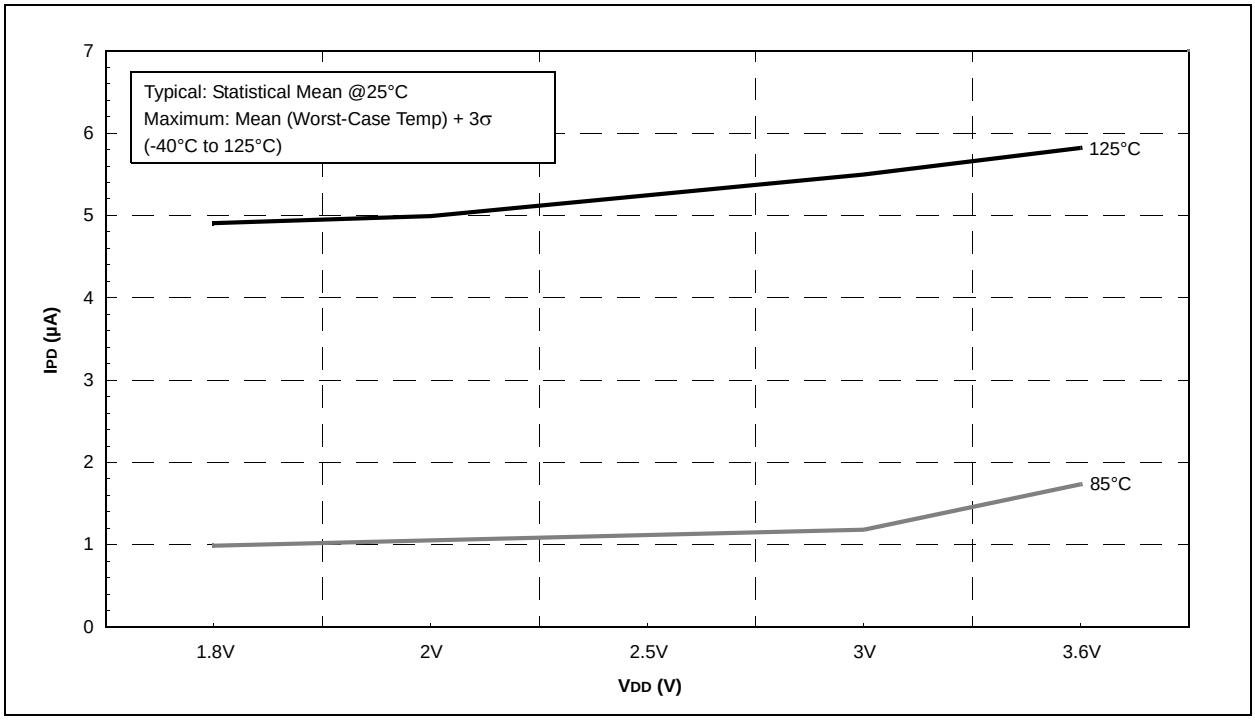


FIGURE 24-31: PIC16F722/3/4/6/7 FIXED VOLTAGE REFERENCE IPD VS. VDD, VCAP = 0.1 µF

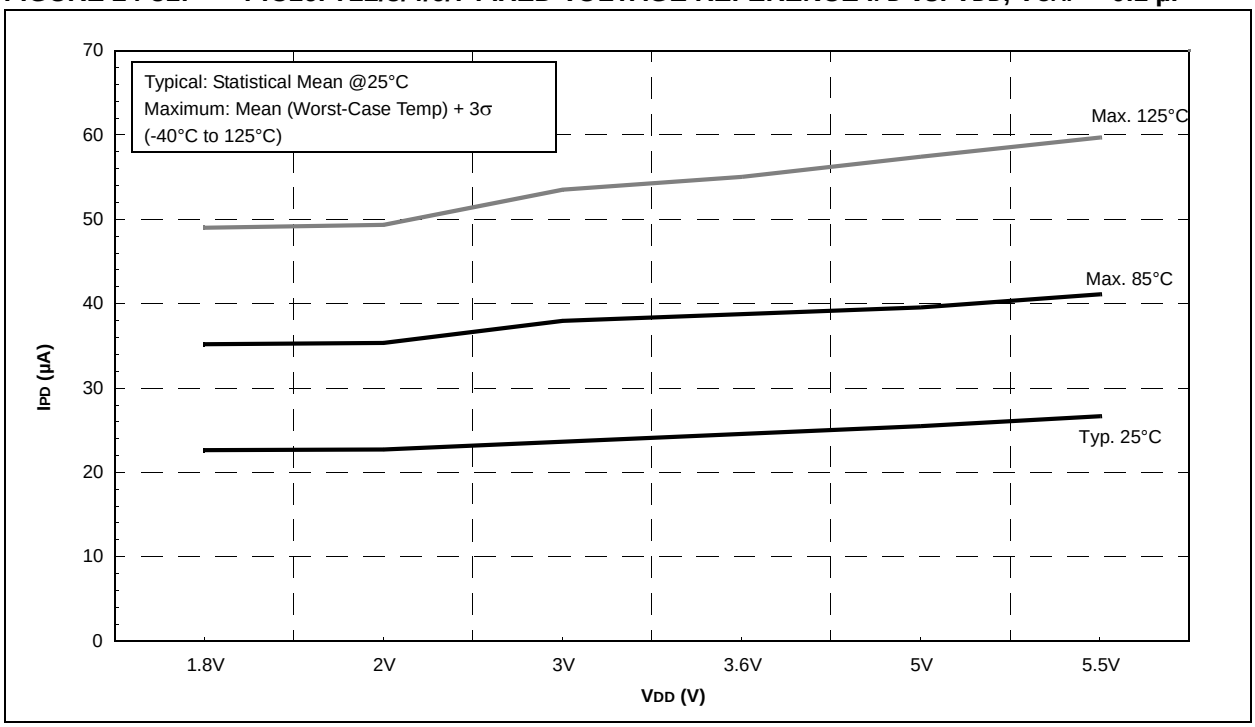


FIGURE 24-32: PIC16LF722/3/4/6/7 FIXED VOLTAGE REFERENCE IPD VS. VDD

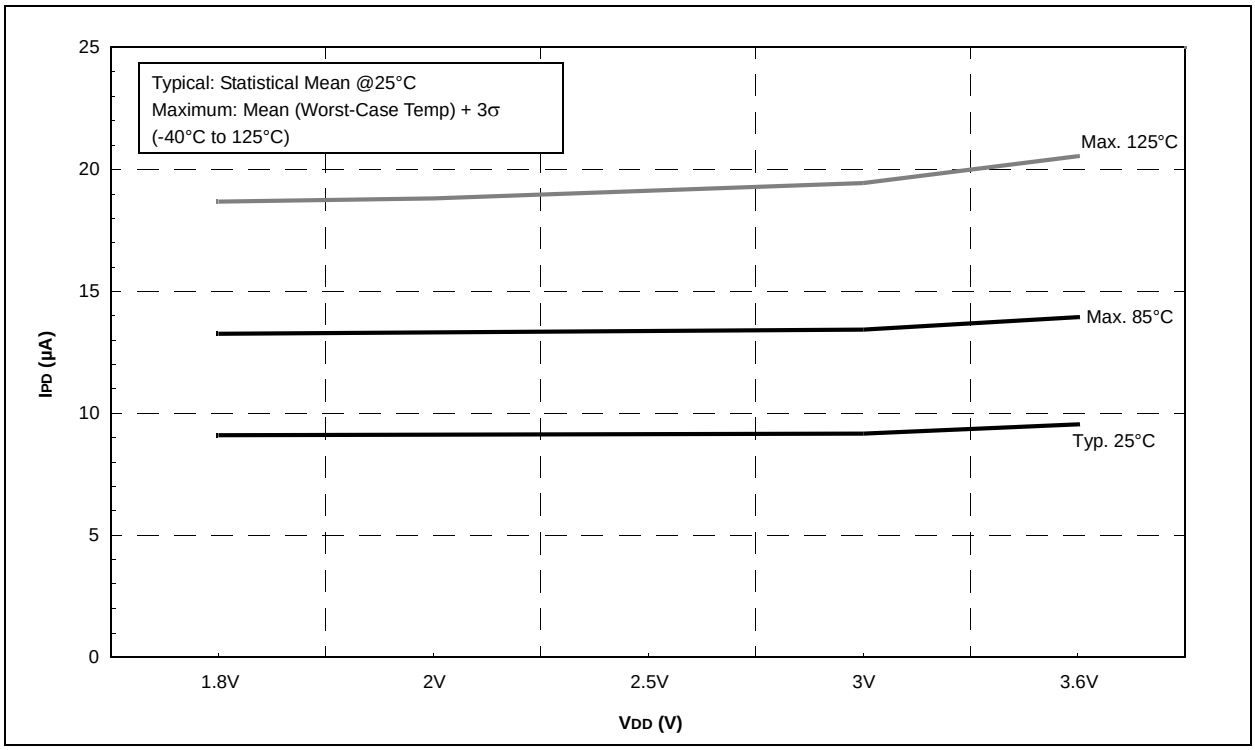


FIGURE 24-35: PIC16F722/3/4/6/7 CAP SENSE HIGH POWER IPD vs. VDD, VCAP = 0.1 µF

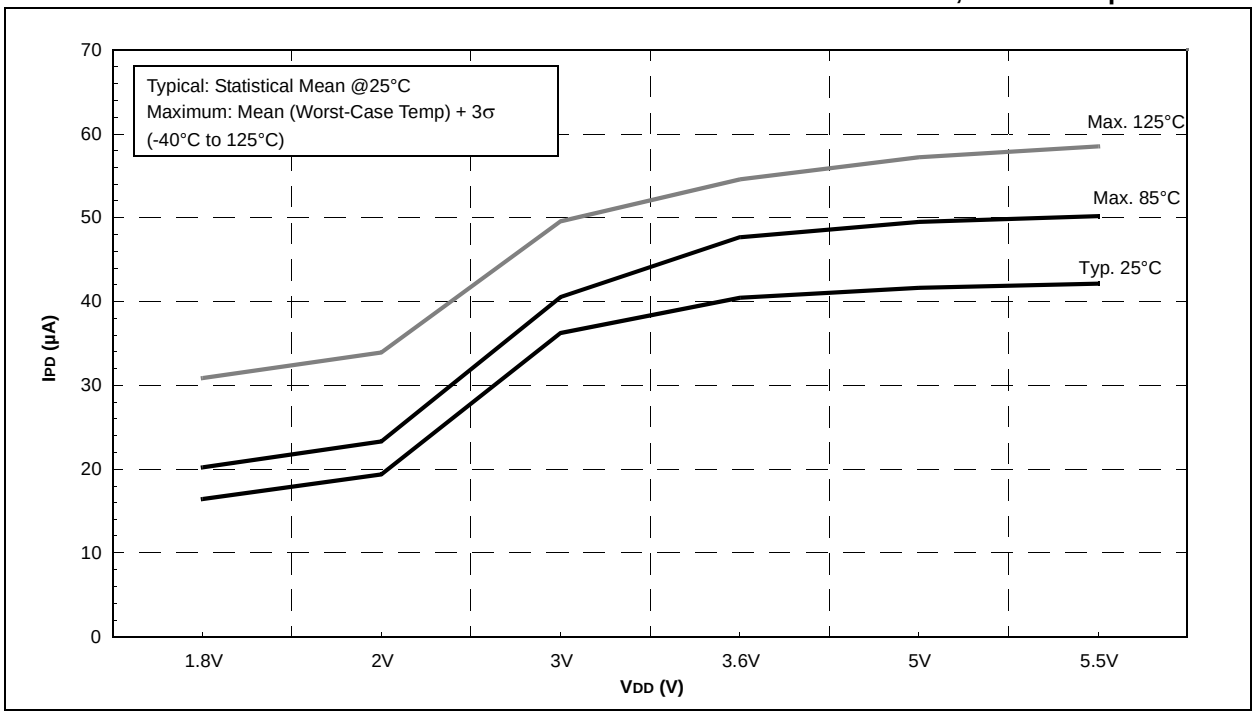


FIGURE 24-36: PIC16LF722/3/4/6/7 CAP SENSE HIGH POWER IPD vs. VDD

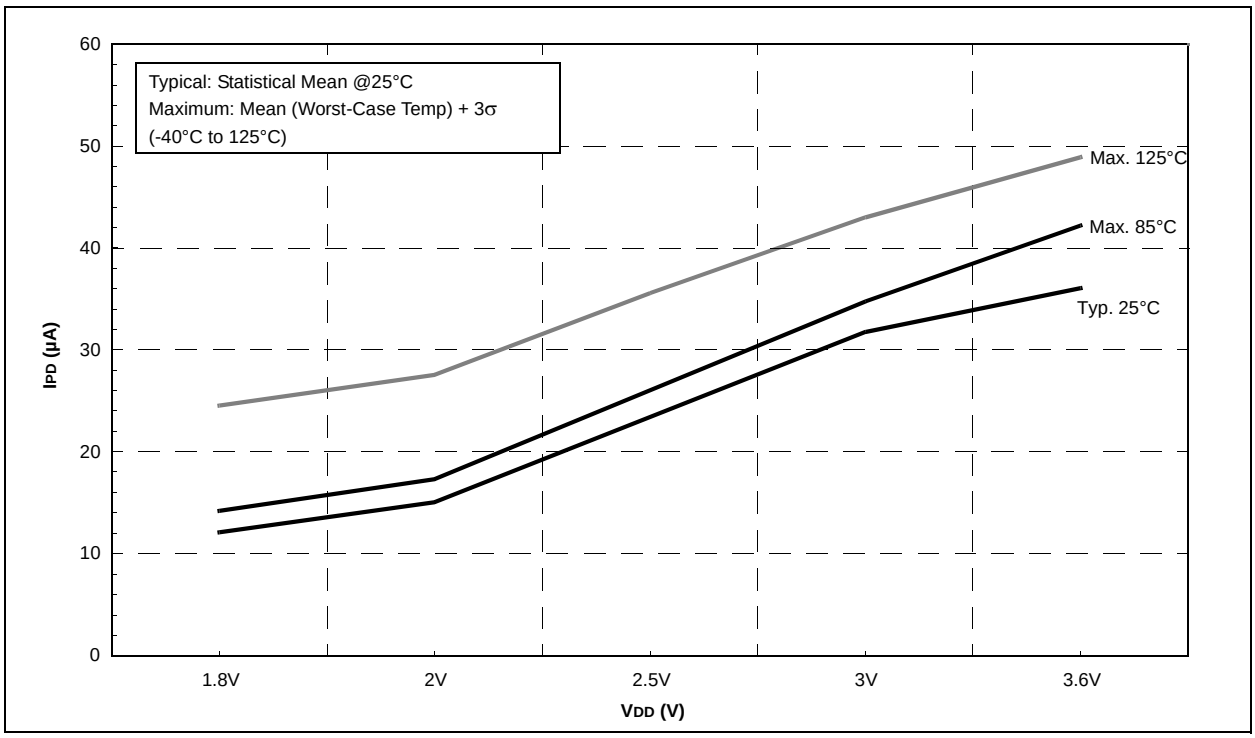


FIGURE 24-37: PIC16F722/3/4/6/7 CAP SENSE MEDIUM POWER IPD vs. VDD, VCAP = 0.1 µF

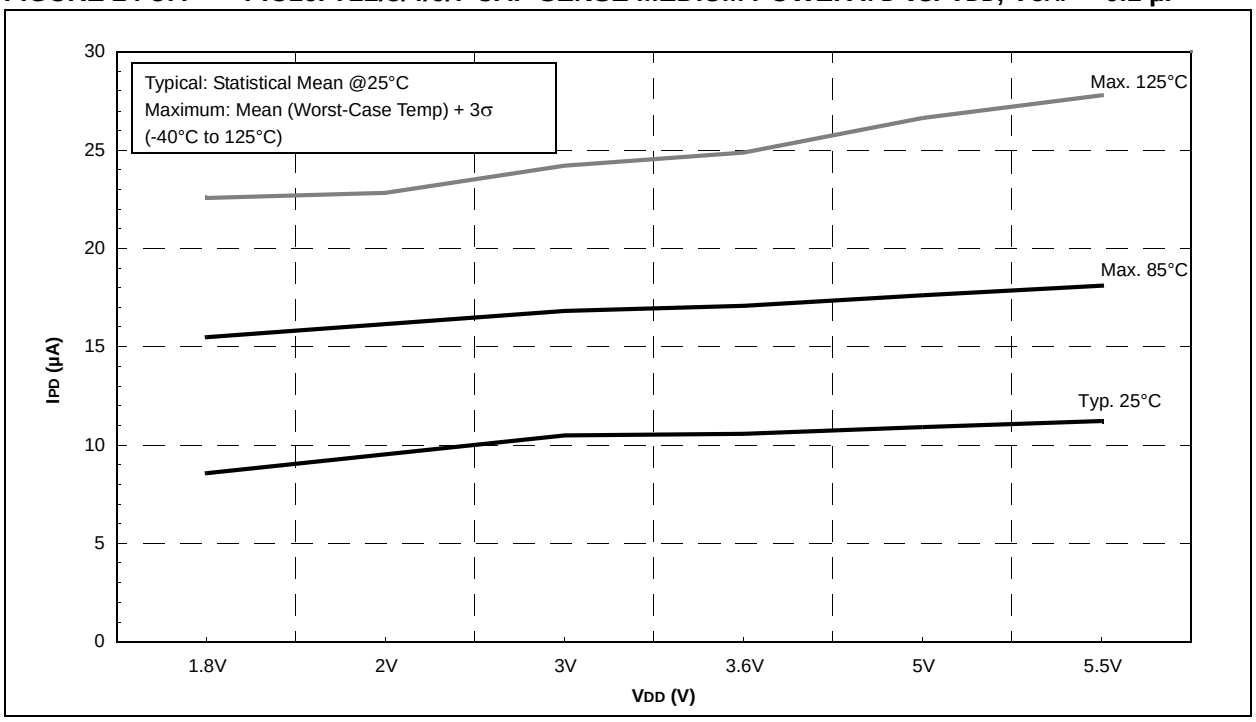


FIGURE 24-38: PIC16LF722/3/4/6/7 CAP SENSE MEDIUM POWER IPD vs. VDD