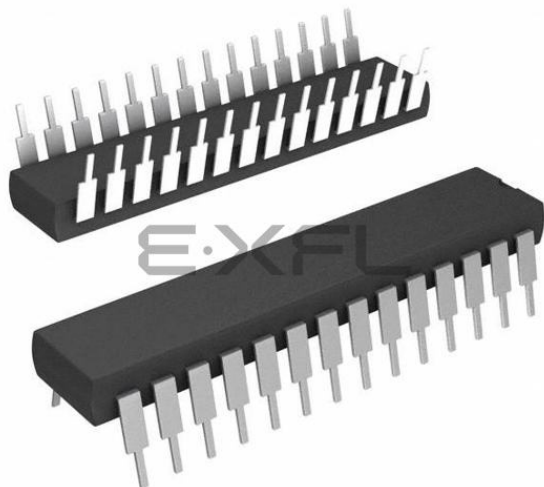




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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f726-i-sp

PIC16(L)F722/3/4/6/7

FIGURE 3-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{\text{MCLR}}$): CASE 1

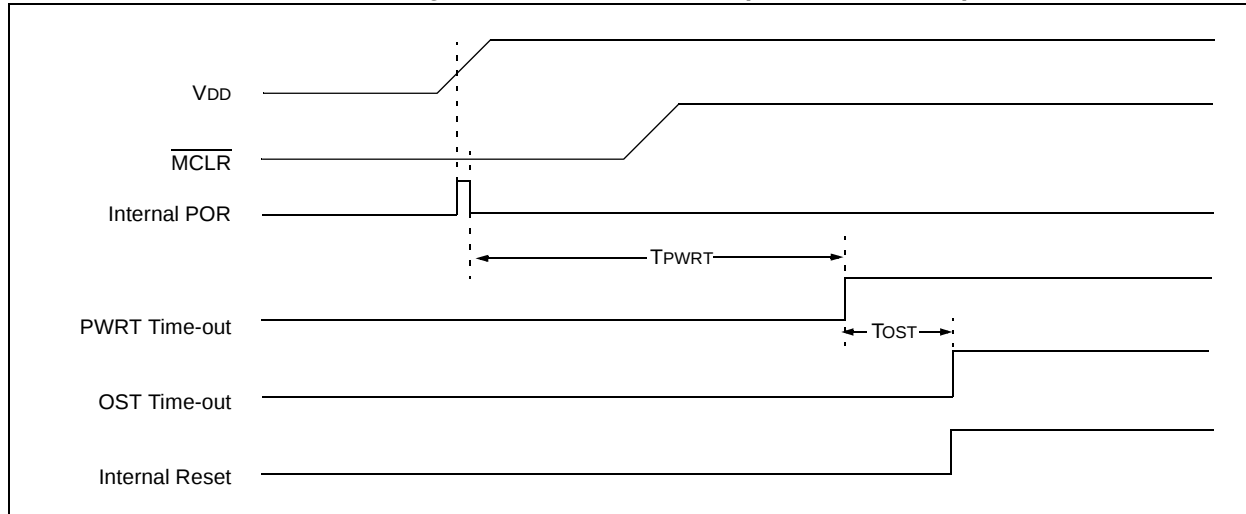


FIGURE 3-5: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{\text{MCLR}}$): CASE 2

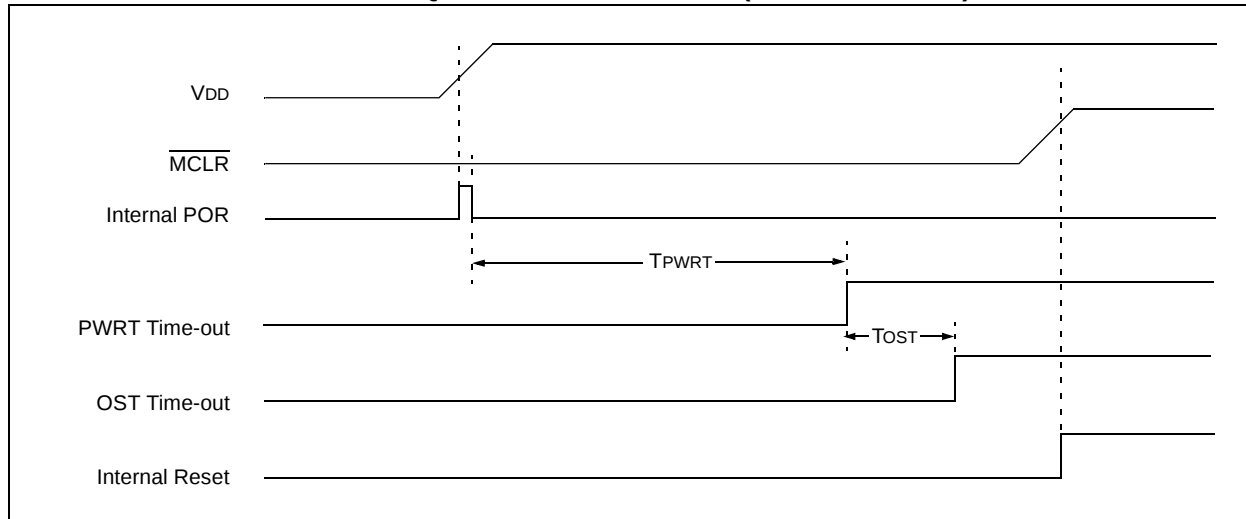
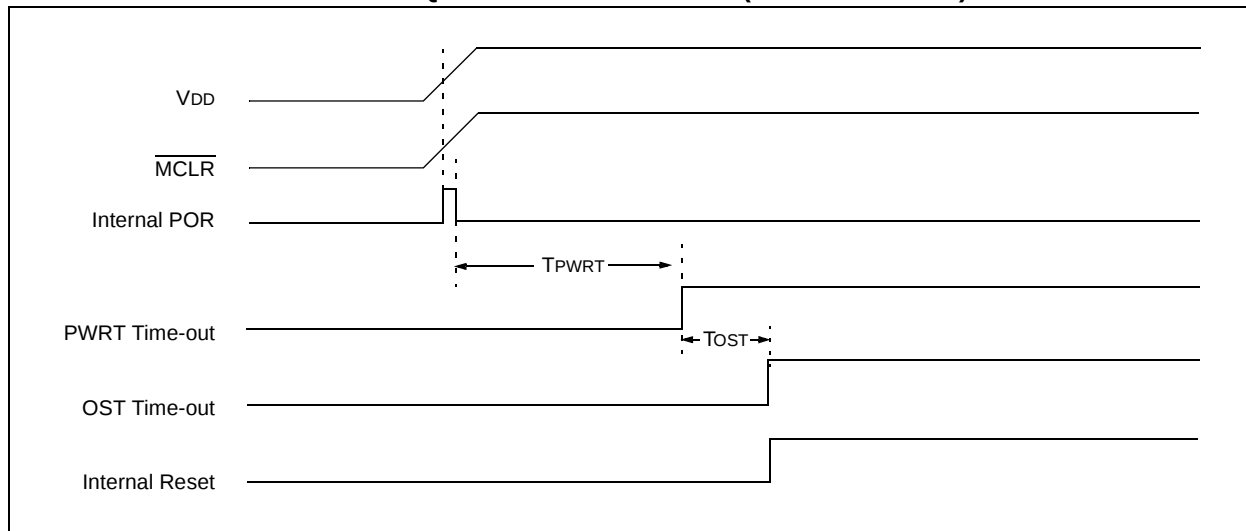


FIGURE 3-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ WITH VDD): CASE 3



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TABLE 3-4: INITIALIZATION CONDITION FOR REGISTERS (CONTINUED)

Register	Address	Power-on Reset/ Brown-out Reset ⁽¹⁾	MCLR Reset/ WDT Reset	Wake-up from Sleep through Interrupt/Time out
PCON	8Eh	---- --qq	---- --uu ^(1,5)	---- --uu
T1GCON	8Fh	0000 0x00	uuuu uxuu	uuuu uxuu
OSCCON	90h	--10 qq--	--10 qq--	--uu qq--
OSCTUNE	91h	--00 0000	--uu uuuu	--uu uuuu
PR2	92h	1111 1111	1111 1111	uuuu uuuu
SSPADD	93h	0000 0000	0000 0000	uuuu uuuu
SSPMSK	93h	1111 1111	1111 1111	uuuu uuuu
SSPSTAT	94h	0000 0000	0000 0000	uuuu uuuu
WPUB	95h	1111 1111	1111 1111	uuuu uuuu
IOCB	96h	0000 0000	0000 0000	uuuu uuuu
TXSTA	98h	0000 -010	0000 -010	uuuu -uuu
SPBRG	99h	0000 0000	0000 0000	uuuu uuuu
APFCON	9Ch	---- --00	---- --00	---- --uu
FVRCON	9Dh	q000 --00	q000 --00	uuuu --uu
ADCON1	9Fh	-000 --00	-000 --00	-uuu --uu
CPSCON0	108h	0--- 0000	0--- 0000	u--- uuuu
CPSCON1	109h	---- 0000	---- 0000	---- uuuu
PMDATL	10Ch	xxxx xxxx	xxxx xxxx	uuuu uuuu
PMADRL	10Dh	xxxx xxxx	xxxx xxxx	uuuu uuuu
PMDATH	10Eh	--xx xxxx	--xx xxxx	--uu uuuu
PMADRH	10Fh	---x xxxx	---x xxxx	---u uuuu
ANSELA	185h	--11 1111	--11 1111	--uu uuuu
ANSELB	186h	--11 1111	--11 1111	--uu uuuu
ANSELD ⁽⁶⁾	188h	1111 1111	1111 1111	uuuu uuuu
ANSELE	189h	---- -111	---- -111	---- -uuu
PMCON1	18Ch	1--- ---0	1--- ---0	u--- ---u

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

- Note**
- 1: If V_{DD} goes too low, Power-on Reset will be activated and registers will be affected differently.
 - 2: One or more bits in INTCON and/or PIR1 and PIR2 will be affected (to cause wake-up).
 - 3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
 - 4: See Table 3-5 for Reset value for specific condition.
 - 5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.
 - 6: PIC16F724/727/PIC16LF724/727 only.

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6.0 I/O PORTS

There are as many as 35 general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

6.1 Alternate Pin Function

The Alternate Pin Function Control (APFCON) register is used to steer specific peripheral input and output functions between different pins. The APFCON register is shown in Register 6-1. For this device family, the following functions can be moved between different pins.

- $\overline{SS}$ (Slave Select)
- CCP2

REGISTER 6-1: APFCON: ALTERNATE PIN FUNCTION CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	SSSEL	CCP2SEL
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'.

bit 1 **SSSEL:** $\overline{SS}$ Input Pin Selection bit

0 = $\overline{SS}$ function is on RA5/AN4/CPS7/ $\overline{SS}$ /VCAP

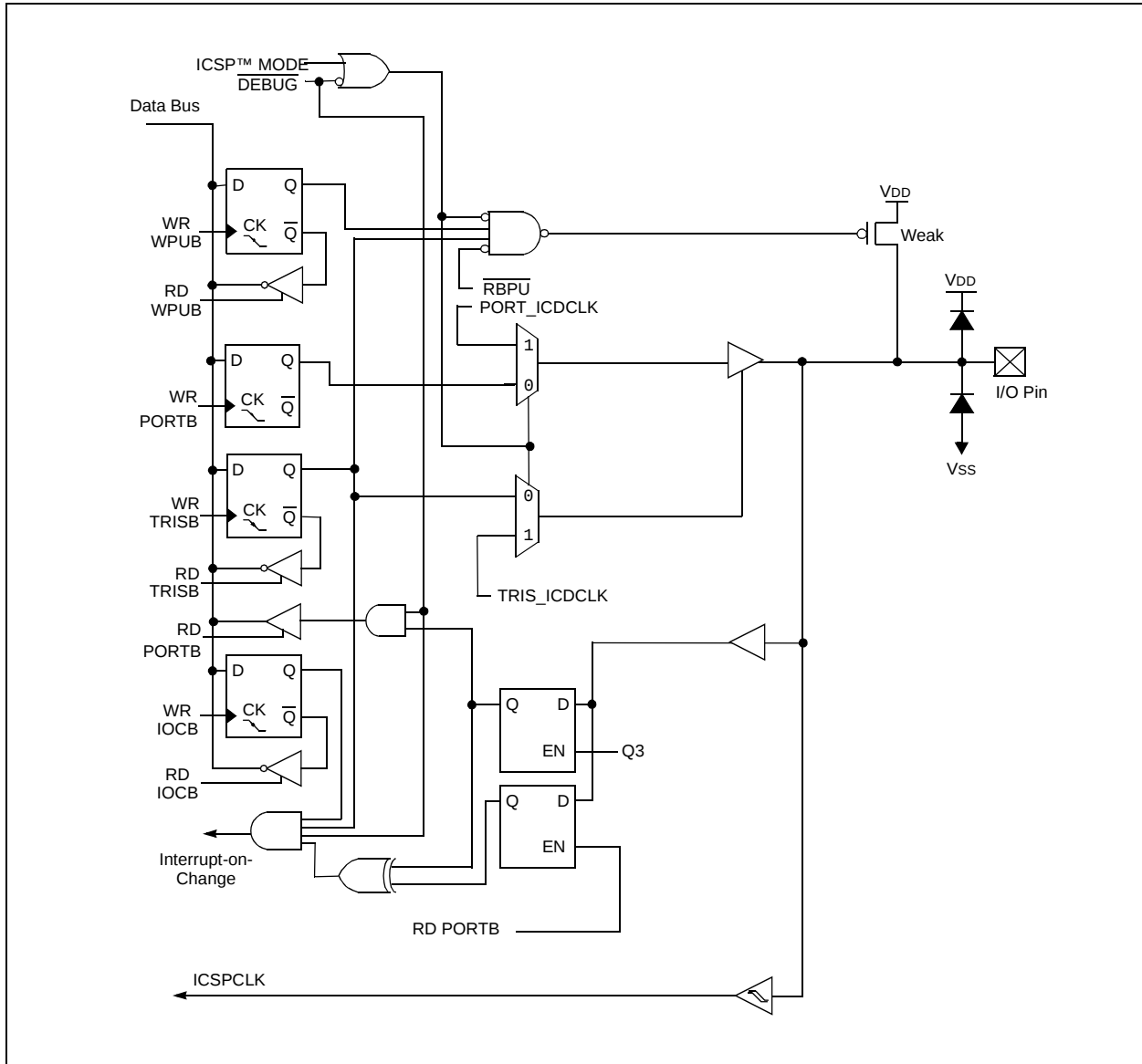
1 = $\overline{SS}$ function is on RA0/AN0/ $\overline{SS}$ /VCAP

bit 0 **CCP2SEL:** CCP2 Input/Output Pin Selection bit

0 = CCP2 function is on RC1/T1OSI/CCP2

1 = CCP2 function is on RB3/CCP2

FIGURE 6-11: BLOCK DIAGRAM OF RB6



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REGISTER 6-13: TRISD: PORTD TRI-STATE REGISTER⁽¹⁾

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **TRISD<7:0>**: PORTD Tri-State Control bits
1 = PORTD pin configured as an input (tri-stated)
0 = PORTD pin configured as an output

Note 1: TRISD is not implemented on PIC16F722/723/726/PIC16LF722/723/726 devices, read as '0'.

REGISTER 6-14: ANSEL: PORTD ANALOG SELECT REGISTER⁽²⁾

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **ANS<7:0>**: Analog Select between Analog or Digital Function on Pins RD<7:0>, respectively
0 = Digital I/O. Pin is assigned to port or Digital special function.
1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital Input buffer disabled.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

2: ANSEL register is not implemented on the PIC16F722/723/726/PIC16LF722/723/726. Read as '0'.

Note: PORTD is available on PIC16F724/LF724 and PIC16F727/LF727 only.

6.5.2 RD0/CPS8

Figure 6-21 shows the diagram for these pins. They are configurable to function as one of the following:

- a general purpose I/O
- a capacitive sensing input

6.5.3 RD1/CPS9

Figure 6-21 shows the diagram for these pins. They are configurable to function as one of the following:

- a general purpose I/O
- a capacitive sensing input

6.5.4 RD2/CPS10

Figure 6-21 shows the diagram for these pins. They are configurable to function as one of the following:

- a general purpose I/O
- a capacitive sensing input

6.5.5 RD3/CPS11

Figure 6-21 shows the diagram for these pins. They are configurable to function as one of the following:

- a general purpose I/O
- a capacitive sensing input

REGISTER 11-1: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBP}}\text{U}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **$\overline{\text{RBP}}\text{U}$** : PORTB Pull-up Enable bit
 1 = PORTB pull-ups are disabled
 0 = PORTB pull-ups are enabled by individual port latch values
- bit 6 **INTEDG**: Interrupt Edge Select bit
 1 = Interrupt on rising edge of INT pin
 0 = Interrupt on falling edge of INT pin
- bit 5 **T0CS**: TMR0 Clock Source Select bit
 1 = Transition on T0CKI pin or CPSOSC signal
 0 = Internal instruction cycle clock (Fosc/4)
- bit 4 **T0SE**: TMR0 Source Edge Select bit
 1 = Increment on high-to-low transition on T0CKI pin
 0 = Increment on low-to-high transition on T0CKI pin
- bit 3 **PSA**: Prescaler Assignment bit
 1 = Prescaler is assigned to the WDT
 0 = Prescaler is assigned to the Timer0 module
- bit 2-0 **PS<2:0>**: Prescaler Rate Select bits

BITS VALUE	TMR0 RATE	WDT RATE
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

TABLE 11-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CPSCON0	CPSON	—	—	—	CPSRNG1	CPSRNG0	CPSOUT	T0XCS	0 --- 0000	0 --- 0000
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
OPTION_REG	$\overline{\text{RBP}}\text{U}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111	1111 1111

Legend: — = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.

TABLE 15-3: SUMMARY OF REGISTERS ASSOCIATED WITH CAPTURE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	--11 1111	--11 1111
APFCON	—	—	—	—	—	—	SSSEL	CCP2SEL	---- --00	---- --00
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000
CCPRxL	Capture/Compare/PWM Register X Low Byte								xxxx xxxx	uuuu uuuu
CCPRxH	Capture/Compare/PWM Register X High Byte								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIE2	—	—	—	—	—	—	—	CCP2IE	---- --0	---- --0
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIR2	—	—	—	—	—	—	—	CCP2IF	---- --0	---- --0
T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	—	TMR1ON	0000 00-0	uuuu uu-u
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/DONE	T1GVAL	T1GSS1	T1GSS0	0000 0x00	0000 0x00
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

Legend: - = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Capture.

16.1.1.4 TSR Status

The TRMT bit of the TXSTA register indicates the status of the TSR register. This is a read-only bit. The TRMT bit is set when the TSR register is empty and is cleared when a character is transferred to the TSR register from the TXREG. The TRMT bit remains clear until all bits have been shifted out of the TSR register. No interrupt logic is tied to this bit, so the user has to poll this bit to determine the TSR status.

Note: The TSR register is not mapped in data memory, so it is not available to the user.

16.1.1.5 Transmitting 9-Bit Characters

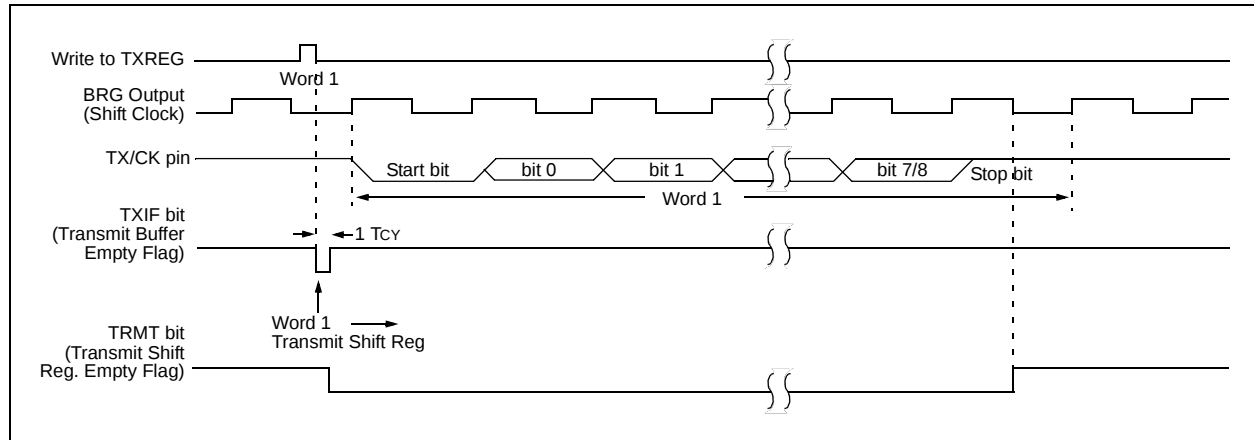
The AUSART supports 9-bit character transmissions. When the TX9 bit of the TXSTA register is set the AUSART will shift nine bits out for each character transmitted. The TX9D bit of the TXSTA register is the ninth, and Most Significant, data bit. When transmitting 9-bit data, the TX9D data bit must be written before writing the eight Least Significant bits into the TXREG. All nine bits of data will be transferred to the TSR shift register immediately after the TXREG is written.

A special 9-bit Address mode is available for use with multiple receivers. Refer to **Section 16.1.2.7 “Address Detection”** for more information on the Address mode.

16.1.1.6 Asynchronous Transmission Set-up:

1. Initialize the SPBRG register and the BRGH bit to achieve the desired baud rate (Refer to **Section 16.2 “AUSART Baud Rate Generator (BRG)”**).
2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
3. If 9-bit transmission is desired, set the TX9 control bit. A set ninth data bit will indicate that the eight Least Significant data bits are an address when the receiver is set for address detection.
4. Enable the transmission by setting the TXEN control bit. This will cause the TXIF interrupt bit to be set.
5. If interrupts are desired, set the TXIE interrupt enable bit of the PIE1 register. An interrupt will occur immediately provided that the GIE and PEIE bits of the INTCON register are also set.
6. If 9-bit transmission is selected, the ninth bit should be loaded into the TX9D data bit.
7. Load 8-bit data into the TXREG register. This will start the transmission.

FIGURE 16-3: ASYNCHRONOUS TRANSMISSION



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TABLE 16-2: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
RCREG	AUSART Receive Data Register								0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SPBRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	0000 0000	0000 0000
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Asynchronous Reception.

17.1.2 SLAVE MODE

For any SPI device acting as a slave, the data is transmitted and received as external clock pulses appear on SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

17.1.2.1 Slave Mode Operation

The SSP consists of a transmit/receive shift register (SSPSR) and a buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPBUF holds the data that was written to the SSPSR until the received data is ready.

The slave has no control as to when data will be clocked in or out of the device. All data that is to be transmitted, to a master or another slave, must be loaded into the SSPBUF register before the first clock pulse is received.

Once eight bits of data have been received:

- Received byte is moved to the SSPBUF register
- BF bit of the SSPSTAT register is set
- SSPIF bit of the PIR1 register is set

Any write to the SSPBUF register during transmission/reception of data will be ignored and the Write Collision Detect bit, WCOL of the SSPCON register, will be set. User software must clear the WCOL bit so that it can be determined if the following write(s) to the SSPBUF register completed successfully.

The user's firmware must read SSPBUF, clearing the BF flag, or the SSPOV bit of the SSPCON register will be set with the reception of the next byte and communication will be disabled.

A SPI module transmits and receives at the same time, occasionally causing dummy data to be transmitted/received. It is up to the user to determine which data is to be used and what can be discarded.

17.1.2.2 Enabling Slave I/O

To enable the serial port, the SSPEN bit of the SSPCON register must be set. If a Slave mode of operation is selected in the SSPM bits of the SSPCON register, the SDI, SDO, SCK pins will be assigned as serial port pins.

For these pins to function as serial port pins, they must have their corresponding data direction bits set or cleared in the associated TRIS register as follows:

- SDI configured as input
- SDO configured as output
- SCK configured as input

Optionally, a fourth pin, Slave Select ($\overline{SS}$) may be used in Slave mode. Slave Select may be configured to operate on one of the following pins via the SSSEL bit in the APFCON register.

- RA5/AN4/ $\overline{SS}$
- RA0/AN0/ $\overline{SS}$

Upon selection of a Slave Select pin, the appropriate bits must be set in the ANSELA and TRISA registers. Slave Select must be set as an input by setting the corresponding bit in TRISA, and digital I/O must be enabled on the $\overline{SS}$ pin by clearing the corresponding bit of the ANSELA register.

17.1.2.3 Slave Mode Setup

When initializing the SSP module to SPI Slave mode, compatibility must be ensured with the master device. This is done by programming the appropriate control bits of the SSPCON and SSPSTAT registers. These control bits allow the following to be specified:

- SCK as clock input
- Idle state of SCK (CKP bit)
- Data input sample phase (SMP bit)
- Output data on rising/falling edge of SCK (CKE bit)

Figure 17-4 and Figure 17-5 show example waveforms of Slave mode operation.

17.2.4 ADDRESSING

Once the SSP module has been enabled, it waits for a Start condition to occur. Following the Start condition, the eight bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock line (SCL).

17.2.4.1 7-bit Addressing

In 7-bit Addressing mode (Figure 17-10), the value of register SSPSR<7:1> is compared to the value of register SSPADD<7:1>. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following events occur:

- The SSPSR register value is loaded into the SSPBUF register.
- The BF bit is set.
- An ACK pulse is generated.
- SSP interrupt flag bit, SSPIF of the PIR1 register, is set (interrupt is generated if enabled) on the falling edge of the ninth SCL pulse.

17.2.4.2 10-bit Addressing

In 10-bit Address mode, two address bytes need to be received by the slave (Figure 17-11). The five Most Significant bits (MSBs) of the first address byte specify if it is a 10-bit address. The R/W bit of the SSPSTAT register must specify a write so the slave device will receive the second address byte. For a 10-bit address, the first byte would equal '1111 0 A9 A8 0', where A9 and A8 are the two MSBs of the address.

The sequence of events for 10-bit address is as follows for reception:

1. Load SSPADD register with high byte of address.
2. Receive first (high) byte of address (bits SSPIF, BF and UA of the SSPSTAT register are set).
3. Read the SSPBUF register (clears bit BF).
4. Clear the SSPIF flag bit.
5. Update the SSPADD register with second (low) byte of address (clears UA bit and releases the SCL line).
6. Receive low byte of address (bits SSPIF, BF and UA are set).
7. Update the SSPADD register with the high byte of address. If match releases SCL line, this will clear bit UA.
8. Read the SSPBUF register (clears bit BF).
9. Clear flag bit SSPIF.

If data is requested by the master, once the slave has been addressed:

1. Receive repeated Start condition.
2. Receive repeat of high byte address with R/W = 1, indicating a read.
3. BF bit is set and the CKP bit is cleared, stopping SCL and indicating a read request.
4. SSPBUF is written, setting BF, with the data to send to the master device.
5. CKP is set in software, releasing the SCL line.

17.2.4.3 Address Masking

The Address Masking register (SSPMSK) is only accessible while the SSPM bits of the SSPCON register are set to '1001'. In this register, the user can select which bits of a received address the hardware will compare when determining an address match. Any bit that is set to a zero in the SSPMSK register, the corresponding bit in the received address byte and SSPADD register are ignored when determining an address match. By default, the register is set to all ones, requiring a complete match of a 7-bit address or the lower eight bits of a 10-bit address.

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17.2.7 CLOCK STRETCHING

During any SCL low phase, any device on the I²C bus may hold the SCL line low and delay, or pause, the transmission of data. This “stretching” of a transmission allows devices to slow down communication on the bus. The SCL line must be constantly sampled by the master to ensure that all devices on the bus have released SCL for more data.

Stretching usually occurs after an $\overline{\text{ACK}}$ bit of a transmission, delaying the first bit of the next byte. The SSP module hardware automatically stretches for two conditions:

- After a 10-bit address byte is received (update SSPADD register)
- Anytime the CKP bit of the SSPCON register is cleared by hardware

The module will hold SCL low until the CKP bit is set. This allows the user slave software to update SSPBUF with data that may not be readily available. In 10-bit addressing modes, the SSPADD register must be updated after receiving the first and second address bytes. The SSP module will hold the SCL line low until the SSPADD has a byte written to it. The UA bit of the SSPSTAT register will be set, along with SSPIF, indicating an address update is needed.

17.2.8 FIRMWARE MASTER MODE

Master mode of operation is supported in firmware using interrupt generation on the detection of the Start and Stop conditions. The Stop (P) and Start (S) bits of the SSPSTAT register are cleared from a Reset or when the SSP module is disabled (SSPEN cleared). The Stop (P) and Start (S) bits will toggle based on the Start and Stop conditions. Control of the I²C bus may be taken when the P bit is set or the bus is Idle and both the S and P bits are clear.

In Firmware Master mode, the SCL and SDA lines are manipulated by setting/clearing the corresponding TRIS bit(s). The output level is always low, irrespective of the value(s) in the corresponding PORT register bit(s). When transmitting a ‘1’, the TRIS bit must be set (input) and a ‘0’, the TRIS bit must be clear (output).

The following events will cause the SSP Interrupt Flag bit, SSPIF, to be set (SSP Interrupt will occur if enabled):

- Start condition
- Stop condition
- Data transfer byte transmitted/received

Firmware Master Mode of operation can be done with either the Slave mode Idle (SSPM<3:0> = 1011), or with either of the Slave modes in which interrupts are enabled. When both master and slave functionality is enabled, the software needs to differentiate the source(s) of the interrupt.

Refer to Application Note AN554, *Software Implementation of I²C™ Bus Master* (DS00554) for more information.

17.2.9 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allow the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the SSP module is disabled. The Stop (P) and Start (S) bits will toggle based on the Start and Stop conditions. Control of the I²C bus may be taken when the P bit of the SSPSTAT register is set or when the bus is Idle, and both the S and P bits are clear. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the Stop condition occurs.

In Multi-Master operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and a low level is present, the device needs to release the SDA and SCL lines (set TRIS bits). There are two stages where this arbitration of the bus can be lost. They are the Address Transfer and Data Transfer stages.

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage, communication to the device may be in progress. If addressed, an ACK pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to re-transfer the data at a later time.

Refer to Application Note AN578, *Use of the SSP Module in the I²C™ Multi-Master Environment* (DS00578) for more information.

22.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

22.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

22.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/librarian features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

22.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

PIC16(L)F722/3/4/6/7

23.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings^(†)

Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to VSS, PIC16F72X	-0.3V to +6.5V
Voltage on VCAP pin with respect to VSS, PIC16F72X	-0.3V to +4.0V
Voltage on VDD with respect to VSS, PIC16LF72X	-0.3V to +4.0V
Voltage on $\overline{\text{MCLR}}$ with respect to VSS	-0.3V to +9.0V
Voltage on all other pins with respect to VSS	-0.3V to (VDD + 0.3V)
Total power dissipation ⁽¹⁾	800 mW
Maximum current out of VSS pin	95 mA
Maximum current into VDD pin	70 mA
Clamp current, I _K (V _{PIN} < 0 or V _{PIN} > VDD).....	± 20 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin.....	25 mA
Maximum current sunk by all ports ⁽²⁾ , -40°C ≤ T _A ≤ +85°C for industrial	200 mA
Maximum current sunk by all ports ⁽²⁾ , -40°C ≤ T _A ≤ +125°C for extended	90 mA
Maximum current sourced by all ports ⁽²⁾ , 40°C ≤ T _A ≤ +85°C for industrial	140 mA
Maximum current sourced by all ports ⁽²⁾ , -40°C ≤ T _A ≤ +125°C for extended	65 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

PIC16(L)F722/3/4/6/7

TABLE 23-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)								
Operating Temperature -40°C ≤ TA ≤ +125°C								
Param No.	Sym.	Characteristic		Min.	Typ†	Max.	Units	Conditions
40*	Tr0H	T0CKI High Pulse Width	No Prescaler	0.5 Tcy + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	Tr0L	T0CKI Low Pulse Width	No Prescaler	0.5 Tcy + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	Tr0P	T0CKI Period		Greater of: 20 or $\frac{Tcy + 40}{N}$	—	—	ns	N = prescale value (2, 4, ..., 256)
45*	Tt1H	T1CKI High Time	Synchronous, No Prescaler	0.5 Tcy + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, No Prescaler	0.5 Tcy + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
47*	Tt1P	T1CKI Input Period	Synchronous	Greater of: 30 or $\frac{Tcy + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	60	—	—	ns	
48	Ft1	Timer1 Oscillator Input Frequency Range (oscillator enabled by setting bit T1OSCEN)		32.4	32.768	33.1	kHz	
49*	TCKEZTMR1	Delay from External Clock Edge to Timer Increment		2 Tosc	—	7 Tosc	—	Timers in Sync mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 23-11: CAPTURE/COMPARE/PWM TIMINGS (CCP)

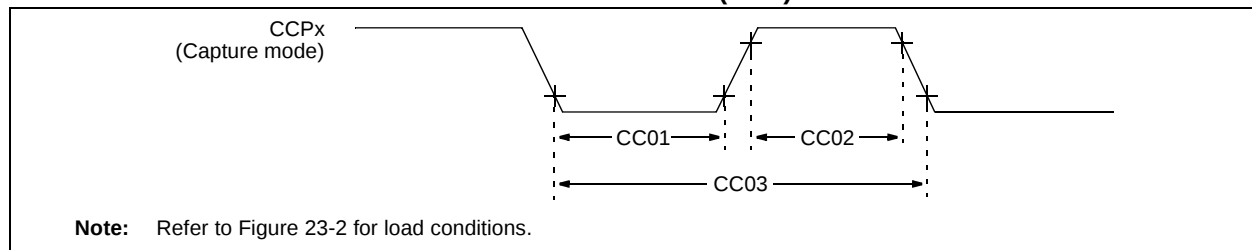


TABLE 23-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP)

Standard Operating Conditions (unless otherwise stated)								
Operating Temperature -40°C ≤ TA ≤ +125°C								
Param No.	Sym.	Characteristic		Min.	Typ†	Max.	Units	Conditions
CC01*	TccL	CCPx Input Low Time	No Prescaler	0.5TcY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC02*	TccH	CCPx Input High Time	No Prescaler	0.5TcY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC03*	TccP	CCPx Input Period		$\frac{3TcY + 40}{N}$	—	—	ns	N = prescale value (1, 4 or 16)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 23-14: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

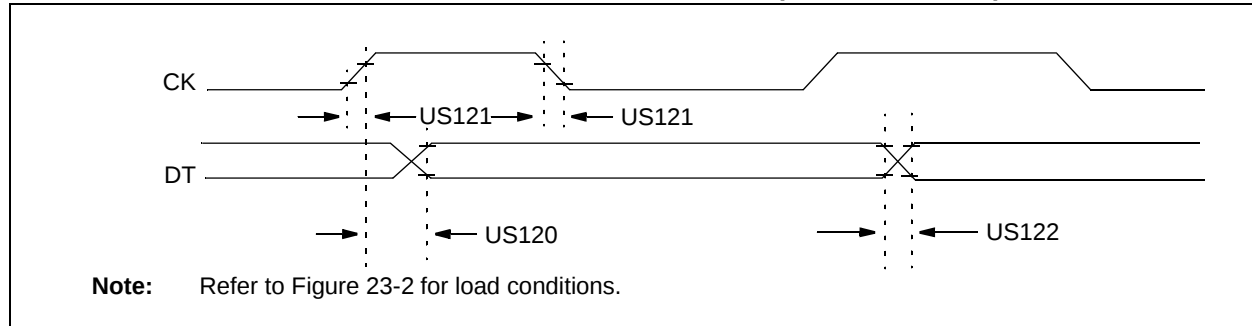


TABLE 23-9: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$							
Param. No.	Symbol	Characteristic		Min.	Max.	Units	Conditions
US120	TCKH2DTV	SYNC XMIT (Master and Slave) Clock high to data-out valid	3.0-5.5V	—	80	ns	
			1.8-5.5V	—	100	ns	
US121	TCKRF	Clock out rise time and fall time (Master mode)	3.0-5.5V	—	45	ns	
			1.8-5.5V	—	50	ns	
US122	TDTRF	Data-out rise time and fall time	3.0-5.5V	—	45	ns	
			1.8-5.5V	—	50	ns	

FIGURE 23-15: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

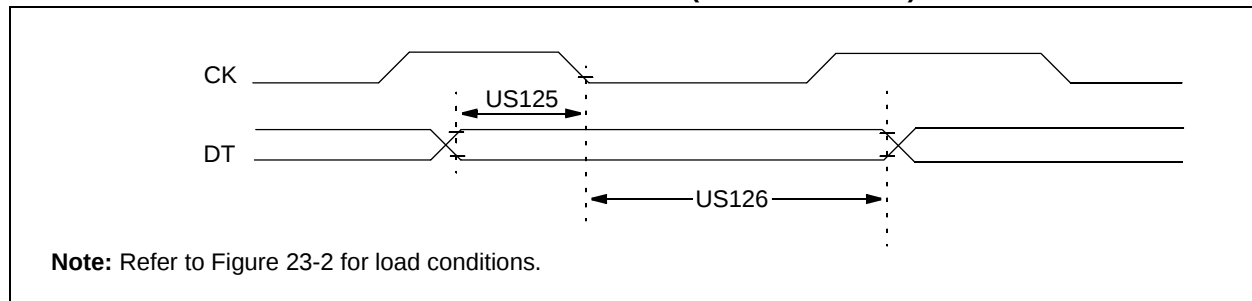


TABLE 23-10: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)						
Operating Temperature -40°C ≤ TA ≤ +125°C						
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Conditions
US125	TdTV2CKL	<u>SYNC RCV (Master and Slave)</u> Data-hold before CK ↓ (DT hold time)	10	—	ns	
US126	TcKL2DTL	Data-hold after CK ↓ (DT hold time)	15	—	ns	

FIGURE 24-11: PIC16F722/3/4/6/7 TYPICAL I_{DD} vs. F_{OSC} OVER V_{DD} , HS MODE, $V_{CAP} = 0.1 \mu F$

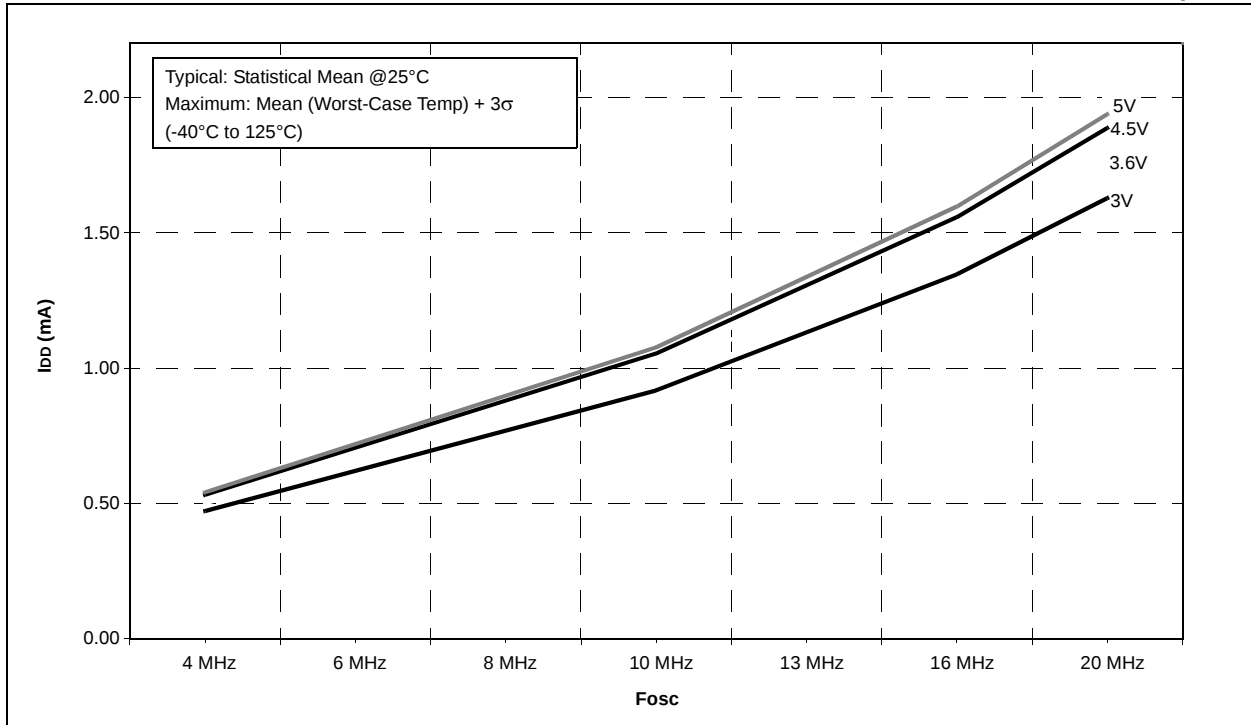


FIGURE 24-12: PIC16LF722/3/4/6/7 TYPICAL I_{DD} vs. F_{OSC} OVER V_{DD} , HS MODE

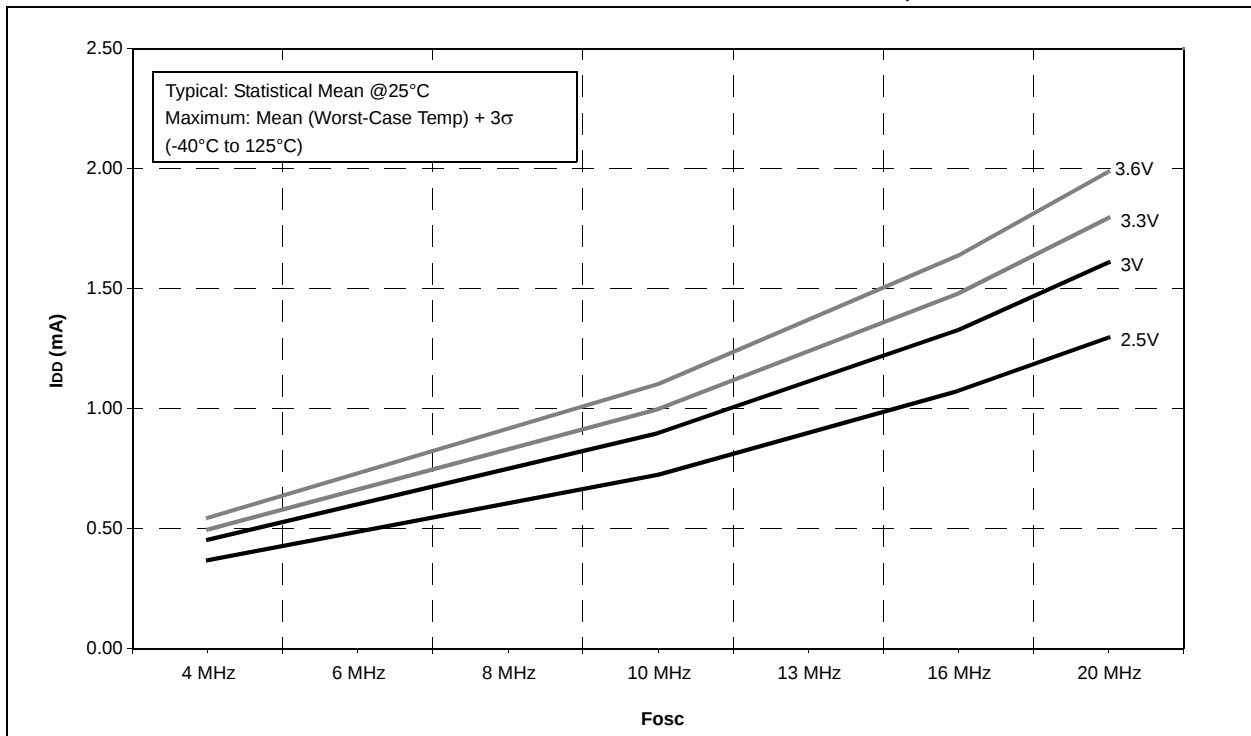


FIGURE 24-59: PIC16F722/3/4/6/7 WDT TIME-OUT PERIOD

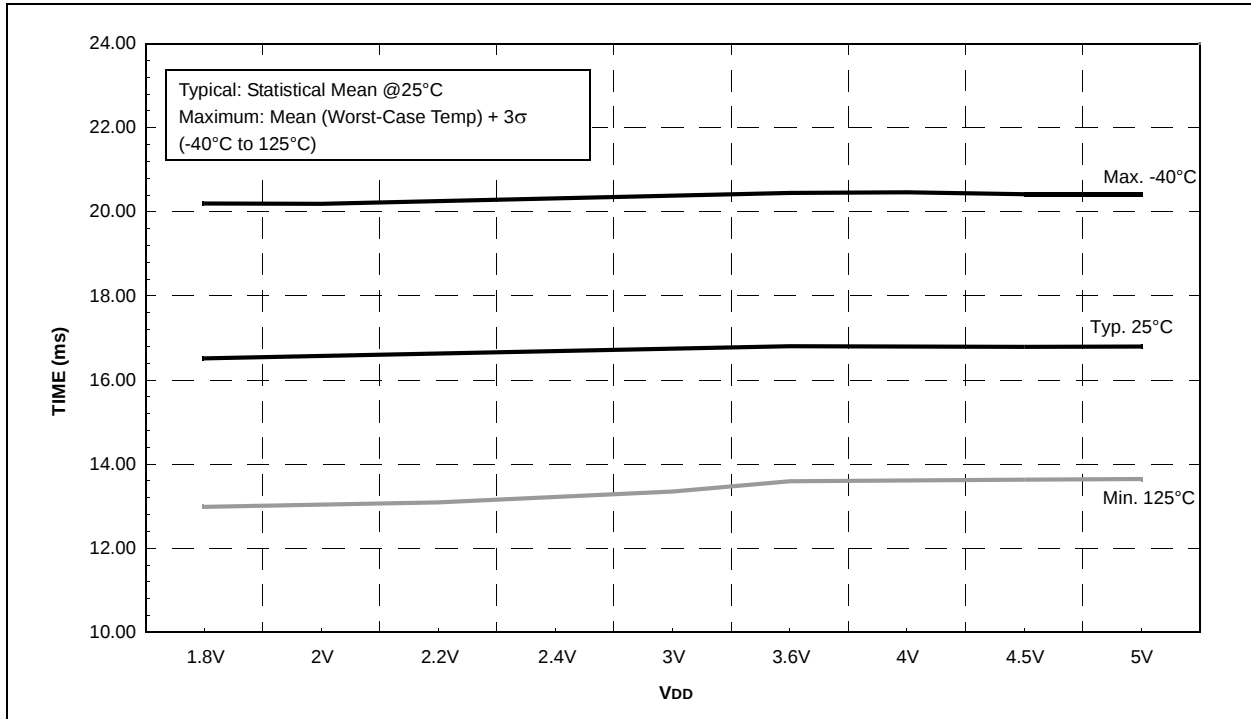
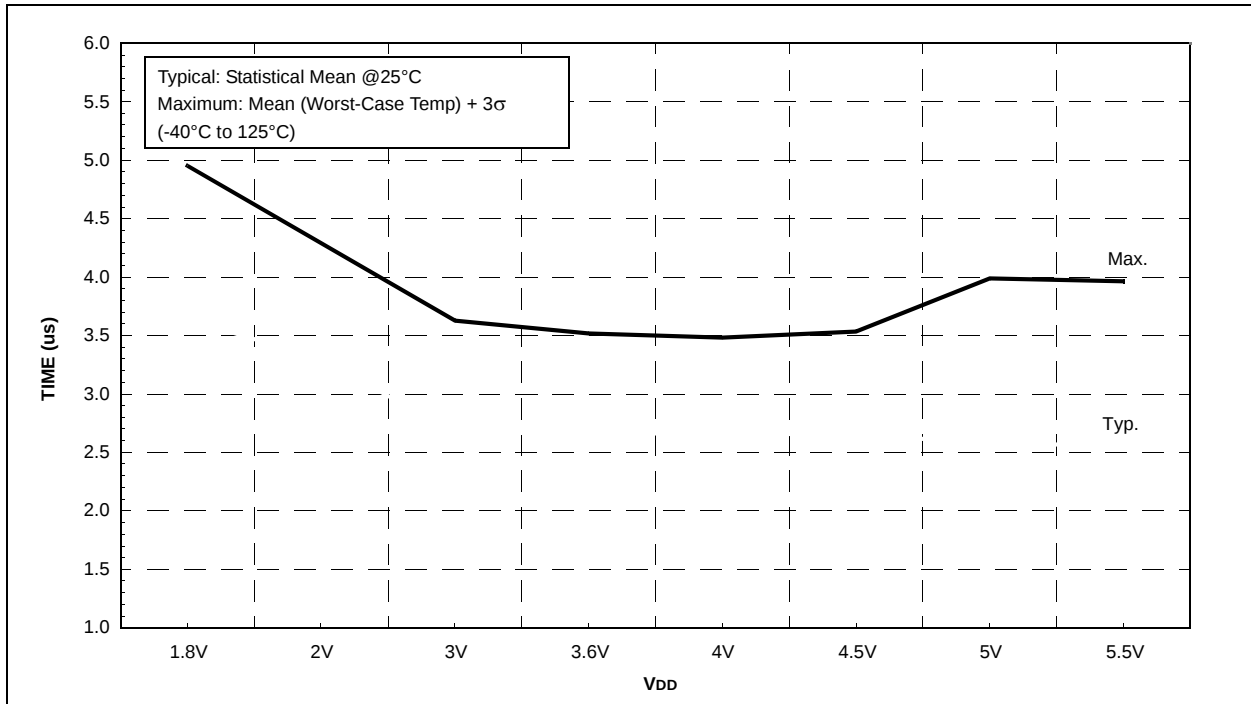


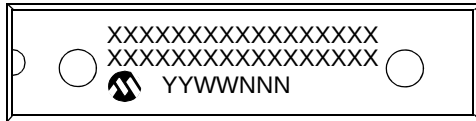
FIGURE 24-60: PIC16F722/3/4/6/7 HFINTOSC WAKE-UP FROM SLEEP START-UP TIME



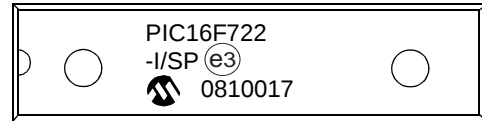
25.0 PACKAGING INFORMATION

25.1 Package Marking Information

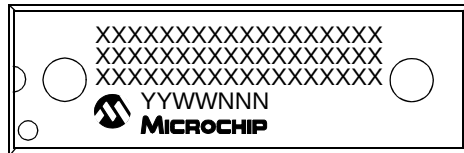
28-Lead SPDIP



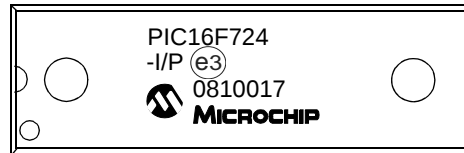
Example



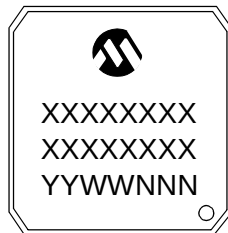
40-Lead PDIP



Example



28-Lead QFN/UQFN



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC® designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

- * Standard PICmicro® device marking consists of Microchip part number, year code, week code and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.