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What is "Embedded - Microcontrollers"?

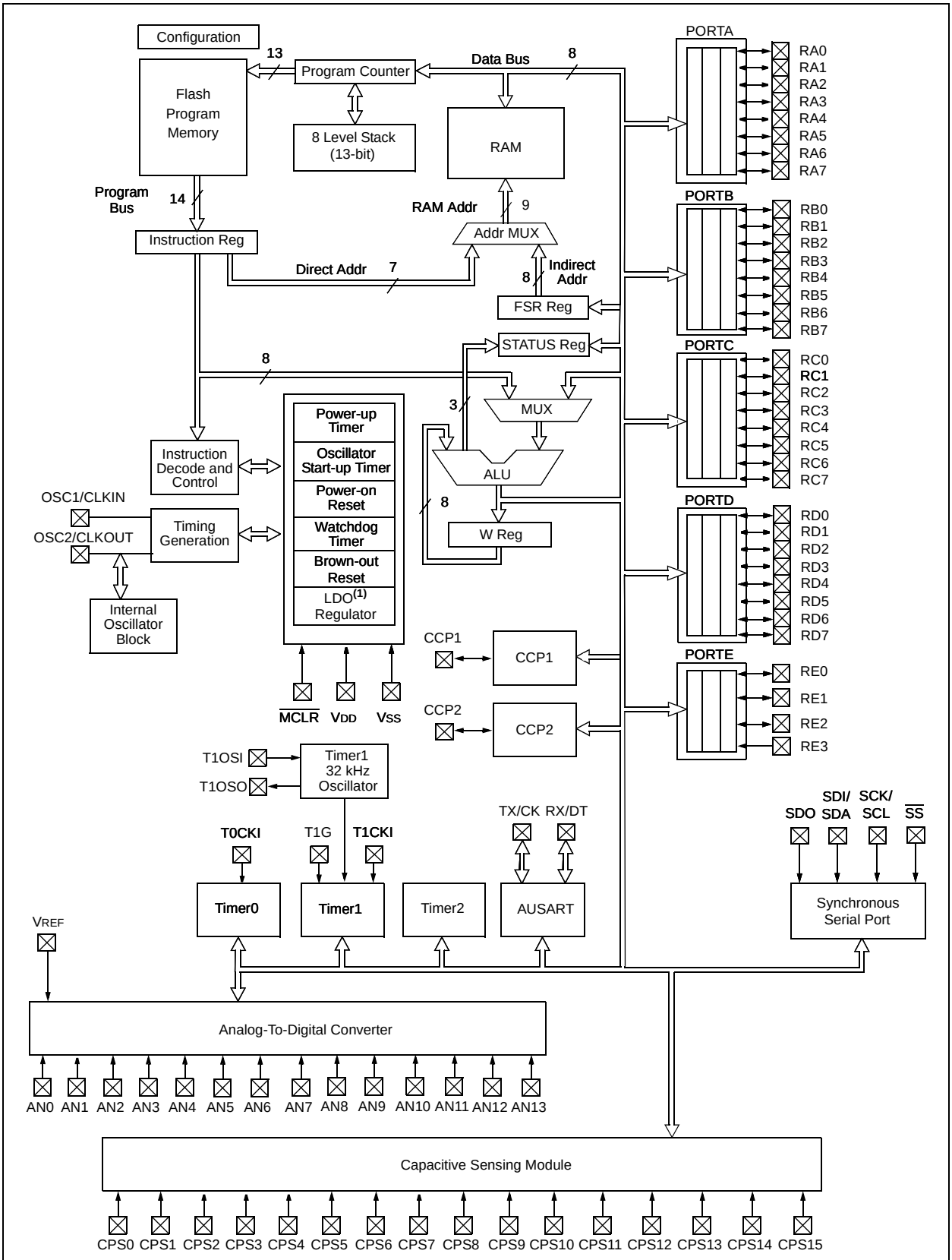
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f726-i-ss

Table of Contents

FIGURE 1-2: PIC16F724/727/PIC16LF724/727 BLOCK DIAGRAM



Note 1: PIC16F724/727 only.

2.5 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

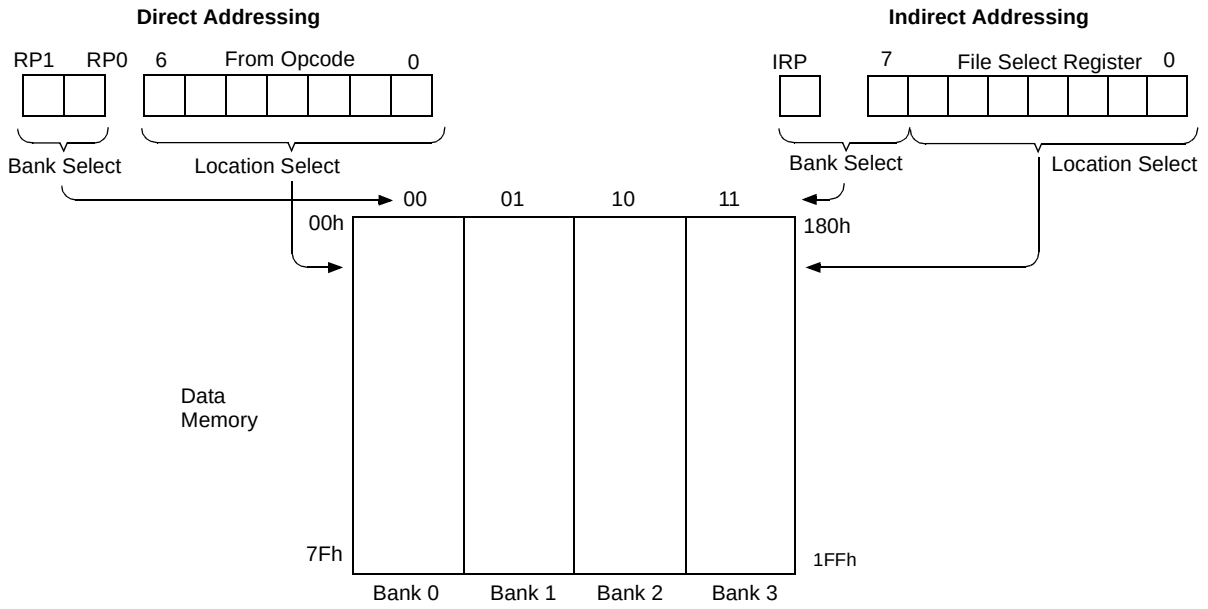
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit of the STATUS register, as shown in Figure 2-8.

A simple program to clear RAM location 020h-02Fh using indirect addressing is shown in Example 2-2.

EXAMPLE 2-2: INDIRECT ADDRESSING

```
     MOVLW     020h   ;initialize pointer
     MOVWF     FSR    ;to RAM
     BANKISEL  020h
NEXT CLRF      INDF   ;clear INDF register
     INCF      FSR    ;inc pointer
     BTFSS     FSR,4  ;all done?
     GOTO      NEXT   ;no clear next
CONTINUE              ;yes continue
```

FIGURE 2-8: DIRECT/INDIRECT ADDRESSING



Note: For memory map detail, refer to Figures 2-4 and 2-5.

3.0 RESETS

The PIC16(L)F722/3/4/6/7 differentiates between various kinds of Reset:

a) Power-on Reset (POR)
b) WDT Reset during normal operation
c) WDT Reset during Sleep
d) $\overline{\text{MCLR}}$ Reset during normal operation
e) $\overline{\text{MCLR}}$ Reset during Sleep
f) Brown-out Reset (BOR)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on:

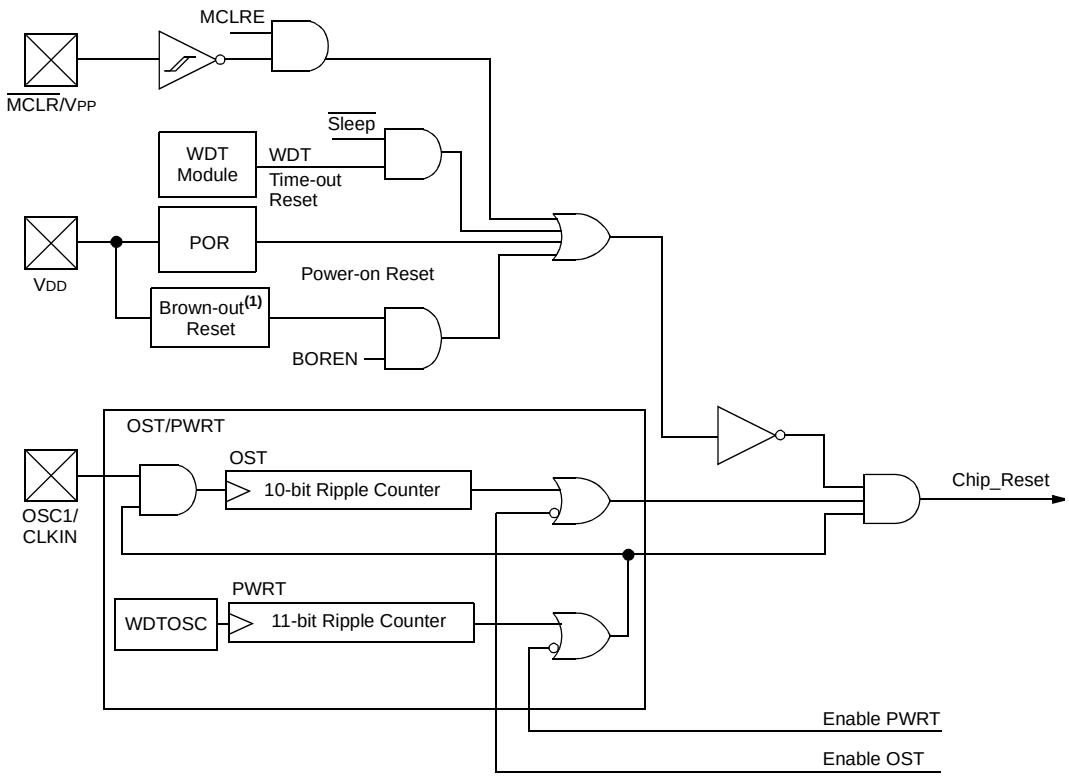
- Power-on Reset (POR)
- $\overline{\text{MCLR}}$ Reset
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Reset
- Brown-out Reset (BOR)

Most registers are not affected by a WDT wake-up since this is viewed as the resumption of normal operation. $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different Reset situations, as indicated in Table 3-3. These bits are used in software to determine the nature of the Reset.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 3-1.

The $\overline{\text{MCLR}}$ Reset path has a noise filter to detect and ignore small pulses. See **Section 23.0 "Electrical Specifications"** for pulse-width specifications.

FIGURE 3-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: Refer to the Configuration Word Register 1 (Register 8-1).

4.5.2 PIE1 REGISTER

The PIE1 register contains the interrupt enable bits, as shown in Register 4-2.

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 4-2: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TMR1GIE:** Timer1 Gate Interrupt Enable bit
1 = Enable the Timer1 Gate Acquisition complete interrupt
0 = Disable the Timer1 Gate Acquisition complete interrupt

bit 6 **ADIE:** A/D Converter (ADC) Interrupt Enable bit
1 = Enables the ADC interrupt
0 = Disables the ADC interrupt

bit 5 **RCIE:** USART Receive Interrupt Enable bit
1 = Enables the USART receive interrupt
0 = Disables the USART receive interrupt

bit 4 **TXIE:** USART Transmit Interrupt Enable bit
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt

bit 3 **SSPIE:** Synchronous Serial Port (SSP) Interrupt Enable bit
1 = Enables the SSP interrupt
0 = Disables the SSP interrupt

bit 2 **CCP1IE:** CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 1 **TMR2IE:** TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the Timer2 to PR2 match interrupt
0 = Disables the Timer2 to PR2 match interrupt

bit 0 **TMR1IE:** Timer1 Overflow Interrupt Enable bit
1 = Enables the Timer1 overflow interrupt
0 = Disables the Timer1 overflow interrupt

FIGURE 6-8: BLOCK DIAGRAM OF RB4, RB<2:1>

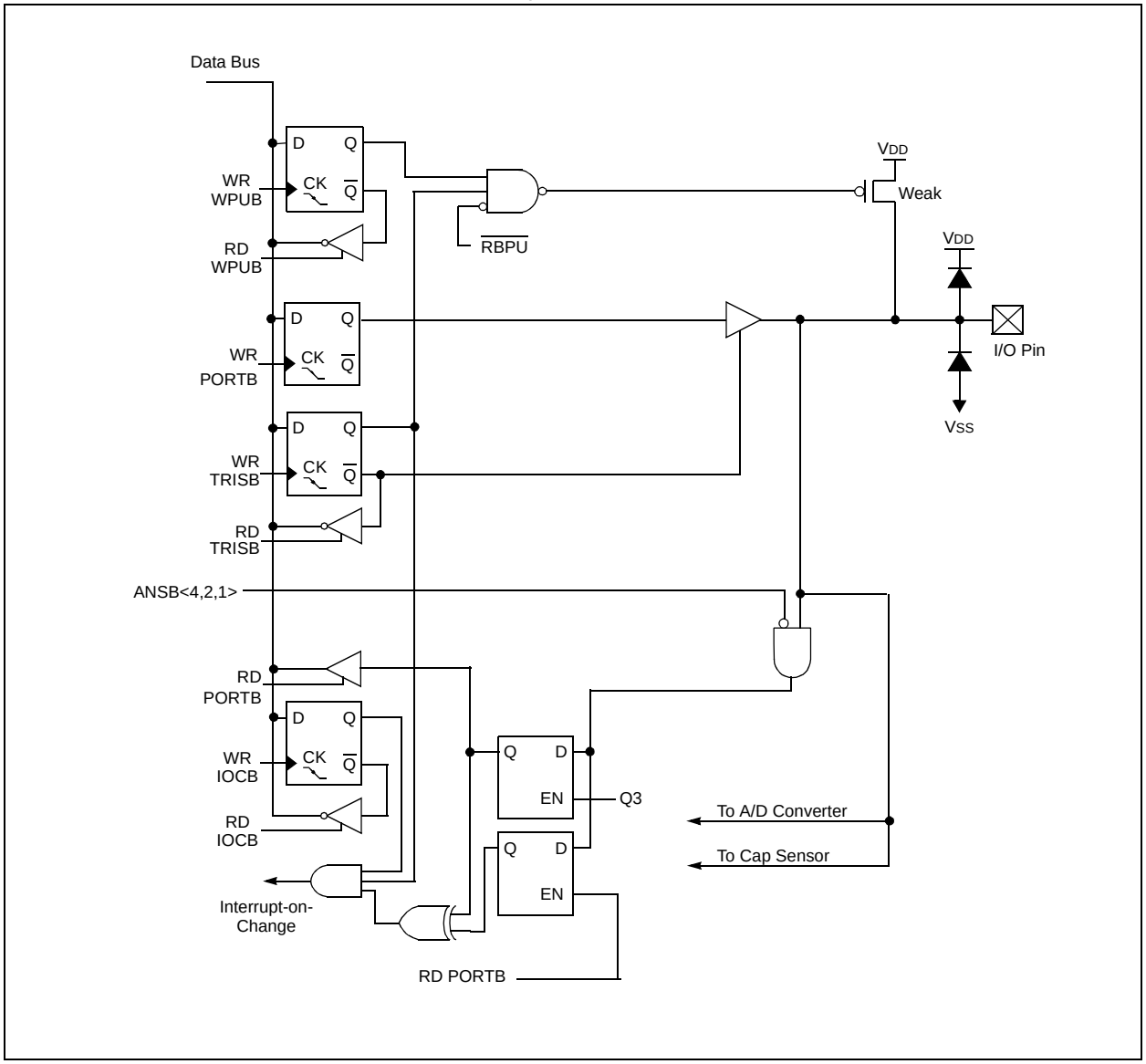


FIGURE 6-19: BLOCK DIAGRAM OF RC6

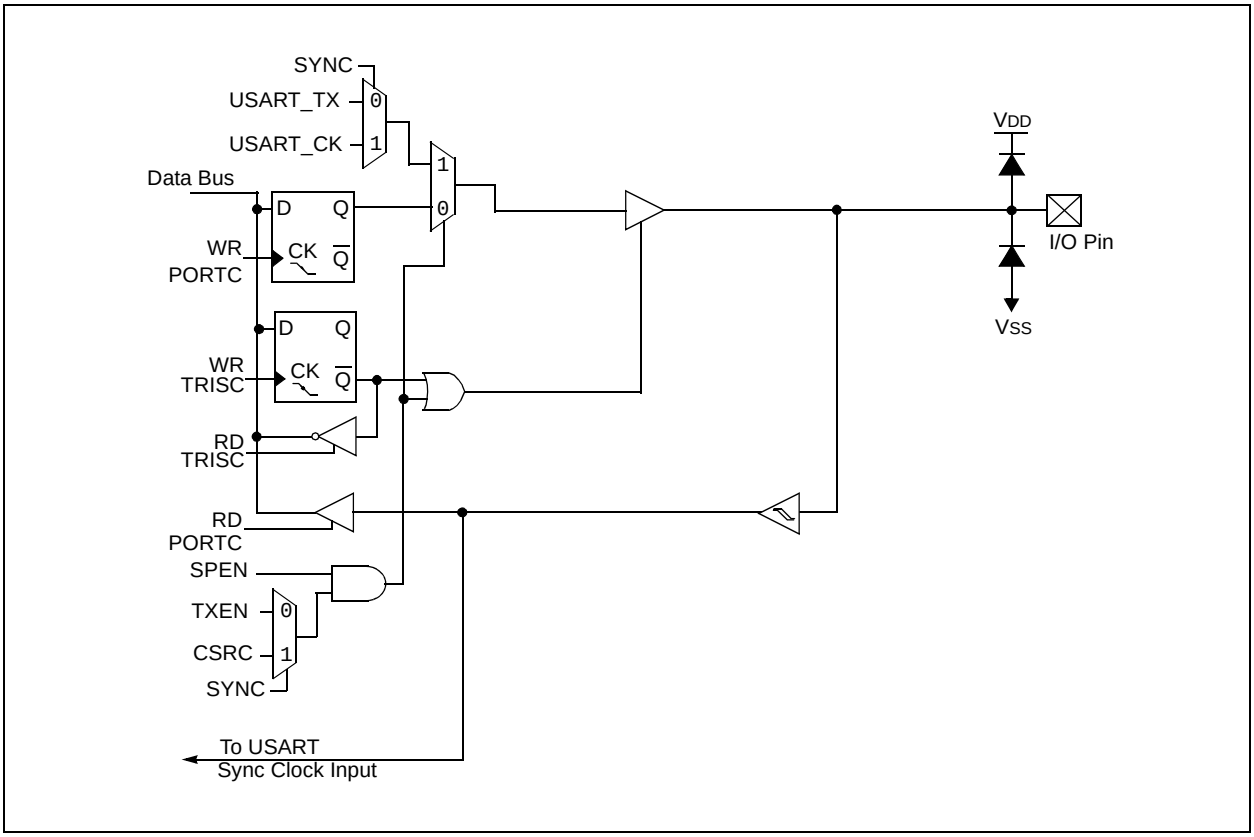
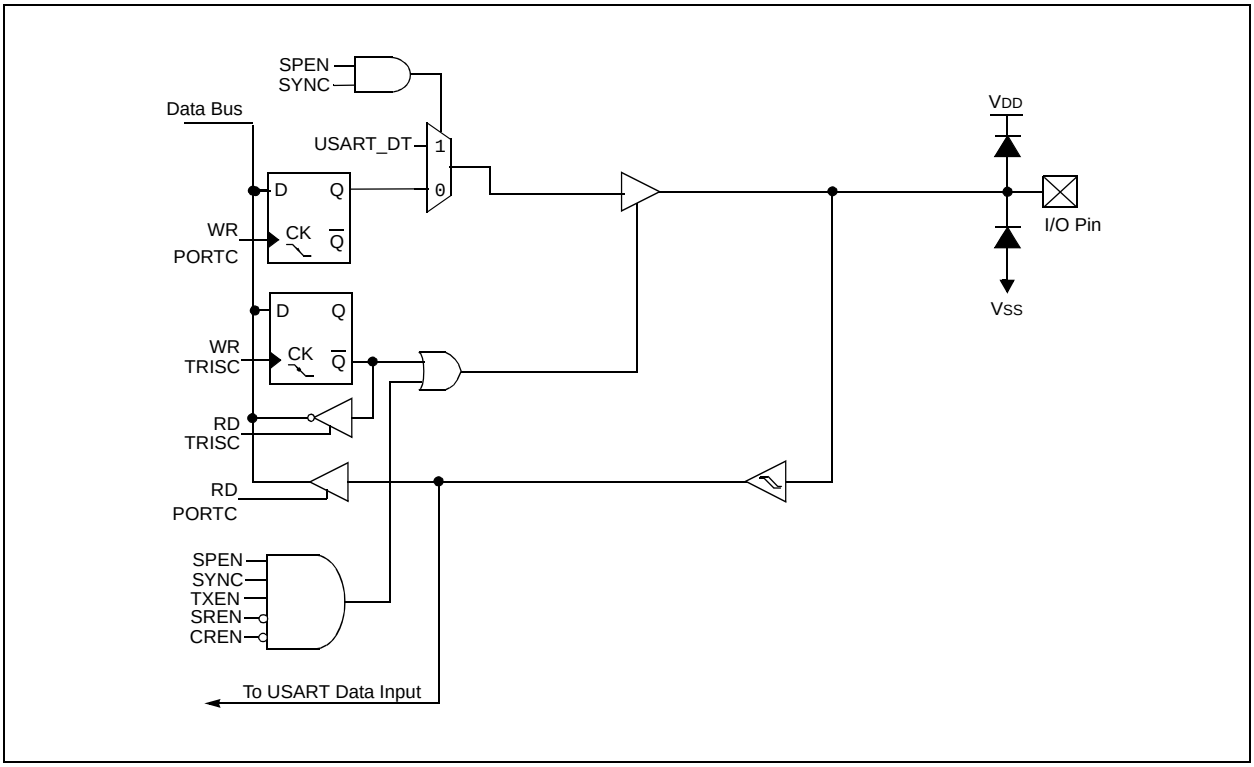


FIGURE 6-20: BLOCK DIAGRAM OF RC7



8.0 DEVICE CONFIGURATION

Device Configuration consists of Configuration Word 1 and Configuration Word 2 registers, Code Protection and Device ID.

8.1 Configuration Words

There are several Configuration Word bits that allow different oscillator and memory protection options. These are implemented as Configuration Word 1 register at 2007h and Configuration Word 2 register at 2008h. These registers are only accessible during programming.

REGISTER 8-1: CONFIG1: CONFIGURATION WORD REGISTER 1

		R/P-1	R/P-1	U-1(4)	R/P-1	R/P-1	R/P-1
—	—	$\overline{\text{DEBUG}}$	PLLEN	—	BORV	BOREN1	BOREN0
bit 15							bit 8

U-1(4)	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
—	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0
bit 7							bit 0

Legend:	P = Programmable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 13 **$\overline{\text{DEBUG}}$:** In-Circuit Debugger Mode bit
1 = In-Circuit Debugger disabled, RB6/ICSPCLK and RB7/ICSPDAT are general purpose I/O pins
0 = In-Circuit Debugger enabled, RB6/ICSPCLK and RB7/ICSPDAT are dedicated to the debugger

bit 12 **PLLEN:** INTOSC PLL Enable bit
0 = INTOSC Frequency is 500 kHz
1 = INTOSC Frequency is 16 MHz (32x)

bit 11 **Unimplemented:** Read as ‘1’

bit 10 **BORV:** Brown-out Reset Voltage selection bit
0 = Brown-out Reset Voltage (V_{BOR}) set to 2.5 V nominal
1 = Brown-out Reset Voltage (V_{BOR}) set to 1.9 V nominal

bit 9-8 **BOREN<1:0>:** Brown-out Reset Selection bits(1)
0x = BOR disabled (Preconditioned State)
10 = BOR enabled during operation and disabled in Sleep
11 = BOR enabled

bit 7 **Unimplemented:** Read as ‘1’

bit 6 **$\overline{\text{CP}}$:** Code Protection bit(2)
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 5 **MCLRE:** RE3/$\overline{\text{MCLR}}$ pin function select bit(3)
1 = RE3/$\overline{\text{MCLR}}$ pin function is $\overline{\text{MCLR}}$
0 = RE3/$\overline{\text{MCLR}}$ pin function is digital input, $\overline{\text{MCLR}}$ internally tied to V_{DD}

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
2: The entire program memory will be erased when the code protection is turned off.
3: When $\overline{\text{MCLR}}$ is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.
4: MPLAB® X IDE masks unimplemented Configuration bits to ‘0’.

REGISTER 8-1: CONFIG1: CONFIGURATION WORD REGISTER 1 (CONTINUED)

bit 4 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
111 = RC oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, RC on RA7/OSC1/CLKIN
110 = RCIO oscillator: I/O function on RA6/OSC2/CLKOUT pin, RC on RA7/OSC1/CLKIN
101 = INTOSC oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN
100 = INTOSCIO oscillator: I/O function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN
011 = EC: I/O function on RA6/OSC2/CLKOUT pin, CLKIN on RA7/OSC1/CLKIN
010 = HS oscillator: High-speed crystal/resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN
001 = XT oscillator: Crystal/resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN
000 = LP oscillator: Low-power crystal on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
2: The entire program memory will be erased when the code protection is turned off.
3: When $\overline{\text{MCLR}}$ is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.
4: MPLAB® X IDE masks unimplemented Configuration bits to '0'.

REGISTER 8-2: CONFIG2: CONFIGURATION WORD REGISTER 2

		U-1(1)	U-1(1)	U-1(1)	U-1(1)	U-1(1)	U-1(1)
—	—	—	—	—	—	—	—
bit 15							bit 8

U-1(1)	U-1(1)	R/P-1	R/P-1	U-1(1)	U-1(1)	U-1(1)	U-1(1)
—	—	VCAPEN1	VCAPEN0	—	—	—	—
bit 7							bit 0

Legend:	P = Programmable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 13-6 **Unimplemented**: Read as '1'

bit 5-4 **VCAPEN<1:0>:** Voltage Regulator Capacitor Enable bits
For the PIC16LF72X:
These bits are ignored. All VCAP pin functions are disabled.
For the PIC16F72X:
00 = VCAP functionality is enabled on RA0
01 = VCAP functionality is enabled on RA5
10 = VCAP functionality is enabled on RA6
11 = All VCAP functions are disabled (not recommended)

bit 3-0 **Unimplemented**: Read as '1'

Note 1: MPLAB® X IDE masks unimplemented Configuration bits to '0'.

12.11 Timer1 Control Register

The Timer1 Control register (T1CON), shown in Register 12-1, is used to control Timer1 and select the various features of the Timer1 module.

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	—	TMR1ON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **TMR1CS<1:0>:** Timer1 Clock Source Select bits
11 = Timer1 clock source is Capacitive Sensing Oscillator (CAPOSC)
10 = Timer1 clock source is pin or oscillator:
If T1OSCEN = 0:
External clock from T1CKI pin (on the rising edge)
If T1OSCEN = 1:
Crystal oscillator on T1OSI/T1OSO pins
01 = Timer1 clock source is system clock (FOSC)
00 = Timer1 clock source is instruction clock (FOSC/4)

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3 **T1OSCEN:** LP Oscillator Enable Control bit
1 = Dedicated Timer1 oscillator circuit enabled
0 = Dedicated Timer1 oscillator circuit disabled

bit 2 **$\overline{\text{T1SYNC}}$:** Timer1 External Clock Input Synchronization Control bit
TMR1CS<1:0> = 1X
1 = Do not synchronize external clock input
0 = Synchronize external clock input with system clock (FOSC)

TMR1CS<1:0> = 0X
This bit is ignored. Timer1 uses the internal clock when TMR1CS<1:0> = 1X.

bit 1 **Unimplemented:** Read as '0'

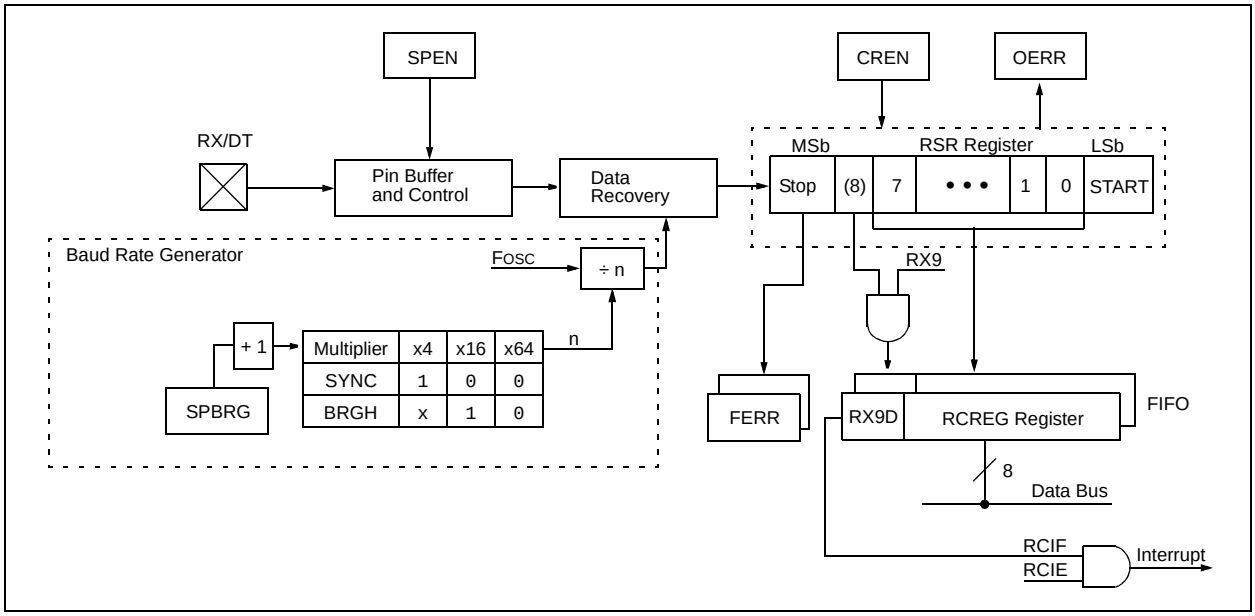
bit 0 **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1
Clears Timer1 Gate flip-flop

TABLE 15-3: SUMMARY OF REGISTERS ASSOCIATED WITH CAPTURE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	--11 1111	--11 1111
APFCON	—	—	—	—	—	—	SSSEL	CCP2SEL	---- --00	---- --00
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000
CCPRxL	Capture/Compare/PWM Register X Low Byte								xxxx xxxx	uuuu uuuu
CCPRxH	Capture/Compare/PWM Register X High Byte								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIE2	—	—	—	—	—	—	—	CCP2IE	---- ---0	---- ---0
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIR2	—	—	—	—	—	—	—	CCP2IF	---- ---0	---- ---0
T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	—	TMR1ON	0000 00-0	uuuu uu-u
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{DONE}}$	T1GVAL	T1GSS1	T1GSS0	0000 0x00	0000 0x00
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

Legend: - = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Capture.

FIGURE 16-2: AUSART RECEIVE BLOCK DIAGRAM



The operation of the AUSART module is controlled through two registers:

- Transmit Status and Control (TXSTA)
- Receive Status and Control (RCSTA)

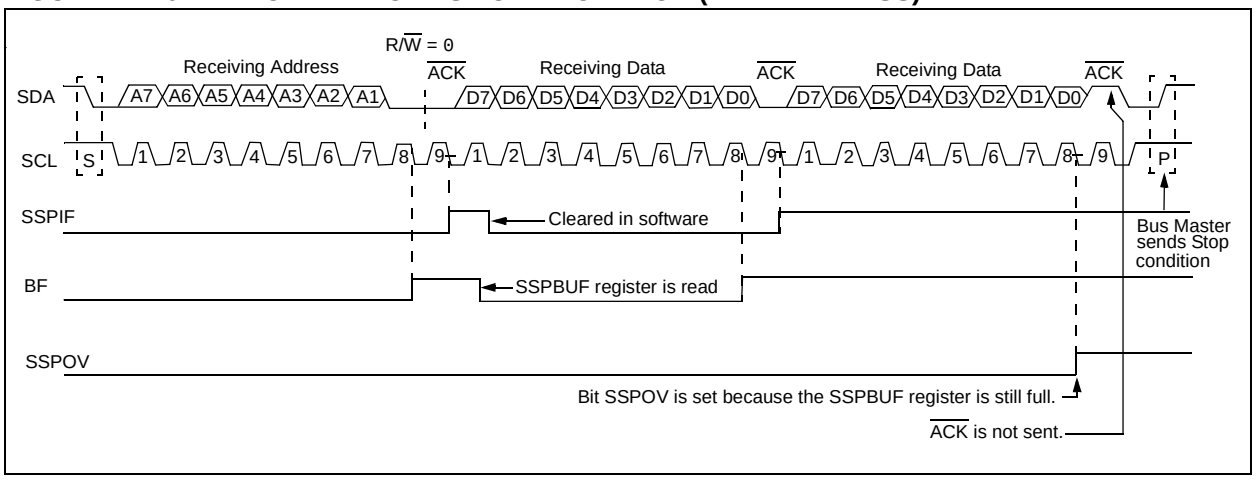
These registers are detailed in Register 16-1 and Register 16-2, respectively.

17.2.5 RECEPTION

When the R/$\overline{W}$ bit of the received address byte is clear, the master will write data to the slave. If an address match occurs, the received address is loaded into the SSPBUF register. An address byte overflow will occur if that loaded address is not read from the SSPBUF before the next complete byte is received.

An SSP interrupt is generated for each data transfer byte. The BF, R/$\overline{W}$ and D/$\overline{A}$ bits of the SSPSTAT register are used to determine the status of the last received byte.

FIGURE 17-10: I²C WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)



REGISTER 18-4: PMADRH: PROGRAM MEMORY ADDRESS HIGH REGISTER

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	PMA12	PMA11	PMA10	PMA9	PMA8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **PMA<12:8>:** Program Memory Read Address bits

REGISTER 18-5: PMADRL: PROGRAM MEMORY ADDRESS LOW REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
PMA7	PMA6	PMA5	PMA4	PMA3	PMA2	PMA1	PMA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **PMA<7:0>:** Program Memory Read Address bits

TABLE 18-1: SUMMARY OF REGISTERS ASSOCIATED WITH PROGRAM MEMORY READ

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
PMCON1	Reserved	—	—	—	—	—	—	RD	1--- ---0	1--- ---0
PMADRH	—	—	—	Program Memory Read Address Register High Byte					---x xxxx	---x xxxx
PMADRL	Program Memory Read Address Register Low Byte								xxxx xxxx	xxxx xxxx
PMDATH	—	—	Program Memory Read Data Register High Byte						--xx xxxx	--xx xxxx
PMDATL	Program Memory Read Data Register Low Byte								xxxx xxxx	xxxx xxxx

Legend: x = unknown, u = unchanged, – = unimplemented, read as ‘0’. Shaded cells are not used by the Program Memory Read.

23.3 DC Characteristics: PIC16(L)F722/3/4/6/7-I/E (Power-Down)

PIC16LF722/3/4/6/7			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
PIC16F722/3/4/6/7			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device Characteristics**	**Min.**	**Typ†**	**Max. +85°C**	**Max. +125°C**	**Units**	**Conditions**	
							VDD	**Note**
	Power-down Base Current (IPD)(2)							
D020		—	0.02	0.7	3.9	µA	1.8	WDT, BOR, FVR, and T1OSC disabled, all Peripherals Inactive
		—	0.08	1.0	4.3	µA	3.0	
D020		—	4.3	10.2	17	µA	1.8	WDT, BOR, FVR, and T1OSC disabled, all Peripherals Inactive
		—	5	10.5	18	µA	3.0	
		—	5.5	11.8	21	µA	5.0	
D021		—	0.5	1.7	4.1	µA	1.8	LPWDT Current **(Note 1)**
		—	0.8	2.5	4.8	µA	3.0	
D021		—	6	13.5	18	µA	1.8	LPWDT Current **(Note 1)**
		—	6.5	14.5	19	µA	3.0	
		—	7.5	16	22	µA	5.0	
D021A		—	8.5	14	19	µA	1.8	FVR current **(Note 1. Note 3)**
		—	8.5	14	20	µA	3.0	
D021A		—	23	44	48	µA	1.8	FVR current **(Note 1, Note 3, Note 5)**
		—	25	45	55	µA	3.0	
		—	26	60	70	µA	5.0	
D022		—	—	—	—	µA	1.8	BOR Current **(Note 1, Note 3)**
		—	7.5	12	22	µA	3.0	
D022		—	—	—	—	µA	1.8	BOR Current **(Note 1, Note 3, Note 5)**
		—	23	42	49	µA	3.0	
		—	25	46	50	µA	5.0	
D026		—	0.6	2	—	µA	1.8	T1OSC Current **(Note 1)**
		—	1.8	3.0	—	µA	3.0	
D026		—	4.5	11.1	—	µA	1.8	T1OSC Current **(Note 1)**
		—	6	12.5	—	µA	3.0	
		—	7	13.5	—	µA	5.0	

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

3: Fixed Voltage Reference is automatically enabled whenever the BOR is enabled

4: A/D oscillator source is FRC

5: 0.1 µF capacitor on VCAP (RA0).

FIGURE 24-7: PIC16F722/3/4/6/7 TYPICAL IDD vs. VDD OVER FOSC, EXTRC MODE, VCAP = 0.1 µF

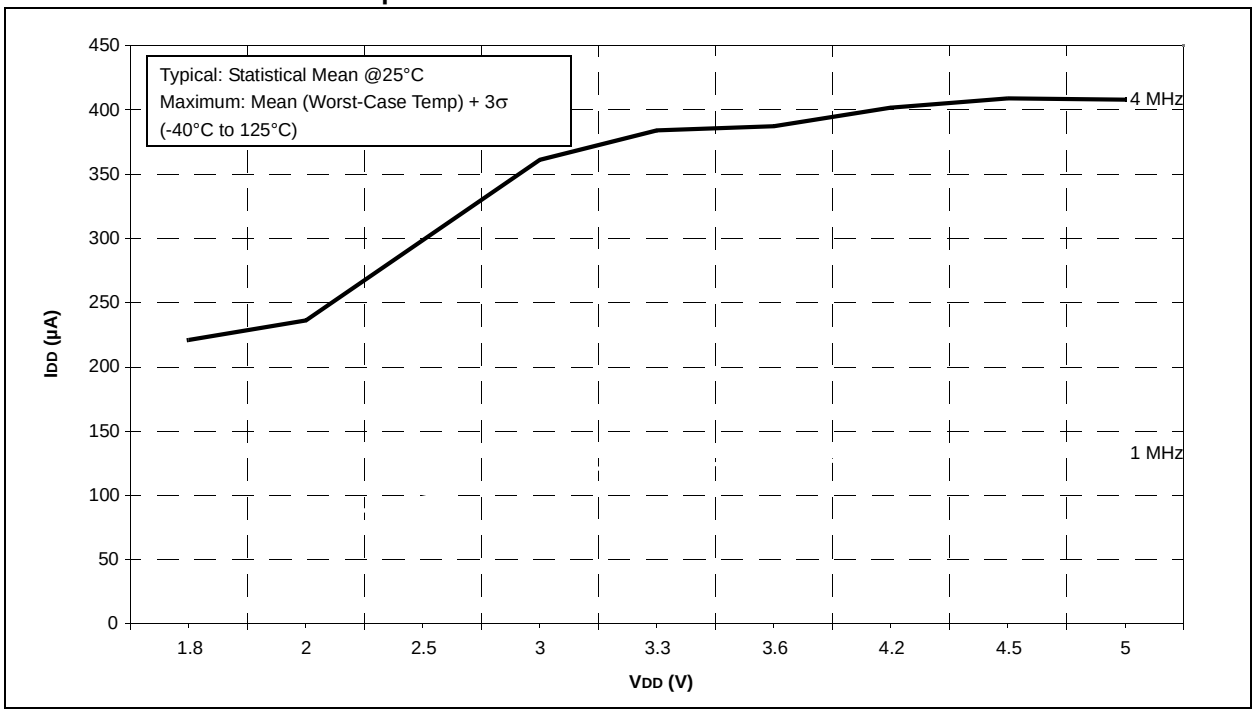


FIGURE 24-8: PIC16LF722/3/4/6/7 TYPICAL IDD vs. VDD OVER FOSC, EXTRC MODE

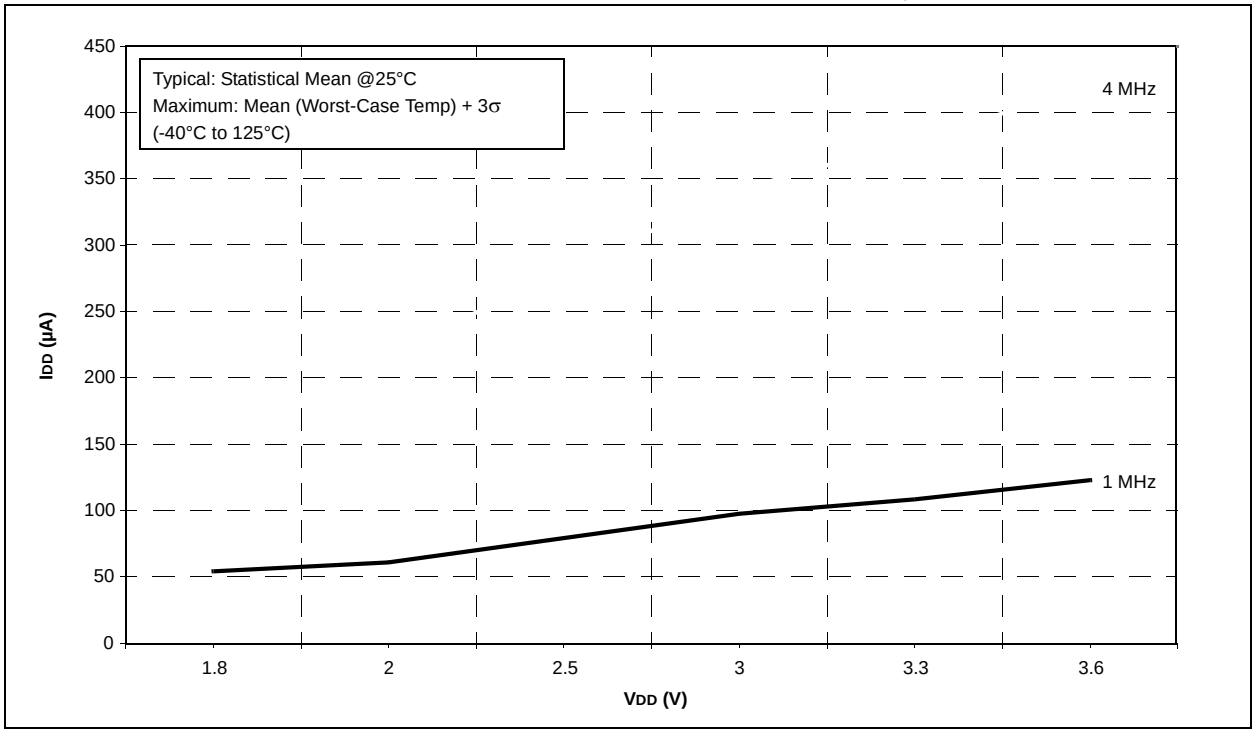


FIGURE 24-31: PIC16F722/3/4/6/7 FIXED VOLTAGE REFERENCE IPD VS. VDD, VCAP = 0.1 µF

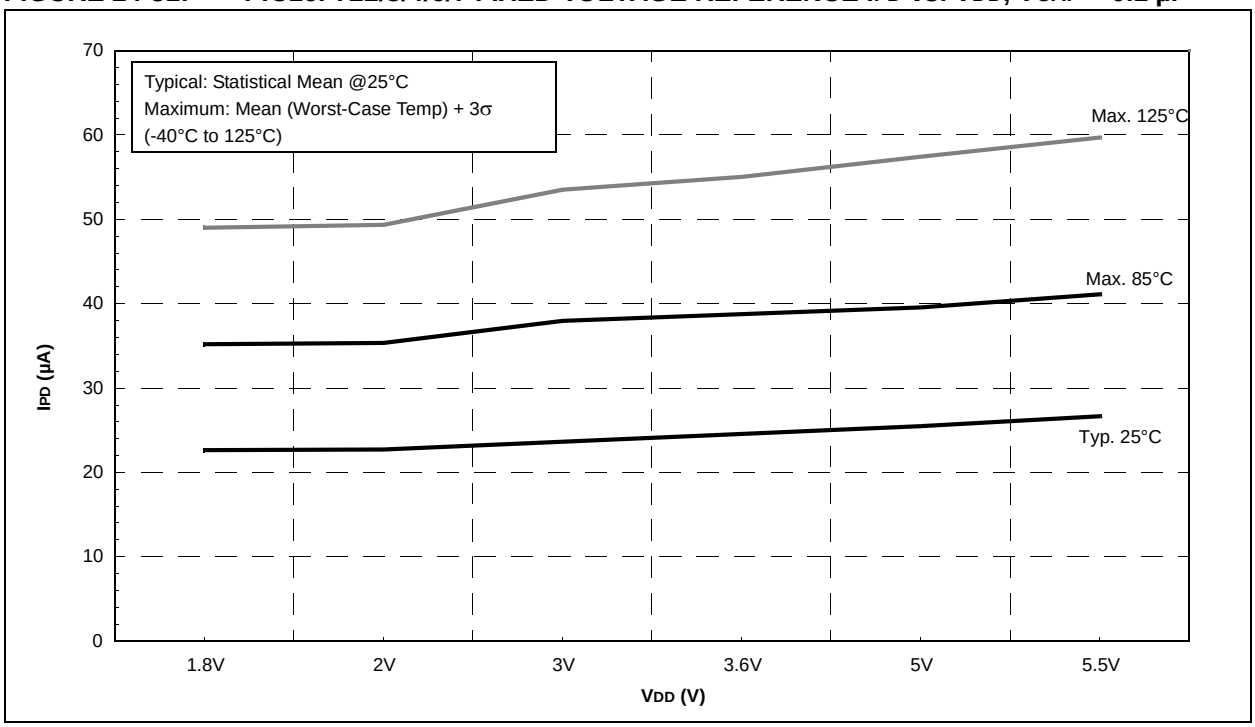


FIGURE 24-32: PIC16LF722/3/4/6/7 FIXED VOLTAGE REFERENCE IPD VS. VDD

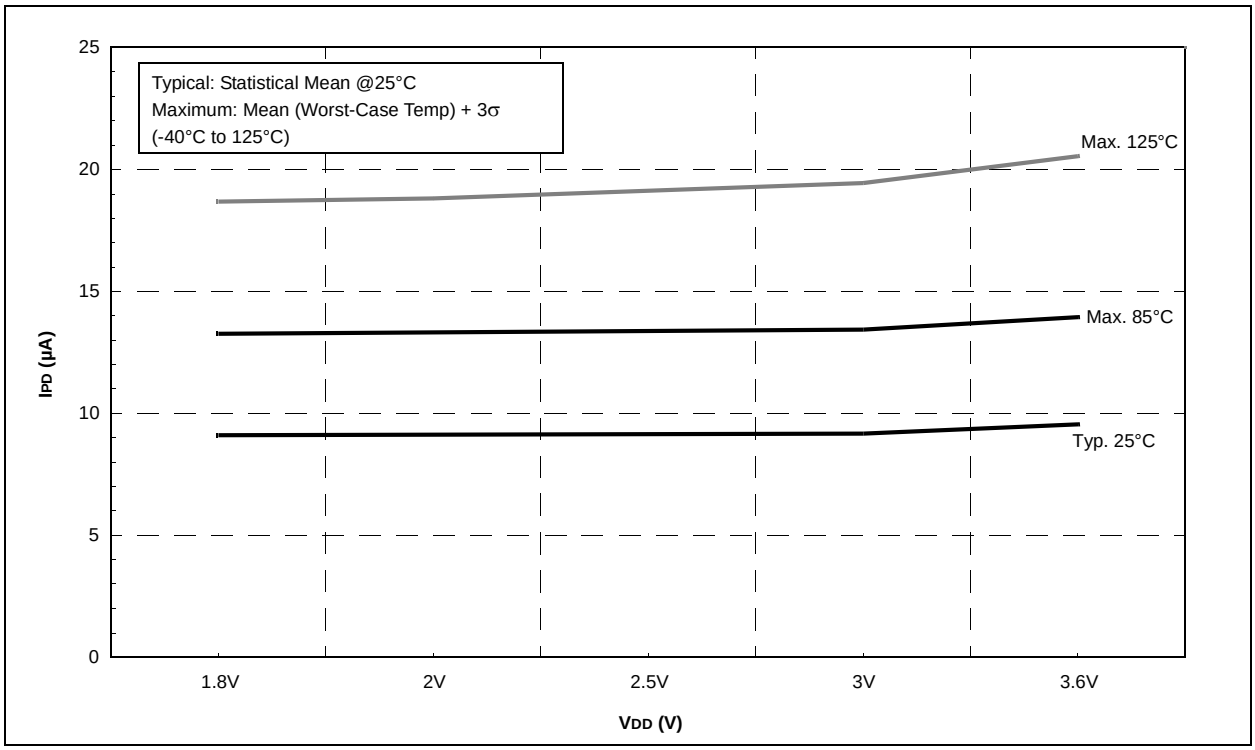


FIGURE 24-43: PIC16F722/3/4/6/7 TYPICAL ADC IPD vs. VDD, VCAP = 0.1 µF

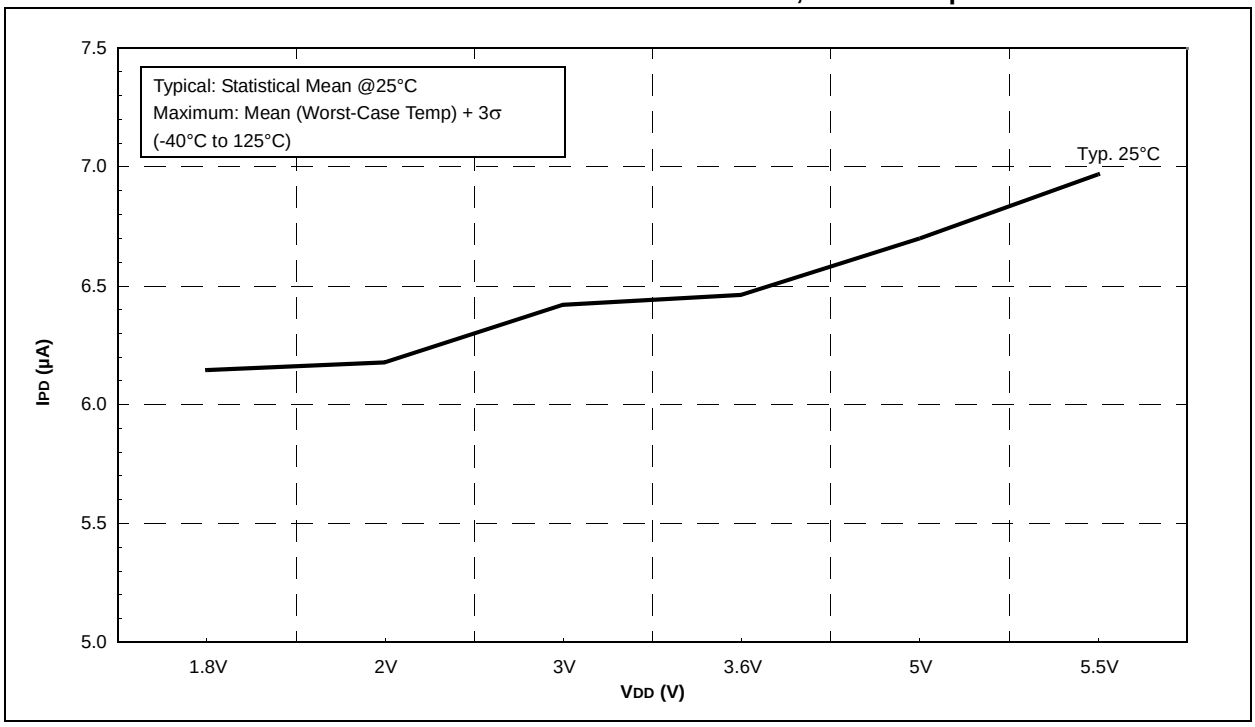


FIGURE 24-44: PIC16LF722/3/4/6/7 TYPICAL ADC IPD vs. VDD

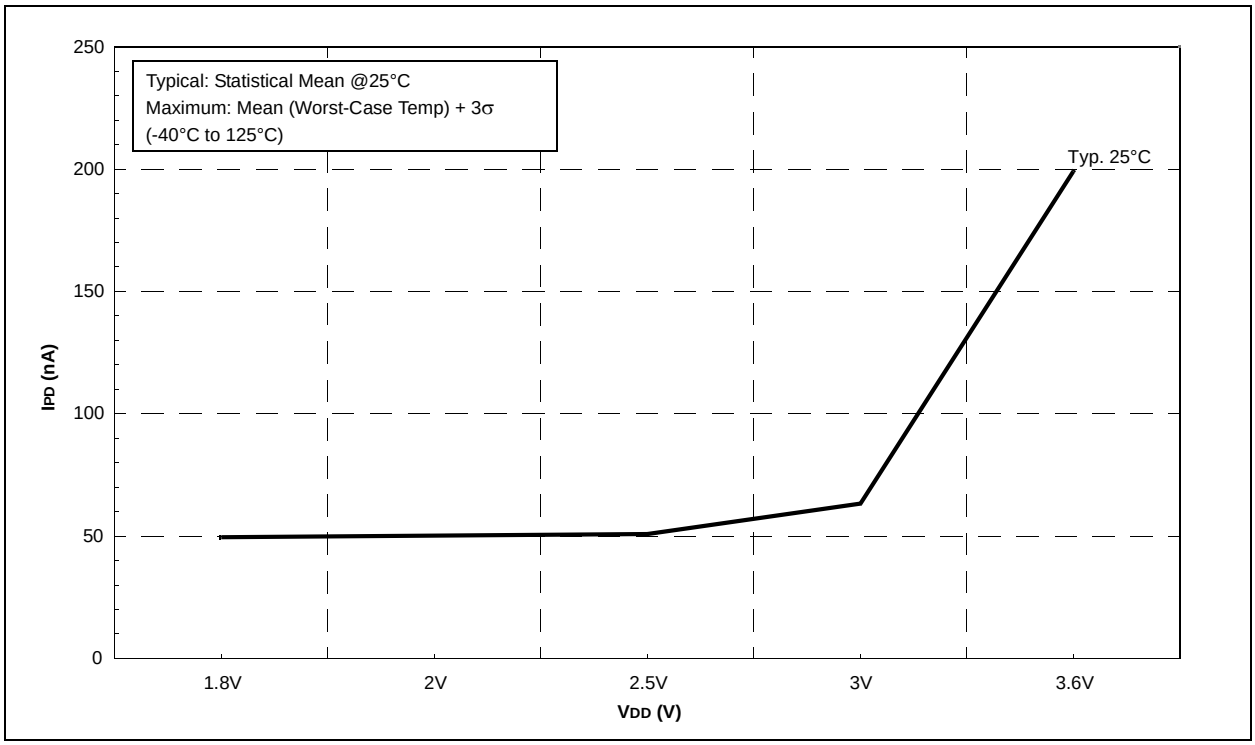


FIGURE 24-51: SCHMITT TRIGGER INPUT THRESHOLD VIN vs. VDD OVER TEMPERATURE

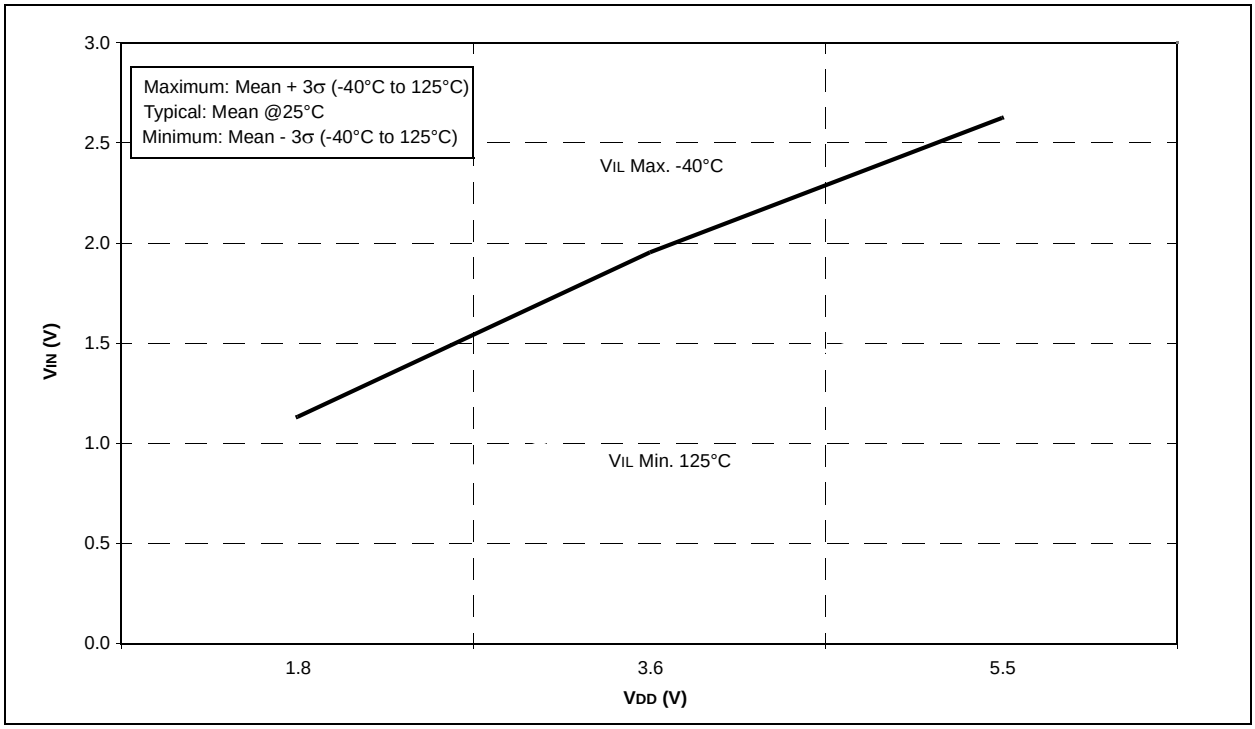
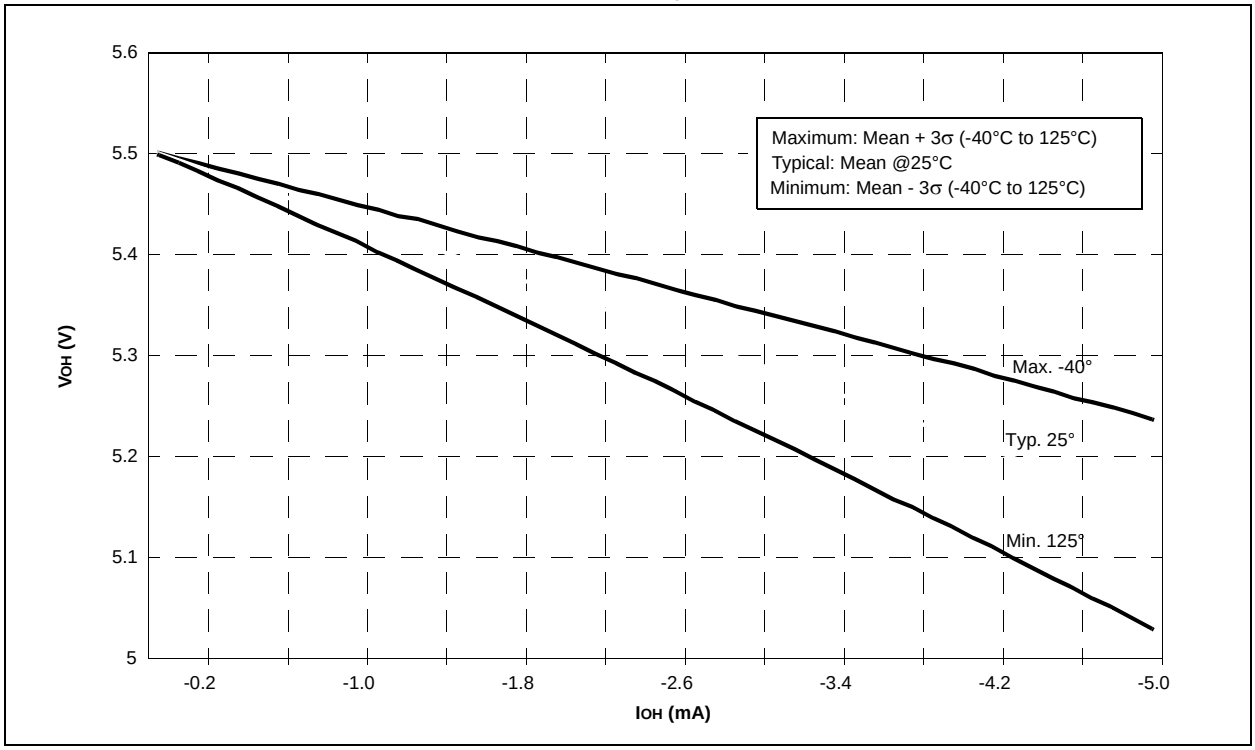


FIGURE 24-52: VOH vs. IOH OVER TEMPERATURE, VDD = 5.5V



APPENDIX A: DATA SHEET REVISION HISTORY

Revision A (12/2007)

Original release.

Revision B (08/2008)

Electrical Specification updates; Package Drawings; miscellaneous updates.

Revision C (04/2009)

Revised data sheet title; Revised Low-Power Features section; Revised Section 6.2.2.4 RA3/AN3/VREF; Revised Figure 16-8 Synchronous Reception.

Revision D (07/2009)

Removed the Preliminary Label; Updated the “Electrical Characteristics” section; Added charts in the “Char. Data” section; Deleted “Based 8-Bit CMOS” from title; Updated the “Special Microcontroller Features” section and the “Peripheral Features” section; Changed the title of the “Low Power Features” section into “Extreme Low-Power Management PIC16LF72X with nanoWatt XLP” and updated this section; Inserted new section – “Analog Features” (page 1); Changed the title of the “Peripheral Features” section into “Peripheral Highlights” and updated the section.

Revision E (10/2009)

Added paragraph to section 5.0 (LDO Voltage Regulator); Updated the Electrical Specifications section (Added another absolute Maximum Rating; Updated section 23.1 and Table 23-4); Updated the Pin Diagrams with the UQFN package; Updated Table 1, adding UQFN; Updated section 23.5 (Thermal Considerations); Updated the Packaging Information section adding the UQFN Package; Updated the Product Identification System section.

Revision F (12/2015)

Updated Table 2; Updated 23.1, 23.3 and 9.2.4 Sections; Updated Figure 23-9; Other minor corrections.

APPENDIX B: MIGRATING FROM OTHER PIC® DEVICES

This discusses some of the issues in migrating from other PIC® devices to the PIC16F72X family of devices.

B.1 PIC16F77 to PIC16F72X

TABLE B-1: FEATURE COMPARISON

Feature	PIC16F77	PIC16F727
Max. Operating Speed	20 MHz	20 MHz
Max. Program Memory (Words)	8K	8K
Max. SRAM (Bytes)	368	368
A/D Resolution	8-bit	8-bit
Timers (8/16-bit)	2/1	2/1
Oscillator Modes	4	8
Brown-out Reset	Y	Y
Internal Pull-ups	RB<7:0>	RB<7:0>
Interrupt-on-change	RB<7:4>	RB<7:0>
Comparator	0	0
USART	Y	Y
Extended WDT	N	N
Software Control Option of WDT/BOR	N	N
INTOSC Frequencies	None	500 kHz - 16 MHz
Clock Switching	N	N