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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f726t-i-ml

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TABLE 1-1: PIC16(L)F722/3/4/6/7 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/SS/Vcap	RA0	TTL	CMOS	General purpose I/O.
	AN0	AN	_	A/D Channel 0 input.
	SS	ST	_	Slave Select input.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F72X only).
RA1/AN1	RA1	TTL	CMOS	General purpose I/O.
	AN1	AN	_	A/D Channel 1 input.
RA2/AN2	RA2	TTL	CMOS	General purpose I/O.
	AN2	AN	_	A/D Channel 2 input.
RA3/AN3/VREF	RA3	TTL	CMOS	General purpose I/O.
	AN3	AN		A/D Channel 3 input.
	Vref	AN	_	A/D Voltage Reference input.
RA4/CPS6/T0CKI	RA4	TTL	CMOS	General purpose I/O.
	CPS6	AN	—	Capacitive sensing input 6.
	T0CKI	ST	_	Timer0 clock input.
RA5/AN4/CPS7/SS/Vcap	RA5	TTL	CMOS	General purpose I/O.
	AN4	AN	—	A/D Channel 4 input.
	CPS7	AN	—	Capacitive sensing input 7.
	SS	ST	_	Slave Select input.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F72X only).
RA6/OSC2/CLKOUT/VCAP	RA6	TTL	CMOS	General purpose I/O.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	Fosc/4 output.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F72X only).
RA7/OSC1/CLKIN	RA7	TTL	CMOS	General purpose I/O.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	CMOS	—	External clock input (EC mode).
	CLKIN	ST	—	RC oscillator connection (RC mode).
RB0/AN12/CPS0/INT	RB0	TTL	CMOS	General purpose I/O. Individually controlled inter- rupt-on-change. Individually enabled pull-up.
	AN12	AN	_	A/D Channel 12 input.
	CPS0	AN	—	Capacitive sensing input 0.
	INT	ST	—	External interrupt.
RB1/AN10/CPS1	RB1	TTL	CMOS	General purpose I/O. Individually controlled inter- rupt-on-change. Individually enabled pull-up.
	AN10	AN		A/D Channel 10 input.
	CPS1	AN	—	Capacitive sensing input 1.
RB2/AN8/CPS2	RB2	TTL	CMOS	General purpose I/O. Individually controlled inter- rupt-on-change. Individually enabled pull-up.
	AN8	AN	_	A/D Channel 8 input.
	CPS2	AN		Capacitive sensing input 2.
RB3/AN9/CPS3/CCP2	RB3	TTL	CMOS	General purpose I/O. Individually controlled inter- rupt-on-change. Individually enabled pull-up.
	AN9	AN	_	A/D Channel 9 input.
	CPS3	AN	_	Capacitive sensing input 3.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
Legend: AN = Analog input or o TTL = TTL compatible in HV = High Voltage	utput CMO nput ST XTAL	S = CMO = Schm = Cryst	S compat iitt Trigger al levels	ible input or output OD = Open Drain r input with CMOS levels I^2C = Schmitt Trigger input with I^2C

2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC16(L)F722/3/4/6/7 has a 13-bit program counter capable of addressing a 2K x 14 program memory space for the PIC16F722/LF722 (0000h-07FFh), a 4K x 14 program memory space for PIC16F723/LF723 and PIC16F724/LF724 the (0000h-0FFFh) and an 8K x 14 program memory space for the PIC16F726/LF726 and PIC16F727/LF727 (0000h-1FFFh). Accessing a location above the memory boundaries for the PIC16F722/LF722 will cause a wrap-around within the first 2K x 14 program memory space. Accessing a location above the memory boundaries for the PIC16F723/LF723 and PIC16F724/LF724 will cause a wrap-around within the first 4K x 14 program memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F722/LF722



FIGURE 2-2:

PROGRAM MEMORY MAP AND STACK FOR THE PIC16F723/LF723 AND PIC16F724/LF724



3.6 Time-out Sequence

On power-up, the time-out sequence is as follows: first, PWRT time out is invoked after POR has expired, then OST is activated after the PWRT time out has expired. The total time out will vary based on oscillator configuration and \overrightarrow{PWRTE} bit status. For example, in EC mode with \overrightarrow{PWRTE} bit = 1 (\overrightarrow{PWRT} disabled), there will be no time out at all. Figure 3-4, Figure 3-5 and Figure 3-6 depict time-out sequences.

Since the time outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time outs will expire. Then, bringing $\overline{\text{MCLR}}$ high will begin execution immediately (see Figure 3-5). This is useful for testing purposes or to synchronize more than one PIC16(L)F722/3/4/6/7 device operating in parallel.

Table 3-3 shows the Reset conditions for some special registers.

3.7 Power Control (PCON) Register

The Power Control (PCON) register has two Status bits to indicate what type of Reset that last occurred.

Bit 0 is $\overline{\text{BOR}}$ (Brown-out Reset). $\overline{\text{BOR}}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if $\overline{\text{BOR}} = 0$, indicating that a brown-out has occurred. The $\overline{\text{BOR}}$ Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (BOREN<1:0> = 00 in the Configuration Word register).

Bit 1 is POR (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent Reset, if POR is '0', it will indicate that a Power-on Reset has occurred (i.e., VDD may have gone too low).

For more information, see Section 3.5 "Brown-Out Reset (BOR)".

Occillator Configuration	Powe	er-up	Brown-o	Wake-up from	
Oscillator Configuration	PWRTE = 0	PWRTE = 1	PWRTE = 0	PWRTE = 1	Sleep
XT, HS, LP ⁽¹⁾	TPWRT + 1024 • Tosc	1024 • Tosc	TPWRT + 1024 • Tosc	1024 • Tosc	1024 • Tosc
RC, EC, INTOSC	TPWRT	_	TPWRT		

TABLE 3-2: TIME OUT IN VARIOUS SITUATIONS

Note 1: LP mode with T1OSC disabled.

TABLE 3-3: RESET BITS AND THEIR SIGNIFICANCE

POR	BOR	то	PD	Condition
0	u	1	1	Power-on Reset
1	0	1	1	Brown-out Reset
u	u	0	u	WDT Reset
u	u	0	0	WDT Wake-up
u	u	u	u	MCLR Reset during normal operation
u	u	1	0	MCLR Reset during Sleep

Legend: u = unchanged, x = unknown

4.5.3 PIE2 REGISTER

Γ.

bit 0

The PIE2 register contains the interrupt enable bits, as shown in Register 4-3.

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 4-3: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	CCP2IE
bit 7							bit 0

Legena:			
R = Readable bit W	= Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR '1'	= Bit is set	0' = Bit is cleared	x = Bit is unknown

bit 7-1 Unimplemented: Read as '0'

CCP2IE: CCP2 Interrupt Enable bit

1 = Enables the CCP2 interrupt

0 = Disables the CCP2 interrupt

4.5.4 PIR1 REGISTER

The PIR1 register contains the interrupt flag bits, as shown in Register 4-4.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 4-4: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

	1 - Timer1 Gate is inactive
	0 = Timer1 Gate is active
bit 6	ADIF: A/D Converter Interrupt Flag bit
	 1 = A/D conversion complete (must be cleared in software) 0 = A/D conversion has not completed or has not been started
bit 5	RCIF: USART Receive Interrupt Flag bit
	1 = The USART receive buffer is full (cleared by reading RCREG)0 = The USART receive buffer is not full
bit 4	TXIF: USART Transmit Interrupt Flag bit
	 1 = The USART transmit buffer is empty (cleared by writing to TXREG) 0 = The USART transmit buffer is full
bit 3	SSPIF: Synchronous Serial Port (SSP) Interrupt Flag bit
	1 = The Transmission/Reception is complete (must be cleared in software)0 = Waiting to Transmit/Receive
bit 2	CCP1IF: CCP1 Interrupt Flag bit
	Capture mode:
	 1 = A TMR1 register capture occurred (must be cleared in software) 0 = No TMR1 register capture occurred
	Compare mode:
	 1 = A TMR1 register compare match occurred (must be cleared in software) 0 = No TMR1 register compare match occurred
	<u>PWM mode</u> : Unused in this mode
bit 1	TMR2IF: Timer2 to PR2 Interrupt Flag bit
	1 = A Timer2 to PR2 match occurred (must be cleared in software)0 = No Timer2 to PR2 match occurred
bit 0	TMR1IF: Timer1 Overflow Interrupt Flag bit
	 1 = The TMR1 register overflowed (must be cleared in software) 0 = The TMR1 register did not overflow

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0
bit 7						•	bit 0
Legend:							
R = Readable bit W = Writable bit		U = Unimplemented bit, read as '0'					
-n = Value at POR '1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown		

REGISTER 6-7: WPUB: WEAK PULL-UP PORTB REGISTER

bit 7-0 WPUB<7:0>: Weak Pull-up Register bits

- 1 = Pull-up enabled
- 0 = Pull-up disabled

Note 1: Global RBPU bit of the OPTION register must be cleared for individual pull-ups to be enabled.

2: The weak pull-up device is automatically disabled if the pin is in configured as an output.

REGISTER 6-8: IOCB: INTERRUPT-ON-CHANGE PORTB REGISTER

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IOCB7 | IOCB6 | IOCB5 | IOCB4 | IOCB3 | IOCB2 | IOCB1 | IOCB0 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **IOCB<7:0>:** Interrupt-on-Change PORTB Control bits

1 = Interrupt-on-change enabled

0 = Interrupt-on-change disabled

REGISTER 6-9: ANSELB: PORTB ANALOG SELECT REGISTER

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 Unimplemented: Read as '0'

bit 5-0 ANSB<5:0>: Analog Select between Analog or Digital Function on Pins RB<5:0>, respectively

0 = Digital I/O. Pin is assigned to port or Digital special function.

1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital Input buffer disabled.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.



FIGURE 6-10: BLOCK DIAGRAM OF RB5









12.7 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt on rollover, you must set these bits:

- TMR1ON bit of the T1CON register
- TMR1IE bit of the PIE1 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

Note: The TMR1H:TMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

12.8 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- TMR1ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set
- TISYNC bit of the T1CON register must be set
- TMR1CS bits of the T1CON register must be configured
- T1OSCEN bit of the T1CON register must be configured
- TMR1GIE bit of the T1GCON register must be configured

The device will wake-up on an overflow and execute the next instructions. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine (0004h).

12.9 CCP Capture/Compare Time Base

The CCP module uses the TMR1H:TMR1L register pair as the time base when operating in Capture or Compare mode.

In Capture mode, the value in the TMR1H:TMR1L register pair is copied into the CCPR1H:CCPR1L register pair on a configured event.

In Compare mode, an event is triggered when the value CCPR1H:CCPR1L register pair matches the value in the TMR1H:TMR1L register pair. This event can be a Special Event Trigger.

For more information, see Section 15.0 "Capture/Compare/PWM (CCP) Module".

12.10 CCP Special Event Trigger

When the CCP is configured to trigger a special event, the trigger will clear the TMR1H:TMR1L register pair. This special event does not cause a Timer1 interrupt. The CCP module may still be configured to generate a CCP interrupt.

In this mode of operation, the CCPR1H:CCPR1L register pair becomes the period register for Timer1.

Timer1 should be synchronized to the Fosc/4 to utilize the Special Event Trigger. Asynchronous operation of Timer1 can cause a Special Event Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with a Special Event Trigger from the CCP, the write will take precedence.

For more information, see Section 9.2.5 "Special Event Trigger".



FIGURE 12-2: TIMER1 INCREMENTING EDGE

17.1.2 SLAVE MODE

For any SPI device acting as a slave, the data is transmitted and received as external clock pulses appear on SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

17.1.2.1 Slave Mode Operation

The SSP consists of a transmit/receive shift register (SSPSR) and a buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPBUF holds the data that was written to the SSPSR until the received data is ready.

The slave has no control as to when data will be clocked in or out of the device. All data that is to be transmitted, to a master or another slave, must be loaded into the SSPBUF register before the first clock pulse is received.

Once eight bits of data have been received:

- · Received byte is moved to the SSPBUF register
- BF bit of the SSPSTAT register is set
- SSPIF bit of the PIR1 register is set

Any write to the SSPBUF register during transmission/reception of data will be ignored and the Write Collision Detect bit, WCOL of the SSPCON register, will be set. User software must clear the WCOL bit so that it can be determined if the following write(s) to the SSPBUF register completed successfully.

The user's firmware must read SSPBUF, clearing the BF flag, or the SSPOV bit of the SSPCON register will be set with the reception of the next byte and communication will be disabled.

A SPI module transmits and receives at the same time, occasionally causing dummy data to be transmitted/received. It is up to the user to determine which data is to be used and what can be discarded.

17.1.2.2 Enabling Slave I/O

To enable the serial port, the SSPEN bit of the SSPCON register must be set. If a Slave mode of operation is selected in the SSPM bits of the SSPCON register, the SDI, SDO, SCK pins will be assigned as serial port pins.

For these pins to function as serial port pins, they must have their corresponding data direction bits set or cleared in the associated TRIS register as follows:

- · SDI configured as input
- · SDO configured as output
- · SCK configured as input

Optionally, a fourth pin, Slave Select (\overline{SS}) may be used in Slave mode. Slave Select may be configured to operate on one of the following pins via the SSSEL bit in the APFCON register.

- RA5/AN4/SS
- RA0/AN0/SS

Upon selection of a Slave Select pin, the appropriate bits must be set in the ANSELA and TRISA registers. Slave Select must be set as an input by setting the corresponding bit in TRISA, and digital I/O must be enabled on the SS pin by clearing the corresponding bit of the ANSELA register.

17.1.2.3 Slave Mode Setup

When initializing the SSP module to SPI Slave mode, compatibility must be ensured with the master device. This is done by programming the appropriate control bits of the SSPCON and SSPSTAT registers. These control bits allow the following to be specified:

- · SCK as clock input
- Idle state of SCK (CKP bit)
- Data input sample phase (SMP bit)
- Output data on rising/falling edge of SCK (CKE bit)

Figure 17-4 and Figure 17-5 show example waveforms of Slave mode operation.

17.2.2 START AND STOP CONDITIONS

During times of no data transfer (Idle time), both the clock line (SCL) and the data line (SDA) are pulled high through external pull-up resistors. The Start and Stop conditions determine the start and stop of data transmission. The Start condition is defined as a high-to-low transition of the SDA line while SCL is high. The Stop condition is defined as a low-to-high transition of the SDA line while SCL is high.

Figure 17-9 shows the Start and Stop conditions. A master device generates these conditions for starting and terminating data transfer. Due to the definition of the Start and Stop conditions, when data is being transmitted, the SDA line can only change state when the SCL line is low.

17.2.3 ACKNOWLEDGE

After the valid reception of an address or data byte, the hardware automatically will generate the Acknowledge (ACK) pulse and load the SSPBUF register with the received value currently in the SSPSR register. There are certain conditions that will cause the SSP module not to generate this ACK pulse. They include any or all of the following:

- The Buffer Full bit, BF of the SSPSTAT register, was set before the transfer was received.
- The SSP Overflow bit, SSPOV of the SSPCON register, was set before the transfer was received.
- The SSP Module is being operated in Firmware Master mode.

In such a case, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF of the PIR1 register is set. Table 17-2 shows the results of when a data transfer byte is received, given the status of bits BF and SSPOV. Flag bit BF is cleared by reading the SSPBUF register, while bit SSPOV is cleared through software.

FIGURE 17-9: START AND STOP CONDITIONS

TABLE 17-2:	DATA TRANSFER RECEIVED BYTE ACTIONS

Status Bits as Data Transfer is Received		$SSPSR \to SSPBUF$	Generate ACK	Set bit SSPIF (SSP Interrupt occurs		
BF	SSPOV		Fuise	if enabled)		
0	0	Yes	Yes	Yes		
1	0	No	No	Yes		
1	1	No	No	Yes		
0	1	No	No	Yes		

Note 1: Shaded cells show the conditions where the user software did not properly clear the overflow condition.

SUBWF	Subtract W from f				
Syntax:	[label] Sl	JBWF f,d			
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$				
Operation:	(f) - (W) \rightarrow (destination)				
Status Affected:	C, DC, Z				
Description:	Subtract (2's complement method W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f.				
	C = 0	W > f			
	C = 1	W < f			

 $\overline{DC} = 0$

DC = 1

W<3:0> > f<3:0> W<3:0> \leq f<3:0>

XORLW	Exclusive OR literal with W				
Syntax:	[<i>label</i>] XORLW k				
Operands:	$0 \leq k \leq 255$				
Operation:	(W) .XOR. $k \rightarrow (W)$				
Status Affected:	Z				
Description:	The contents of the W register are XOR'ed with the 8-bit literal 'k'. The result is placed in the W register.				

SWAPF	Swap Nibbles in f				
Syntax:	[label] SWAPF f,d				
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$				
Operation:	$(f<3:0>) \rightarrow (destination<7:4>),$ $(f<7:4>) \rightarrow (destination<3:0>)$				
Status Affected:	None				
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.				

XORWF	Exclusive OR W with f				
Syntax:	[label] XORWF f,d				
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$				
Operation:	(W) .XOR. (f) \rightarrow (destination)				
Status Affected:	Z				
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.				

22.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM[™] and dsPICDEM[™] demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ[®] security ICs, CAN, IrDA[®], PowerSmart battery management, SEEVAL[®] evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

22.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent[®] and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika[®]

TABLE 23-2: **OSCILLATOR PARAMETERS**

Standar Operatir	Standard Operating Conditions (unless otherwise stated)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$							
Param No.	Sym.	Characteristic	Freq. Tolerance	Min.	Тур†	Max.	Units	Conditions
OS08	HFosc	Internal Calibrated HFINTOSC Frequency ⁽²⁾	±2%		16.0	_	MHz	$\begin{array}{l} 0^{\circ}C \leq TA \leq \texttt{+85}^{\circ}C, \\ V\text{DD} \geq 2.5 V \end{array}$
			±5%	—	16.0	—	MHz	$-40^{\circ}C \leq TA \leq +125^{\circ}C$
OS08A	MFosc	Internal Calibrated MFINTOSC Frequency ⁽²⁾	±2%		500	—	kHz	$0^{\circ}C \le TA \le +85^{\circ}C$ VDD $\ge 2.5V$
			±5%	—	500	10	kHz	$-40^{\circ}C \leq TA \leq +125^{\circ}C$
OS10*	TIOSC ST	HFINTOSC Wake-up from Sleep Start-up Time	—		5	8	μS	
		MFINTOSC Wake-up from Sleep Start-up Time	_	—	20	30	μS	

These parameters are characterized but not tested.

Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are t not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: To ensure these oscillator frequency tolerances, VDD and Vss must be capacitively decoupled as close to the device as possible. 0.1 μ F and 0.01 μ F values in parallel are recommended.

3: By design.

a. . . .







FIGURE 23-16: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)







FIGURE 24-21: PIC16F722/3/4/6/7 MAXIMUM IDD vs. Fosc OVER VDD, INTOSC MODE, VCAP =1µF





25.2 Package Details

The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES		
Dimensio	Dimension Limits		NOM	MAX	
Number of Pins	Ν	28			
Pitch	е	.100 BSC			
Top to Seating Plane	Α	-	-	.200	
Molded Package Thickness	A2	.120	.135	.150	
Base to Seating Plane	A1	.015	-	-	
Shoulder to Shoulder Width	E	.290	.310	.335	
Molded Package Width	E1	.240	.285	.295	
Overall Length	D	1.345	1.365	1.400	
Tip to Seating Plane	L	.110	.130	.150	
Lead Thickness	с	.008	.010	.015	
Upper Lead Width	b1	.040	.050	.070	
Lower Lead Width	b	.014	.018	.022	
Overall Row Spacing §	eB	_	_	.430	

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic.
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-152A Sheet 1 of 2

NOTES: