Microchip Technology - PIC16F726T-I/SO Datasheet





Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f726t-i-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Website at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Website; http://www.microchip.com
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our website at www.microchip.com to receive the most current information on all of our products.

1.0 DEVICE OVERVIEW

The PIC16(L)F722/3/4/6/7 devices are covered by this data sheet. They are available in 28/40/44-pin packages. Figure 1-1 shows a block diagram of the PIC16F722/723/726/PIC16LF722/723/726 devices and Figure 1-2 shows a block diagram of the PIC16F724/727/PIC16LF724/727 devices. Table 1-1 shows the pinout descriptions.

PIC16(L)F722/3/4/6/7

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Page
Bank 2	Bank 2										
100h ⁽²⁾	INDF	Addressing	this location	uses conten	ts of FSR to a	ddress data	memory (not	a physical re	gister)	xxxx xxxx	29,37
101h	TMR0	Timer0 Mod	ule Register							xxxx xxxx	105,37
102h ⁽²⁾	PCL	Program Co	unter's (PC)	Least Signif	icant Byte					0000 0000	28,37
103h ⁽²⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	25,37
104h ⁽²⁾	FSR	Indirect Data	a Memory Ac	dress Point	er					xxxx xxxx	29,37
105h	_	Unimplemen	nted							_	_
106h	_	Unimplemen	nted							_	_
107h	—	Unimplemen	nted								_
108h	CPSCON0	CPSON	_	_	_	CPSRNG1	CPSRNG0	CPSOUT	TOXCS	0 0000	126,38
109h	CPSCON1	—	_	_	_	CPSCH3	CPSCH2	CPSCH1	CPSCH0	0000	127,38
10Ah ^(1, 2)	PCLATH	—	_	_	Write Buffer	for the upper	5 bits of the F	Program Cou	nter	0 0000	28,37
10Bh ⁽²⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	44,37
10Ch	PMDATL	Program Me	mory Read	Data Registe	er Low Byte					XXXX XXXX	181,38
10Dh	PMADRL	Program Me	mory Read	Address Reg	gister Low Byt	е				XXXX XXXX	181,38
10Eh	PMDATH	—	_	Program Me	emory Read D	Data Register	High Byte			xx xxxx	181,38
10Fh	PMADRH	—	—	—	Program Me	mory Read A	ddress Regis	ter High Byte	1	x xxxx	181,38
Bank 3											
180h ⁽²⁾	INDF	Addressing	this location	uses conten	ts of FSR to a	ddress data	memory (not	a physical re	gister)	XXXX XXXX	29,37
181h	OPTION_REG	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	26,37
182h ⁽²⁾	PCL	Program Co	unter (PC) L	east Signific	ant Byte					0000 0000	28,37
183h ⁽²⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	25,37
184h ⁽²⁾	FSR	Indirect Data	a Memory Ac	dress Point	er					XXXX XXXX	29,37
185h	ANSELA	—	_	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	11 1111	52,38
186h	ANSELB		_	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	11 1111	61,38
187h	—	Unimplemen	nted								_
188h	ANSELD	ANSD7	ANSD6	ANSD5	ANSD4	ANSD3	ANSD2	ANSD1	ANSD0	1111 1111	78,38
189h ⁽³⁾	ANSELE	—	_	_	_	—	ANSE2	ANSE1	ANSE0	111	82,38
18Ah ^(1, 2)	PCLATH	—	_	_	Write Buffer	for the upper	5 bits of the F	Program Cou	nter	0 0000	28,37
18Bh ⁽²⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	44,37
18Ch	PMCON1	Reserved	_	—	—	—	—	—	RD	10	182,38
18Dh	—	Unimplemen	nted							-	-
18Eh	—	Unimplemen	nted							-	-
18Fh	—	Unimplemen	nted							_	_

TABLE 2-1: PIC16(L)F722/3/4/6/7 SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'. Legend:

The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter. Note 1:

These registers can be addressed from any bank. 2:

These registers/bits are not implemented on PIC16F722/723/726/PIC16LF722/723/726 devices, read as '0'. Accessible only when SSPM<3:0> = 1001. Accessible only when SSPM<3:0> \neq 1001. This bit is always '1' as RE3 is input-only. 3:

4:

5:

6:

3.4.2 WDT CONTROL

The WDTE bit is located in the Configuration Word Register 1. When set, the WDT runs continuously.

The PSA and PS<2:0> bits of the OPTION register control the WDT period. See **Section 11.0 "Timer0 Module"** for more information.





TABLE 3-1: WDT STATUS

Conditions	WDT
WDTE = 0	Cleared
CLRWDT Command	
Exit Sleep + System Clock = T1OSC, EXTRC, INTOSC, EXTCLK	
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST

REGISTER 6-5: PORTB: PORTB REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0		
bit 7 bit									
Legend:	Legend:								
R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'						
-n = Value at POR '1' = Bit is set			0' = Bit is cleared $x = Bit is unknown$						

bit 7-0 **RB<7:0>**: PORTB I/O Pin bit 1 = Port pin is > VIH 0 = Port pin is < VIL

REGISTER 6-6: TRISB: PORTB TRI-STATE REGISTER

| R/W-1 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| TRISB7 | TRISB6 | TRISB5 | TRISB4 | TRISB3 | TRISB2 | TRISB1 | TRISB0 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 TRISB<7:0>: PORTB Tri-State Control bit

1 = PORTB pin configured as an input (tri-stated)

0 = PORTB pin configured as an output

PIC16(L)F722/3/4/6/7

FIGURE 6-10: BLOCK DIAGRAM OF RB5



7.0 OSCILLATOR MODULE

7.1 Overview

The oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 7-1 illustrates a block diagram of the oscillator module.

Clock sources can be configured from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system can be configured to use an internal calibrated high-frequency oscillator as clock source, with a choice of selectable speeds via software.

Clock source modes are configured by the FOSC bits in Configuration Word 1 (CONFIG1). The oscillator module can be configured for one of eight modes of operation.

- 1. RC External Resistor-Capacitor (RC) with Fosc/4 output on OSC2/CLKOUT.
- 2. RCIO External Resistor-Capacitor (RC) with I/O on OSC2/CLKOUT.
- 3. INTOSC Internal oscillator with Fosc/4 output on OSC2 and I/O on OSC1/CLKIN.
- 4. INTOSCIO Internal oscillator with I/O on OSC1/CLKIN and OSC2/CLKOUT.
- 5. EC External clock with I/O on OSC2/CLKOUT.
- 6. HS High Gain Crystal or Ceramic Resonator mode.
- 7. XT Medium Gain Crystal or Ceramic Resonator Oscillator mode.
- 8. LP Low-Power Crystal mode.



FIGURE 7-1: SIMPLIFIED PIC[®] MCU CLOCK SOURCE BLOCK DIAGRAM

12.6 Timer1 Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using Timer1 Gate circuitry. This is also referred to as Timer1 Gate Count Enable.

Timer1 Gate can also be driven by multiple selectable sources.

12.6.1 TIMER1 GATE COUNT ENABLE

The Timer1 Gate is enabled by setting the TMR1GE bit of the T1GCON register. The polarity of the Timer1 Gate is configured using the T1GPOL bit of the T1GCON register.

When Timer1 Gate (T1G) input is active, Timer1 will increment on the rising edge of the Timer1 clock source. When Timer1 Gate input is inactive, no incrementing will occur and Timer1 will hold the current count. See Figure 12-3 for timing details.

TABLE 12-3: TIMER1 GATE ENABLE SELECTIONS

T1CLK	T1GPOL	T1G	Timer1 Operation
\uparrow	0	0	Counts
1	0	1	Holds Count
\uparrow	1	0	Holds Count
\uparrow	1	1	Counts

12.6.2 TIMER1 GATE SOURCE SELECTION

The Timer1 Gate source can be selected from one of four different sources. Source selection is controlled by the T1GSS bits of the T1GCON register. The polarity for each available source is also selectable. Polarity selection is controlled by the T1GPOL bit of the T1GCON register.

TABLE 12-4: TIMER1 GATE SOURCES

T1GSS	Timer1 Gate Source
00	Timer1 Gate Pin
01	Overflow of Timer0 (TMR0 increments from FFh to 00h)
10	Timer2 match PR2 (TMR2 increments to match PR2)
11	Count Enabled by WDT Overflow (Watchdog Time-out interval expired)

12.6.2.1 T1G Pin Gate Operation

The T1G pin is one source for Timer1 Gate Control. It can be used to supply an external source to the Timer1 Gate circuitry.

12.6.2.2 Timer0 Overflow Gate Operation

When Timer0 increments from FFh to 00h, a low-to-high pulse will automatically be generated and internally supplied to the Timer1 Gate circuitry.

12.6.2.3 Timer2 Match Gate Operation

The TMR2 register will increment until it matches the value in the PR2 register. On the very next increment cycle, TMR2 will be reset to 00h. When this Reset occurs, a low-to-high pulse will automatically be generated and internally supplied to the Timer1 Gate circuitry.

12.6.2.4 Watchdog Overflow Gate Operation

The Watchdog Timer oscillator, prescaler and counter will be automatically turned on when TMR1GE = 1 and T1GSS selects the WDT as a gate source for Timer1 (T1GSS = 11). TMR1ON does not factor into the oscillator, prescaler and counter enable. See Table 12-5.

The PSA and PS bits of the OPTION register still control what time-out interval is selected. Changing the prescaler during operation may result in a spurious capture.

Enabling the Watchdog Timer oscillator does not automatically enable a Watchdog Reset or Wake-up from Sleep upon counter overflow.

Note:	When using the WDT as a gate source for
	limer1, operations that clear the Watchdog
	Timer (CLRWDT, SLEEP instructions) will
	affect the time interval being measured for
	capacitive sensing. This includes waking
	from Sleep. All other interrupts that might
	wake the device from Sleep should be
	disabled to prevent them from disturbing
	the measurement period.

As the gate signal coming from the WDT counter will generate different pulse widths depending on if the WDT is enabled, when the CLRWDT instruction is executed, and so on, Toggle mode must be used. A specific sequence is required to put the device into the correct state to capture the next WDT counter interval.

PIC16(L)F722/3/4/6/7



FIGURE 12-4: TIMER1 GATE TOGGLE MODE



17.0 SSP MODULE OVERVIEW

The Synchronous Serial Port (SSP) module is a serial interface useful for communicating with other peripherals or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I²C)

17.1 SPI Mode

The SPI mode allows eight bits of data to be synchronously transmitted and received, simultaneously. The SSP module can be operated in one of two SPI modes:

- Master mode
- Slave mode

SPI is a full-duplex protocol, with all communication being bidirectional and initiated by a master device. All clocking is provided by the master device and all bits are transmitted, MSb first. Care must be taken to ensure that all devices on the SPI bus are setup to allow all controllers to send and receive data at the same time. A typical SPI connection between microcontroller devices is shown in Figure 17-1. Addressing of more than one slave device is accomplished via multiple hardware slave select lines. External hardware and additional I/O pins must be used to support multiple slave select addressing. This prevents extra overhead in software for communication.

For SPI communication, typically three pins are used:

- Serial Data Out (SDO)
- Serial Data In (SDI)
- Serial Clock (SCK)

Additionally, a fourth pin may be used when in a Slave mode of operation:

Slave Select (SS)





17.1.1 MASTER MODE

In Master mode, data transfer can be initiated at any time because the master controls the SCK line. Master mode determines when the slave (Figure 17-1, Processor 2) transmits data via control of the SCK line.

17.1.1.1 Master Mode Operation

The SSP consists of a transmit/receive shift register (SSPSR) and a buffer register (SSPBUF). The SSPSR register shifts the data in and out of the device, MSb first. The SSPBUF register holds the data that is written out of the master until the received data is ready. Once the eight bits of data have been received, the byte is moved to the SSPBUF register. The Buffer Full Status bit, BF of the SSPSTAT register, and the SSP Interrupt Flag bit, SSPIF of the PIR1 register, are then set.

Any write to the SSPBUF register during transmission/reception of data will be ignored and the Write Collision Detect bit, WCOL of the SSPCON register, will be set. User software must clear the WCOL bit so that it can be determined if the following write(s) to the SSPBUF register completed successfully.

When the application software is expecting to receive valid data, the SSPBUF should be read before the next byte of data is written to the SSPBUF. The BF bit of the SSPSTAT register is set when SSPBUF has been loaded with the received data (transmission is complete). When the SSPBUF is read, the BF bit is cleared. This data may be irrelevant if the SPI is only a transmitter. The SSP interrupt may be used to determine when the transmission/reception is complete and the SSPBUF must be read and/or written. If interrupts are not used, then software polling can be done to ensure that a write collision does not occur. Example 17-1 shows the loading of the SSPBUF (SSPSR) for data transmission.

Note: The SSPSR is not directly readable or writable and can only be accessed by addressing the SSPBUF register.

17.1.1.2 Enabling Master I/O

To enable the serial port, the SSPEN bit of the SSPCON register, must be set. To reset or reconfigure SPI mode, clear the SSPEN bit, re-initialize the SSPCON register and then set the SSPEN bit. If a Master mode of operation is selected in the SSPM bits of the SSPCON register, the SDI, SDO and SCK pins will be assigned as serial port pins.

For these pins to function as serial port pins, they must have their corresponding data direction bits set or cleared in the associated TRIS register as follows:

- · SDI configured as input
- SDO configured as output
- SCK configured as output

17.1.1.3 Master Mode Setup

In Master mode, the data is transmitted/received as soon as the SSPBUF register is loaded with a byte value. If the master is only going to receive, SDO output could be disabled (programmed and used as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate.

When initializing SPI Master mode operation, several options need to be specified. This is accomplished by programming the appropriate control bits in the SSPCON and SSPSTAT registers. These control bits allow the following to be specified:

- SCK as clock output
- Idle state of SCK (CKP bit)
- Data input sample phase (SMP bit)
- Output data on rising/falling edge of SCK (CKE bit)
- Clock bit rate

In Master mode, the SPI clock rate (bit rate) is user selectable to be one of the following:

- Fosc/4 (or TCY)
- Fosc/16 (or 4 TCY)
- Fosc/64 (or 16 TCY)
- (Timer2 output)/2

This allows a maximum data rate of 5 Mbps (at Fosc = 20 MHz).

Figure 17-3 shows the waveforms for Master mode. The clock polarity is selected by appropriately programming the CKP bit of the SSPCON register. When the CKE bit is set, the SDO data is valid before there is a clock edge on SCK. The sample time of the input data is shown based on the state of the SMP bit and can occur at the middle or end of the data output time. The time when the SSPBUF is loaded with the received data is shown.

17.1.1.4 Sleep in Master Mode

In Master mode, all module clocks are halted and the transmission/reception will remain in their current state, paused, until the device wakes from Sleep. After the device wakes up from Sleep, the module will continue to transmit/receive data.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	11 1111	11 1111
APFCON	_	—	—	—	-	-	SSSEL	CCP2SEL	00	00
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PR2	Timer2 Peri	od Register							1111 1111	1111 1111
SSPBUF	Synchronou	us Serial Port	Receive But	fer/Transmit	Register				XXXX XXXX	uuuu uuuu
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
SSPSTAT	SMP	CKE	D/A	Р	S	R/W	UA	BF	0000 0000	0000 0000
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111	1111 1111
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
T2CON		TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000

TABLE 17-1: SUMMARY OF REGISTERS ASSOCIATED WITH SPI OPERATION

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the SSP in SPI mode.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0			
bit 7	·	·					bit 0			
Legend:	1.5		,							
R = Readabl	e bit	VV = VVritable	bit	U = Unimpler	nented bit, rea	d as '0'				
-n = Value at	POR	'1' = Bit is set		0' = Bit is cle	ared	x = Bit is unki	nown			
bit 7	WCOL: Write	e Collision Dete	ct bit							
	1 = The SSF	PBUF register is	s written while	e it is still transn	nitting the prev	ious word (mus	t be cleared in			
	software	e)								
1.11.0	0 = INO COIIIS		P 4 1 1							
DIT 6	SSPOV: Rec	eive Overflow II	ndicator bit							
	$\perp = A byte Is$	A byte is received while the SSPBUF register is still holding the previous byte. SSPOV is a "don't care" in Transmit mode. SSPOV must be cleared in software in either mode.								
	0 = No overf	flow				ier mode.				
bit 5	SSPEN: Syn	chronous Serial	Port Enable	bit						
	1 = Enables	the serial port a	ne serial port and configures the SDA and SCL pins as serial port pins ⁽²⁾							
	0 = Disables	serial port and	configures th	ese pins as I/O	port pins					
bit 4	CKP: Clock F	Polarity Select b	oit							
	1 = Release	control of SCL								
	0 = Holds cld	ock low (clock st	retch). (Usec	I to ensure data	setup time.)					
bit 3-0	SSPM<3:0>:	Synchronous S	Serial Port Mo	ode Select bits						
	$0110 = I^2 C S$	Slave mode, 7-b	it address							
	1000 = Rese	ave mode, 10-	DIL AUULESS							
	1001 = Load	SSPMSK regis	ter at SSPAD	D SFR Addres	_S (1)					
	1010 = Rese	erved								
	$1011 = I^2 C F$	irmware Contro	olled Master r	node (Slave Idle	e)					
	1100 = Rese	erved								
	1101 = Rese $1110 = I^2 C S$	Slave mode 7-b	it address wit	th Start and Sto	n hit interrunts	enabled				
	1110 = 1000 $1111 = 1^{2}CS$	Slave mode, 10-	bit address w	vith Start and St	op bit interrupt	s enabled				
Note 1: V	When this mode is	s selected, anv re	eads or writes	to the SSPADD	SFR address a	accesses the SS	PMSK reaister.			

REGISTER 17-3: SSPCON: SYNCHRONOUS SERIAL PORT CONTROL REGISTER (I²C MODE)

- - 2: When enabled, these pins must be properly configured as input or output using the associated TRIS bit.

18.0 PROGRAM MEMORY READ

The Flash program memory is readable during normal operation over the full VDD range of the device. To read data from Program Memory, five Special Function Registers (SFRs) are used:

- PMCON1
- PMDATL
- PMDATH
- PMADRL
- PMADRH

The value written to the PMADRH:PMADRL register pair determines which program memory location is read. The read operation will be initiated by setting the RD bit of the PMCON1 register. The program memory flash controller takes two instructions to complete the read, causing the second instruction after the setting the RD bit will be ignored. To avoid conflict with program execution, it is recommended that the two instructions following the setting of the RD bit are NOP. When the read completes, the result is placed in the PMDATLH:PMDATL register pair. Refer to Example 18-1 for sample code.

Note: Code-protect does not effect the CPU from performing a read operation on the program memory. For more information, refer to Section 8.2 "Code Protection".

=				
		BANKSEL MOVF MOVWF MOVF	PMADRL MS_PROG_ADDR, PMADRH LS_PROG_ADDR,	; W; ;MS Byte of Program Address to read W;
		MOVWF	PMADRL	;LS Byte of Program Address to read
		BANKSEL	PMCON1	i
	ed	BSF	PMCON1, RD	;Initiate Read
	uen	NOP		
	Sec	NOP		;Any instructions here are ignored as program
	<u> </u>			;memory is read in second cycle after BSF
		BANKSEL	PMDATL	;
		MOVF	PMDATL, W	;W = LS Byte of Program Memory Read
		MOVWF	LOWPMBYTE	;
		MOVF	PMDATH, W	;W = MS Byte of Program Memory Read
l		MOVWF	HIGHPMBYTE	;

EXAMPLE 18-1: PROGRAM MEMORY READ

20.0 IN-CIRCUIT SERIAL PROGRAMMING[™] (ICSP[™])

ICSP[™] programming allows customers to manufacture circuit boards with unprogrammed devices. Programming can be done after the assembly process allowing the device to be programmed with the most recent firmware or a custom firmware. Five pins are needed for ICSP[™] programming:

- ICSPCLK
- ICSPDAT
- MCLR/VPP
- VDD
- Vss

The device is placed into Program/Verify mode by holding the ICSPCLK and ICSPDAT pins low then raising the voltage on MCLR/VPP from 0v to VPP. In Program/Verify mode the program memory, User IDs and the Configuration Words are programmed through serial communications. The ICSPDAT pin is a bidirectional I/O used for transferring the serial data and the ISCPCLK pin is the clock input. For more information on ICSP, refer to the "*PIC16(L)F72x Memory Programming Specification*" (DS41332).

Note: The ICD 2 produces a VPP voltage greater than the maximum VPP specification of the PIC16(L)F722/3/4/6/7. When using this programmer, an external circuit, such as the AC164112 MPLAB ICD 2 VPP voltage limiter, is required to keep the VPP voltage within the device specifications.



FIGURE 20-1: TYPICAL CONNECTION FOR ICSP™ PROGRAMMING

Mnemonic, Operands		Description	Cyclos	14-Bit Opcode				Status	Notos
		Description	Cycles	MSb			LSb	Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C, DC, Z	1, 2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1, 2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1, 2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1, 2
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	00	1011	dfff	ffff		1, 2, 3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1, 2
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	00	1111	dfff	ffff		1, 2, 3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1, 2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1, 2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	С	1, 2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	С	1, 2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C, DC, Z	1, 2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1, 2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1, 2
		BIT-ORIENTED FILE REGIST		RATION	IS				•
BCF	f. b	Bit Clear f	1	01	00bb	bfff	ffff		1.2
BSF	f. b	Bit Set f	1	01	01bb	bfff	ffff		1.2
BTFSC	f. b	Bit Test f. Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f. b	Bit Test f. Skip if Set	1 (2)	01	11bb	bfff	ffff		3
	, -	LITERAL AND CONTROL	OPERAT	IONS					
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C, DC, Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call Subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO, PD	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into Standby mode	1	00	0000	0110	0011	TO, PD	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C, DC, Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

TABLE 21-2: PIC16(L)F722/3/4/6/7 INSTRUCTION SET

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTA, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

3: If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

Param. No.	Symbol	Characteristic		Min.	Тур†	Max.	Units	Conditions
CS01	ISRC	Current Source	High	—	-5.8	-6	μΑ	
			Medium	—	-1.1	-3.2	μΑ	-40, -85°C
			Low	—	-0.2	-0.9	μΑ	
CS02	Isnk	Current Sink	High	—	6.6	6	μΑ	
			Medium	_	1.3	3.2	μΑ	-40, -85°C
			Low	—	0.24	0.9	μΑ	
CS03	VCHYST	Cap Hysteresis	High	—	525	—	mV	
			Medium	—	375	—	mV	VCTH-VCTL
			Low	_	280	_	mV	

TABLE 23-14: CAP SENSE OSCILLATOR SPECIFICATIONS

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



FIGURE 23-22: CAP SENSE OSCILLATOR

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Contact Pitch	0.65 BSC				
Optional Center Pad Width	W2			4.25	
Optional Center Pad Length	T2			4.25	
Contact Pad Spacing	C1		5.70		
Contact Pad Spacing	C2		5.70		
Contact Pad Width (X28)	X1			0.37	
Contact Pad Length (X28)	Y1			1.00	
Distance Between Pads	G	0.20			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS				
Dimensi	MIN	NOM	MAX			
Number of Pins	Ν					
Pitch	е	0.65 BSC				
Overall Height	Α	-	-	2.00		
Molded Package Thickness	A2	1.65	1.75	1.85		
Standoff	A1	0.05	-	-		
Overall Width	E	7.40	7.80	8.20		
Molded Package Width	E1	5.00	5.30	5.60		
Overall Length	D	9.90	10.20	10.50		
Foot Length	L	0.55	0.75	0.95		
Footprint	L1	1.25 REF				
Lead Thickness	С	0.09	-	0.25		
Foot Angle	φ	0°	4°	8°		
Lead Width	b	0.22	-	0.38		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.

- 3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Contact Pitch E		0.80 BSC			
Contact Pad Spacing	C1		11.40		
Contact Pad Spacing	C2		11.40		
Contact Pad Width (X44)	X1			0.55	
Contact Pad Length (X44)	Y1			1.50	
Distance Between Pads	G	0.25			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076A