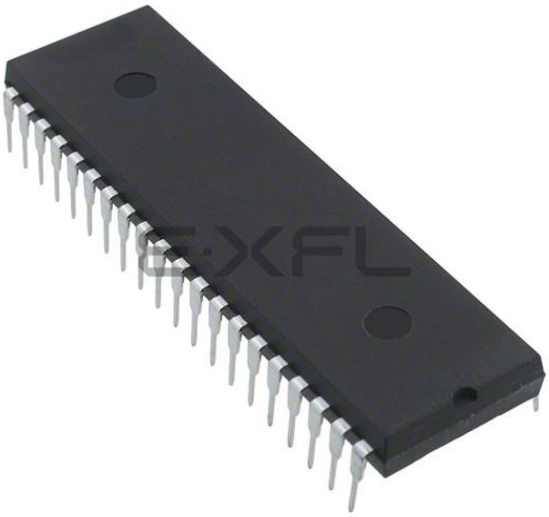
# Microchip Technology - PIC16F727-E/P Datasheet



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## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 36 |
| Program Memory Size | 14KB (8K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 368 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 14x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 40-DIP (0.600", 15.24mm) |
| Supplier Device Package | 40-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16f727-e-p |

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# 2.0 MEMORY ORGANIZATION

## 2.1 Program Memory Organization

The PIC16(L)F722/3/4/6/7 has a 13-bit program counter capable of addressing a 2K x 14 program memory space for the PIC16F722/LF722 (0000h-07FFh), a 4K x 14 program memory space for the PIC16F723/LF723 and PIC16F724/LF724 (0000h-0FFFh) and an 8K x 14 program memory space for the PIC16F726/LF726 and PIC16F727/LF727 (0000h-1FFFh). Accessing a location above the memory boundaries for the PIC16F722/LF722 will cause a wrap-around within the first 2K x 14 program memory space. Accessing a location above the memory boundaries for the PIC16F723/LF723 and PIC16F724/LF724 will cause a wrap-around within the first 4K x 14 program memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h.

**FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F722/LF722**

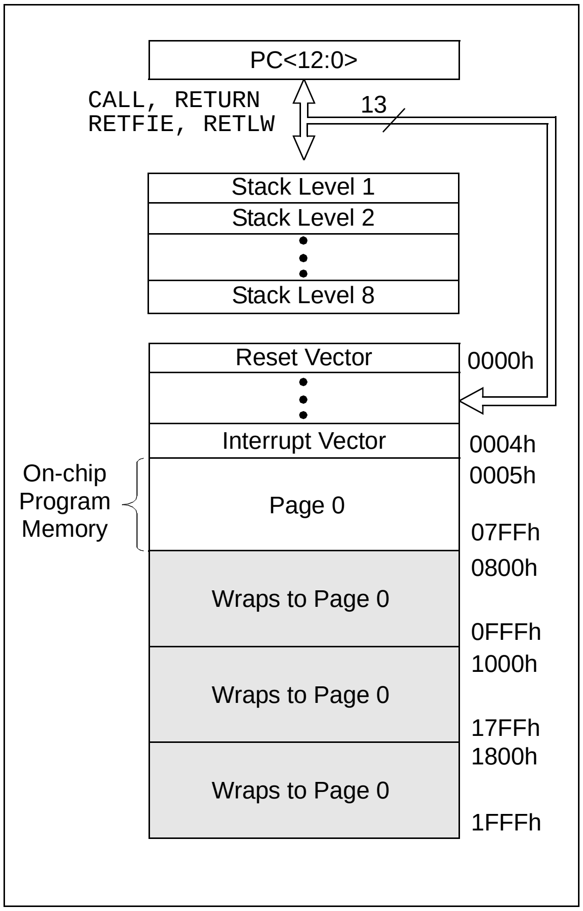
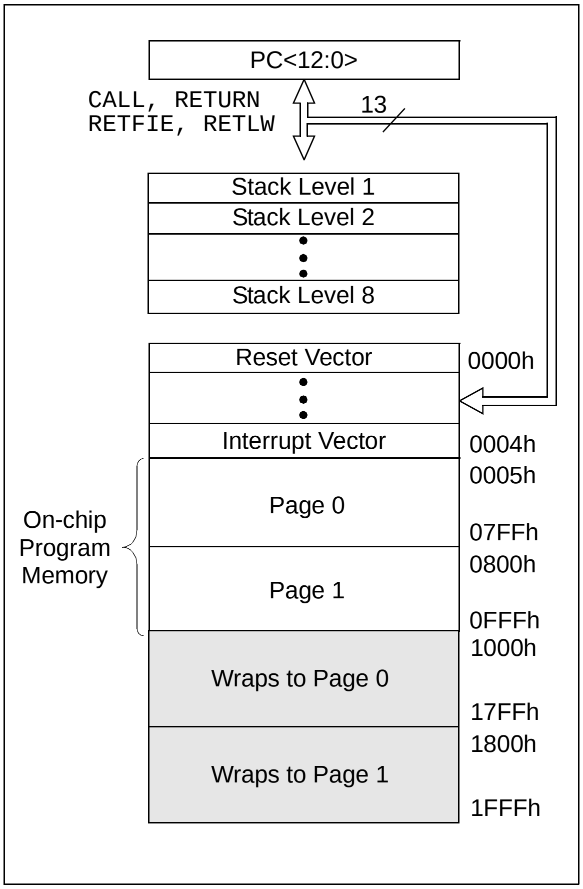

PC<12:0>
CALL, RETURN
RETFIE, RETLW
13
Stack Level 1
Stack Level 2
Stack Level 8
Reset Vector
0000h
Interrupt Vector
0004h
0005h
On-chip
Program
Memory
Page 0
07FFh
0800h
Wraps to Page 0
0FFFh
1000h
Wraps to Page 0
17FFh
1800h
Wraps to Page 0
1FFFh

**FIGURE 2-2: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F723/LF723 AND PIC16F724/LF724**


PC<12:0>
CALL, RETURN
RETFIE, RETLW
13
Stack Level 1
Stack Level 2
Stack Level 8
Reset Vector
0000h
Interrupt Vector
0004h
0005h
On-chip
Program
Memory
Page 0
07FFh
0800h
Page 1
0FFFh
1000h
Wraps to Page 0
17FFh
1800h
Wraps to Page 1
1FFFh

### 4.5.3 PIE2 REGISTER

The PIE2 register contains the interrupt enable bits, as shown in Register 4-3.

> **Note:** Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

### REGISTER 4-3: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | CCP2IE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-1 **Unimplemented:** Read as ‘`0`’

bit 0 **CCP2IE:** CCP2 Interrupt Enable bit

`1` = Enables the CCP2 interrupt
`0` = Disables the CCP2 interrupt

### TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| ADCON0 | — | — | CHS3 | CHS2 | CHS1 | CHS0 | GO/$\overline{\text{DONE}}$ | ADON | 0000 0000 | 0000 0000 |
| ADCON1 | — | ADCS2 | ADCS1 | ADCS0 | — | — | ADREF1 | ADREF0 | -000 --00 | -000 --00 |
| ANSELA | — | — | ANSA5 | ANSA4 | ANSA3 | ANSA2 | ANSA1 | ANSA0 | --11 1111 | --11 1111 |
| APFCON | — | — | — | — | — | — | SSSEL | CCP2SEL | ---- --00 | ---- --00 |
| CPSCON0 | CPSON | — | — | — | CPSRNG1 | CPSRNG0 | CPSOUT | T0XCS | 0--- 0000 | 0--- 0000 |
| CPSCON1 | — | — | — | — | CPSCH3 | CPSCH2 | CPSCH1 | CPSCH0 | ---- 0000 | ---- 0000 |
| CONFIG2[(1)] | — | — | VCAPEN1 | VCAPEN0 | — | — | — | — | — | — |
| OPTION_REG | $\overline{\text{RBPU}}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| PORTA | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | xxxx xxxx | xxxx xxxx |
| SSPCON | WCOL | SSPOV | SSPEN | CKP | SSPM3 | SSPM2 | SSPM1 | SSPM0 | 0000 0000 | 0000 0000 |
| TRISA | TRISA7 | TRISA6 | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | 1111 1111 | 1111 1111 |

**Legend:** x = unknown, u = unchanged, – = unimplemented locations read as ‘0’. Shaded cells are not used by PORTA.

**Note 1:** PIC16F72X only.

### 6.6.1 RE0/AN5[1]

Figure 6-22 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC

**Note 1:** RE0/AN5 is available on PIC16F724/LF724 and PIC16F727/LF727 only.

### 6.6.2 RE1/AN6[1]

Figure 6-22 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC

**Note 1:** RE0/AN5 is available on PIC16F724/LF724 and PIC16F727/LF727 only.

### 6.6.3 RE2/AN7[1]

Figure 6-22 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC

**Note 1:** RE0/AN5 is available on PIC16F724/LF724 and PIC16F727/LF727 only.

### 6.6.4 RE3/$\overline{\text{MCLR}}$/VPP

Figure 6-23 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose input
- as Master Clear Reset with weak pull-up
- a programming voltage reference input

## 7.2 Clock Source Modes

Clock source modes can be classified as external or internal.

- Internal clock source (INTOSC) is contained within the oscillator module and derived from a 500 kHz high precision oscillator. The oscillator module has eight selectable output frequencies, with a maximum internal frequency of 16 MHz.
- External clock modes rely on external circuitry for the clock source. Examples are: oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes) and Resistor-Capacitor (RC) mode circuits.

The system clock can be selected between external or internal clock sources via the FOSC bits of the Configuration Word 1.

## 7.3 Internal Clock Modes

The oscillator module has eight output frequencies derived from a 500 kHz high precision oscillator. The IRCF bits of the OSCCON register select the postscaler applied to the clock source dividing the frequency by 1, 2, 4 or 8. Setting the PLLEN bit of the Configuration Word 1 locks the internal clock source to 16 MHz before the postscaler is selected by the IRCF bits. The PLLEN bit must be set or cleared at the time of programming; therefore, only the upper or low four clock source frequencies are selectable in software.

### 7.3.1 INTOSC AND INTOSCIO MODES

The INTOSC and INTOSCIO modes configure the internal oscillators as the system clock source when the device is programmed using the oscillator selection or the FOSC<2:0> bits in the CONFIG1 register. See **Section 8.0 “Device Configuration”** for more information.

In INTOSC mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT outputs the selected internal oscillator frequency divided by 4. The CLKOUT signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements.

In INTOSCIO mode, OSC1/CLKIN and OSC2/CLKOUT are available for general purpose I/O.

### 7.3.2 FREQUENCY SELECT BITS (IRCF)

The output of the 500 kHz INTOSC and 16 MHz INTOSC, with Phase-Locked Loop enabled, connect to a postscaler and multiplexer (see Figure 7-1). The Internal Oscillator Frequency Select bits (IRCF) of the OSCCON register select the frequency output of the internal oscillator. Depending upon the PLLEN bit, one of four frequencies of two frequency sets can be selected via software:

If PLLEN = `1`, frequency selection is as follows:

- 16 MHz
- 8 MHz (default after Reset)
- 4 MHz
- 2 MHz

If PLLEN = `0`, frequency selection is as follows:

- 500 kHz
- 250 kHz (default after Reset)
- 125 kHz
- 62.5 kHz

**Note:** Following any Reset, the IRCF<1:0> bits of the OSCCON register are set to ‘`10`’ and the frequency selection is set to 8 MHz or 250 kHz. The user can modify the IRCF bits to select a different frequency.

There is no start-up delay before a new frequency selected in the IRCF bits takes effect. This is because the old and new frequencies are derived from INTOSC via the postscaler and multiplexer.

Start-up delay specifications are located in the Table 23-2 in **Section 23.0 “Electrical Specifications”**.

### REGISTER 9-2: ADCON1: A/D CONTROL REGISTER 1

| U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | ADCS2 | ADCS1 | ADCS0 | — | — | ADREF1 | ADREF0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **ADCS<2:0>:** A/D Conversion Clock Select bits

`000` = FOSC/2
`001` = FOSC/8
`010` = FOSC/32
`011` = FRC (clock supplied from a dedicated RC oscillator)
`100` = FOSC/4
`101` = FOSC/16
`110` = FOSC/64
`111` = FRC (clock supplied from a dedicated RC oscillator)

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1-0 **ADREF<1:0>:** Voltage Reference Configuration bits

`0x` = VREF is connected to VDD
`10` = VREF is connected to external VREF (RA3/AN3)
`11` = VREF is connected to internal Fixed Voltage Reference

### REGISTER 9-3: ADRES: ADC RESULT REGISTER

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| ADRES7 | ADRES6 | ADRES5 | ADRES4 | ADRES3 | ADRES2 | ADRES1 | ADRES0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-0 **ADRES<7:0>**: ADC Result Register bits
8-bit conversion result.

### REGISTER 11-1: OPTION_REG: OPTION REGISTER

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| $\overline{\text{RBPU}}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 |
| bit 7 | | | | | | | bit 0 |

**Legend:**

| | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **$\overline{\text{RBPU}}$:** PORTB Pull-up Enable bit
`1` = PORTB pull-ups are disabled
`0` = PORTB pull-ups are enabled by individual port latch values

bit 6 **INTEDG:** Interrupt Edge Select bit
`1` = Interrupt on rising edge of INT pin
`0` = Interrupt on falling edge of INT pin

bit 5 **T0CS:** TMR0 Clock Source Select bit
`1` = Transition on T0CKI pin or CPSOSC signal
`0` = Internal instruction cycle clock (FOSC/4)

bit 4 **T0SE:** TMR0 Source Edge Select bit
`1` = Increment on high-to-low transition on T0CKI pin
`0` = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
`1` = Prescaler is assigned to the WDT
`0` = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

| BIT VALUE | TMR0 RATE | WDT RATE |
|---|---|---|
| 000 | 1 : 2 | 1 : 1 |
| 001 | 1 : 4 | 1 : 2 |
| 010 | 1 : 8 | 1 : 4 |
| 011 | 1 : 16 | 1 : 8 |
| 100 | 1 : 32 | 1 : 16 |
| 101 | 1 : 64 | 1 : 32 |
| 110 | 1 : 128 | 1 : 64 |
| 111 | 1 : 256 | 1 : 128 |

### TABLE 11-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| CPSCON0 | CPSON | — | — | — | CPSRNG1 | CPSRNG0 | CPSOUT | T0XCS | `0--- 0000` | `0--- 0000` |
| INTCON | GIE | PEIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | `0000 000x` | `0000 000x` |
| OPTION_REG | $\overline{\text{RBPU}}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | `1111 1111` | `1111 1111` |
| TMR0 | Timer0 Module Register | | | | | | | | `xxxx xxxx` | `uuuu uuuu` |
| TRISA | TRISA7 | TRISA6 | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | `1111 1111` | `1111 1111` |

**Legend:** – = Unimplemented locations, read as ‘`0`’, u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.

### 17.2.5 RECEPTION

When the R/$\overline{W}$ bit of the received address byte is clear, the master will write data to the slave. If an address match occurs, the received address is loaded into the SSPBUF register. An address byte overflow will occur if that loaded address is not read from the SSPBUF before the next complete byte is received.

An SSP interrupt is generated for each data transfer byte. The BF, R/$\overline{W}$ and D/$\overline{A}$ bits of the SSPSTAT register are used to determine the status of the last received byte.

**FIGURE 17-10: $I^2C$ WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)**

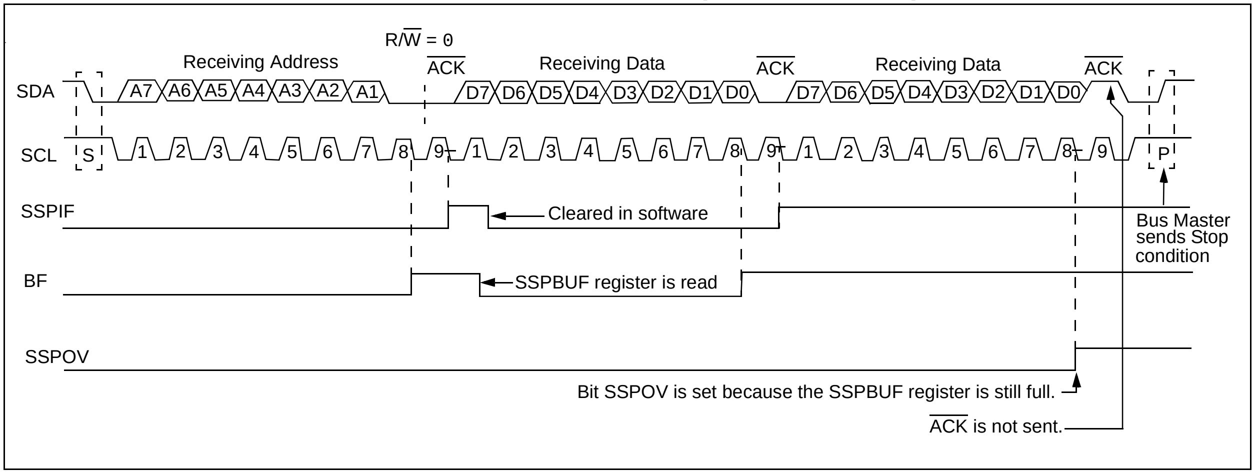
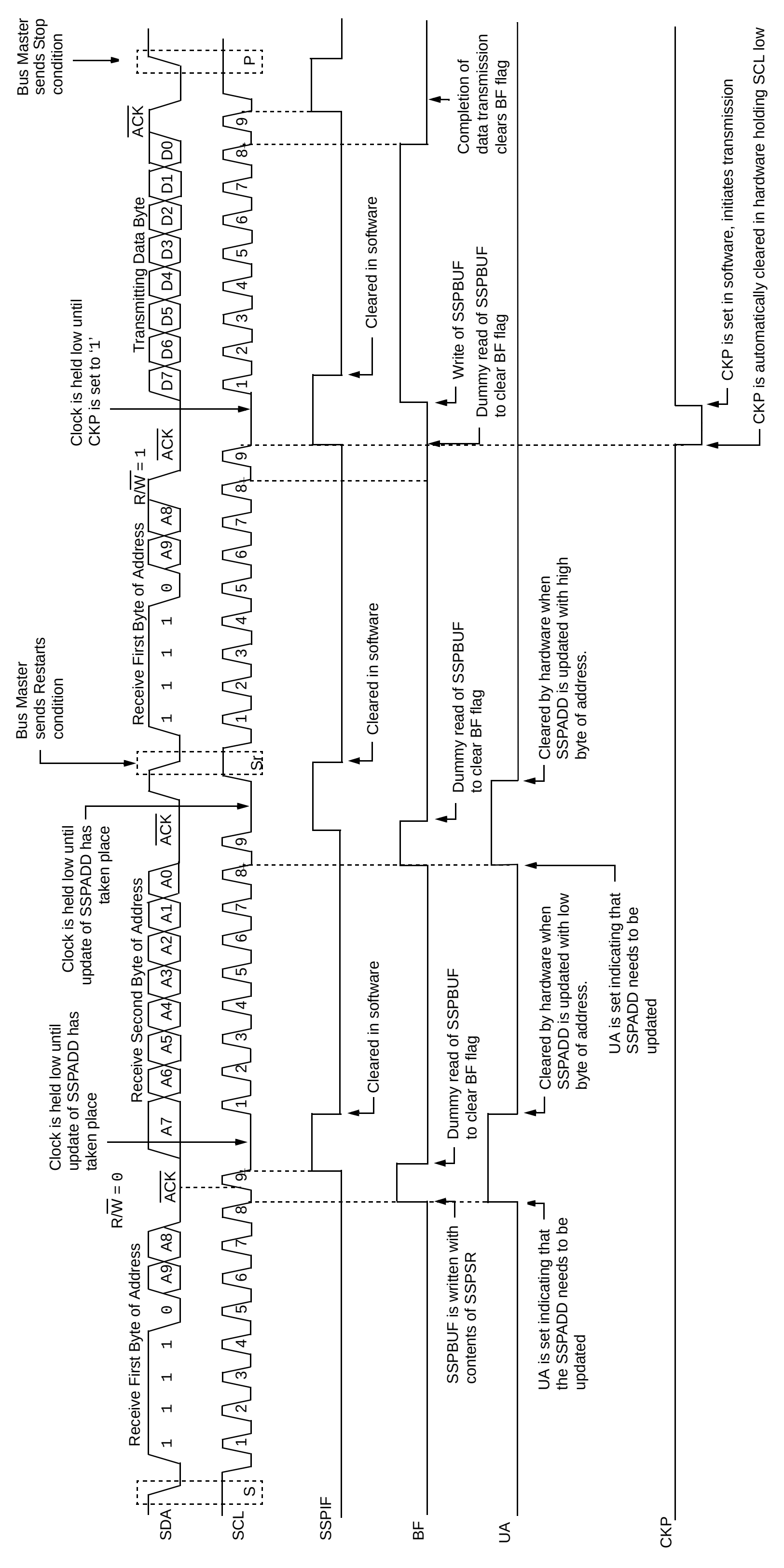

R/$\overline{W}$ = 0
Receiving Address
$\overline{ACK}$
Receiving Data
$\overline{ACK}$
Receiving Data
$\overline{ACK}$
SDA
A7 A6 A5 A4 A3 A2 A1
D7 D6 D5 D4 D3 D2 D1 D0
D7 D6 D5 D4 D3 D2 D1 D0
SCL
S
1 2 3 4 5 6 7 8 9
1 2 3 4 5 6 7 8 9
1 2 3 4 5 6 7 8 9
P
SSPIF
Cleared in software
Bus Master sends Stop condition
BF
SSPBUF register is read
SSPOV
Bit SSPOV is set because the SSPBUF register is still full.
$\overline{ACK}$ is not sent.

**FIGURE 17-13: I²C SLAVE MODE TIMING (TRANSMISSION 10-BIT ADDRESS)**


SDA
SCL
SSPIF
BF
UA
CKP
S
Sr
P
Receive First Byte of Address
1 1 1 1 0 A9 A8
R/W = 0
ACK
Clock is held low until update of SSPADD has taken place
Receive Second Byte of Address
A7 A6 A5 A4 A3 A2 A1 A0
ACK
Clock is held low until update of SSPADD has taken place
Bus Master sends Restarts condition
Receive First Byte of Address
1 1 1 1 0 A9 A8
R/W = 1
ACK
Clock is held low until CKP is set to '1'
Transmitting Data Byte
D7 D6 D5 D4 D3 D2 D1 D0
ACK
Bus Master sends Stop condition
1 2 3 4 5 6 7 8 9
1 2 3 4 5 6 7 8 9
1 2 3 4 5 6 7 8 9
1 2 3 4 5 6 7 8 9
Cleared in software
Cleared in software
Cleared in software
SSPBUF is written with contents of SSPSR
Dummy read of SSPBUF to clear BF flag
Dummy read of SSPBUF to clear BF flag
Write of SSPBUF
Dummy read of SSPBUF to clear BF flag
Completion of data transmission clears BF flag
UA is set indicating that the SSPADD needs to be updated
Cleared by hardware when SSPADD is updated with low byte of address.
UA is set indicating that SSPADD needs to be updated
Cleared by hardware when SSPADD is updated with high byte of address.
CKP is set in software, initiates transmission
CKP is automatically cleared in hardware holding SCL low

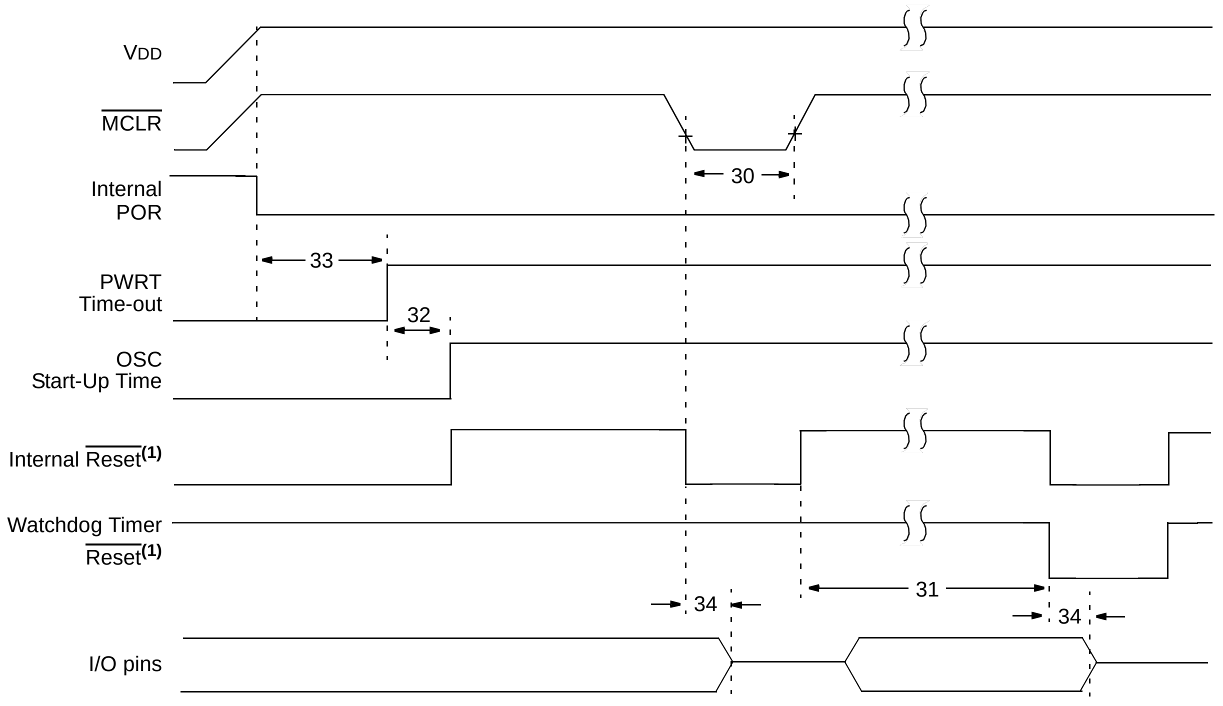
### TABLE 23-3: CLKOUT AND I/O TIMING PARAMETERS

**Standard Operating Conditions (unless otherwise stated)**
Operating Temperature -40°C ≤ TA ≤ +125°C

| Param No. | Sym. | Characteristic | Min. | Typ† | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| OS11 | TosH2ckL | Fosc↑ to CLKOUT↓ (1) | — | — | 70 | ns | VDD = 3.3-5.0V |
| OS12 | TosH2ckH | Fosc↑ to CLKOUT↑ (1) | — | — | 72 | ns | VDD = 3.3-5.0V |
| OS13 | TckL2ioV | CLKOUT↓ to Port out valid(1) | — | — | 20 | ns | |
| OS14 | TioV2ckH | Port input valid before CLKOUT↑(1) | TOSC + 200 ns | — | — | ns | |
| OS15 | TosH2ioV | Fosc↑ (Q1 cycle) to Port out valid | — | 50 | 70* | ns | VDD = 3.3-5.0V |
| OS16 | TosH2ioI | Fosc↑ (Q2 cycle) to Port input invalid (I/O in hold time) | 50 | — | — | ns | VDD = 3.3-5.0V |
| OS17 | TioV2osH | Port input valid to Fosc↑ (Q2 cycle) (I/O in setup time) | 20 | — | — | ns | |
| OS18 | TioR | Port output rise time(2) | —<br>— | 40<br>15 | 72<br>32 | ns | VDD = 2.0V<br>VDD = 3.3-5.0V |
| OS19 | TioF | Port output fall time(2) | —<br>— | 28<br>15 | 55<br>30 | ns | VDD = 2.0V<br>VDD = 3.3-5.0V |
| OS20* | Tinp | INT pin input high or low time | 25 | — | — | ns | |
| OS21* | Trbp | PORTB interrupt-on-change new input level time | TCY | — | — | ns | |

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated.
**Note 1:** Measurements are taken in RC mode where CLKOUT output is 4 x TOSC.
**2:** Includes OSC2 in CLKOUT mode.

FIGURE 23-8: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



**Note 1:** Asserted low.

**FIGURE 24-7: PIC16F722/3/4/6/7 TYPICAL IDD vs. VDD OVER FOSC, EXTRC MODE, VCAP = 0.1 µF**

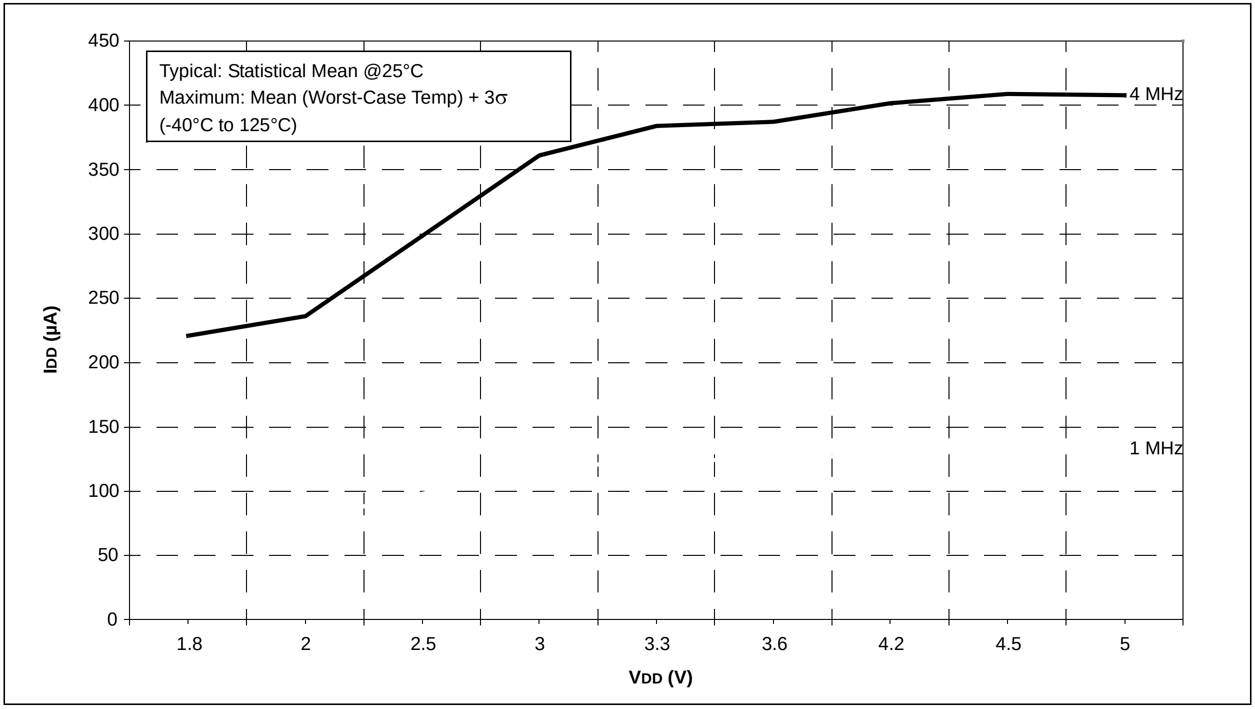


**FIGURE 24-8: PIC16LF722/3/4/6/7 TYPICAL IDD vs. VDD OVER FOSC, EXTRC MODE**

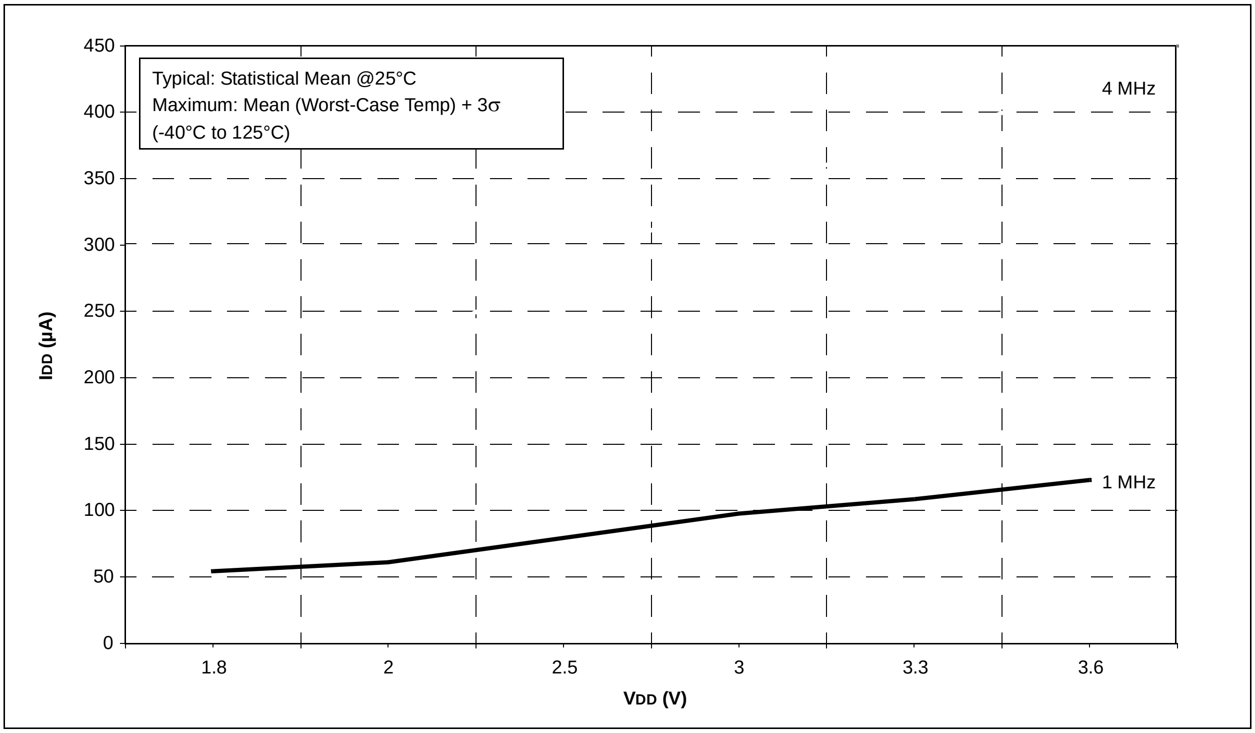


**FIGURE 24-11: PIC16F722/3/4/6/7 TYPICAL $I_{DD}$ vs. $F_{OSC}$ OVER $V_{DD}$, HS MODE, $V_{CAP}$ = 0.1 µF**

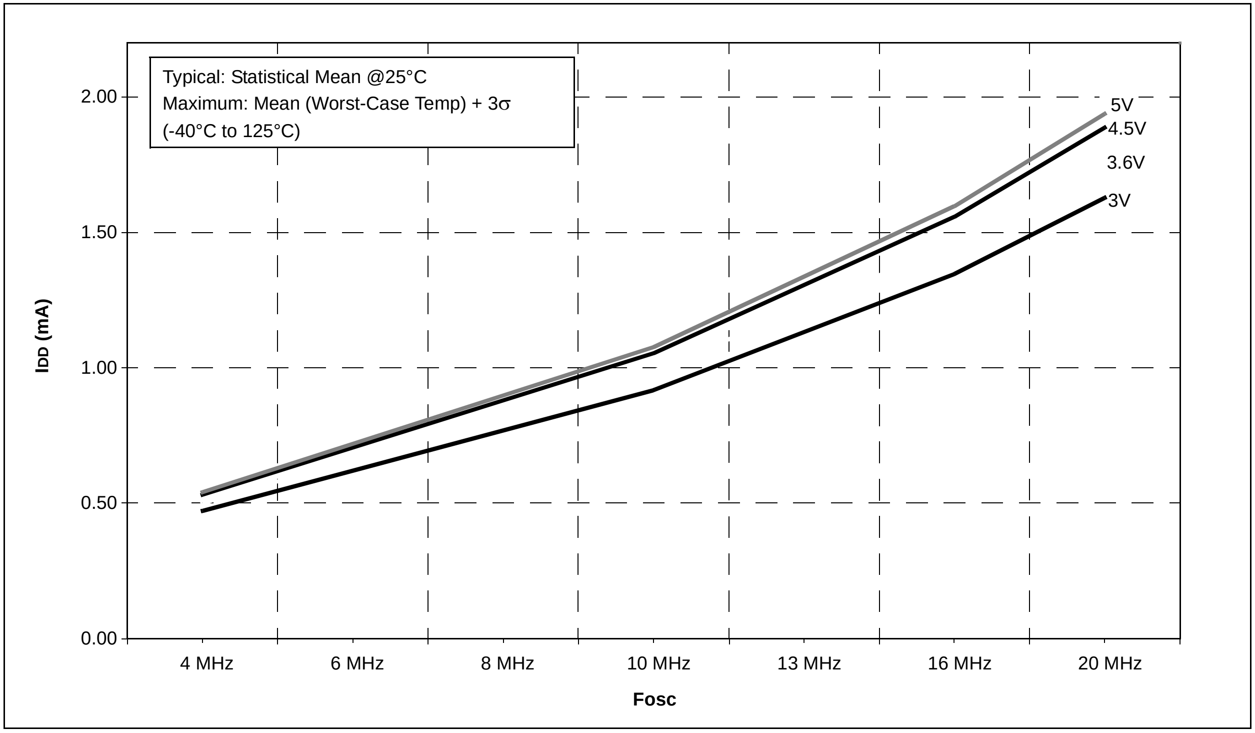


**FIGURE 24-12: PIC16LF722/3/4/6/7 TYPICAL $I_{DD}$ vs. $F_{OSC}$ OVER $V_{DD}$, HS MODE**

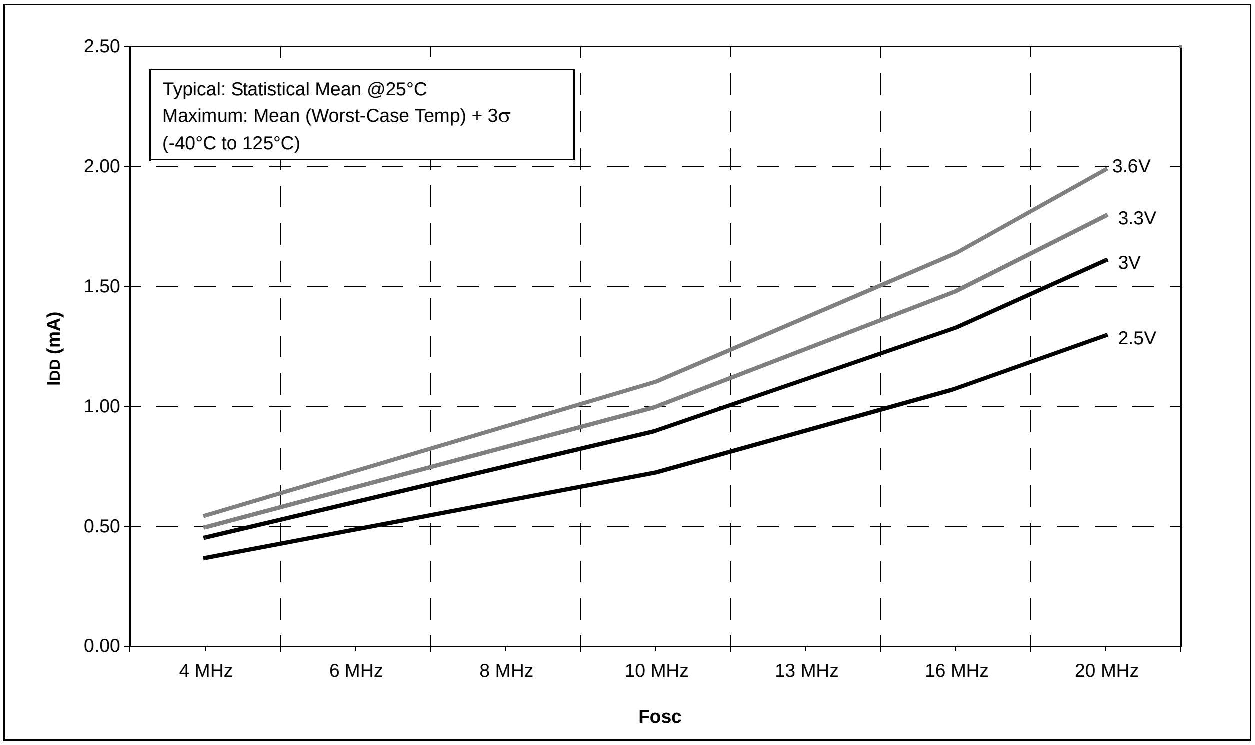


**FIGURE 24-29: PIC16F722/3/4/6/7 TYPICAL BASE IPD VS. VDD, VCAP = 0.1 µF**

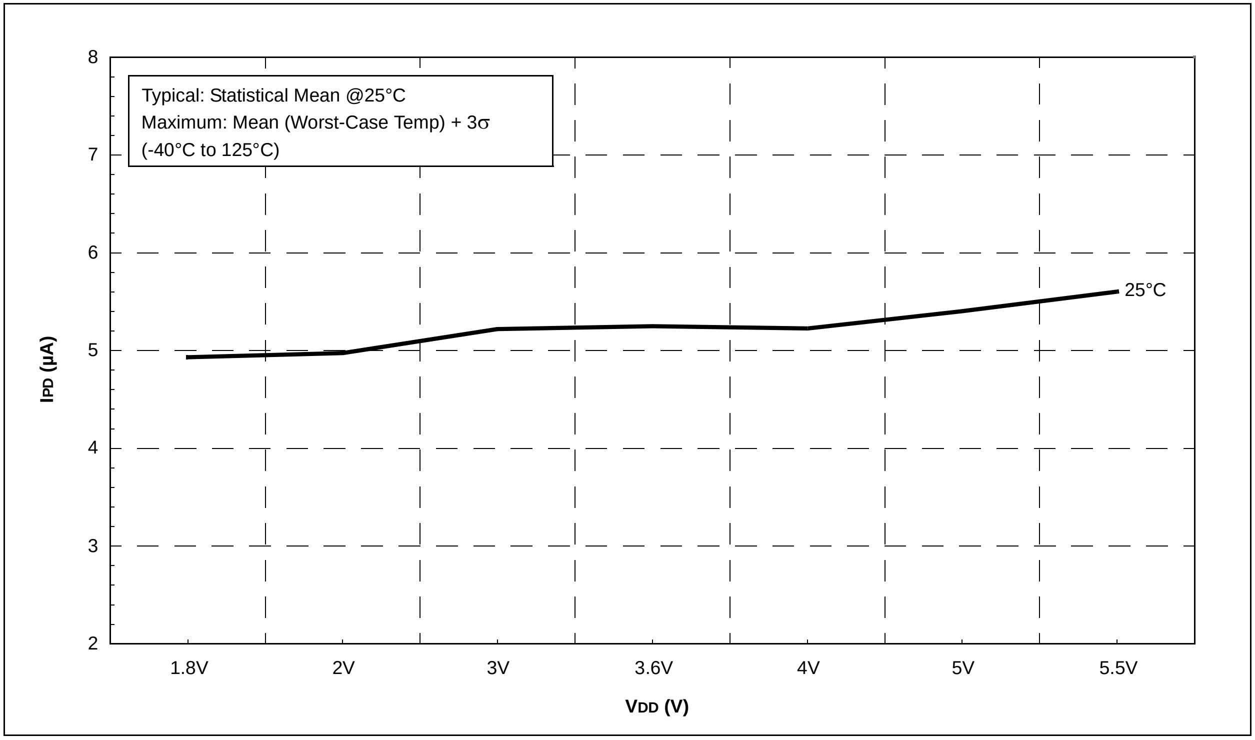


**FIGURE 24-30: PIC16LF722/3/4/6/7 TYPICAL BASE IPD VS. VDD**

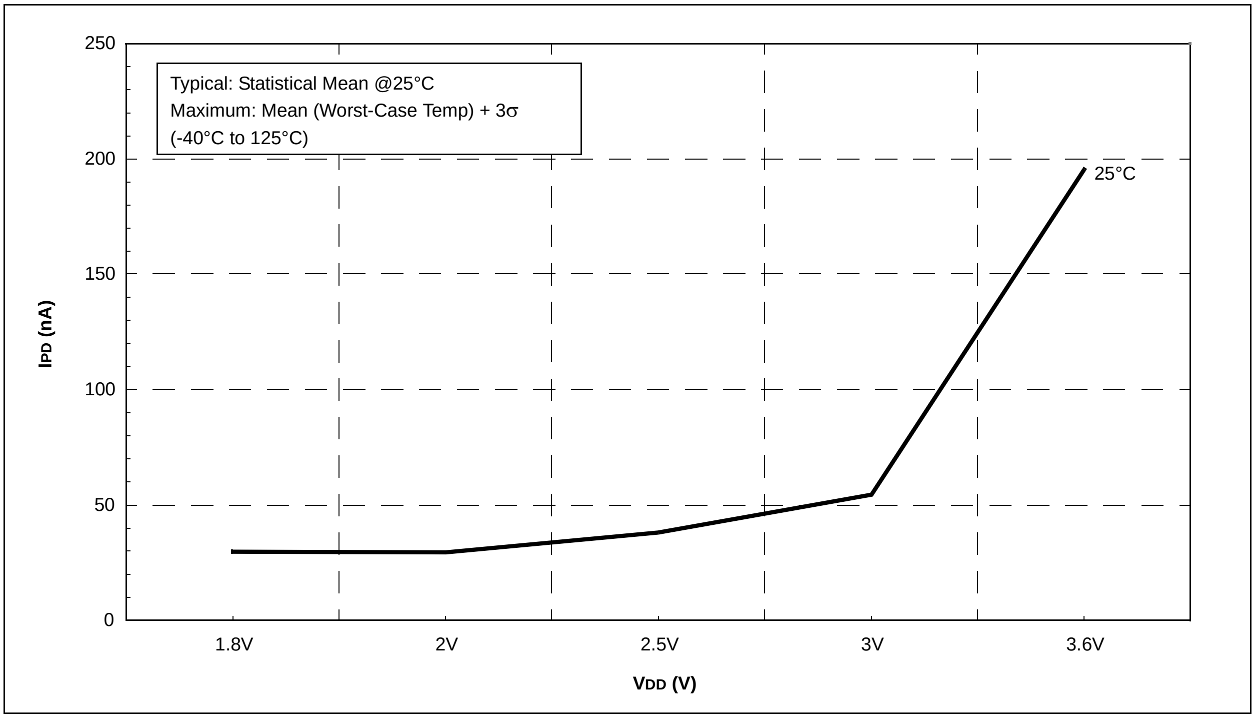


**FIGURE 24-33:** PIC16F722/3/4/6/7 BOR IPD vs. VDD, VCAP = 0.1 µF

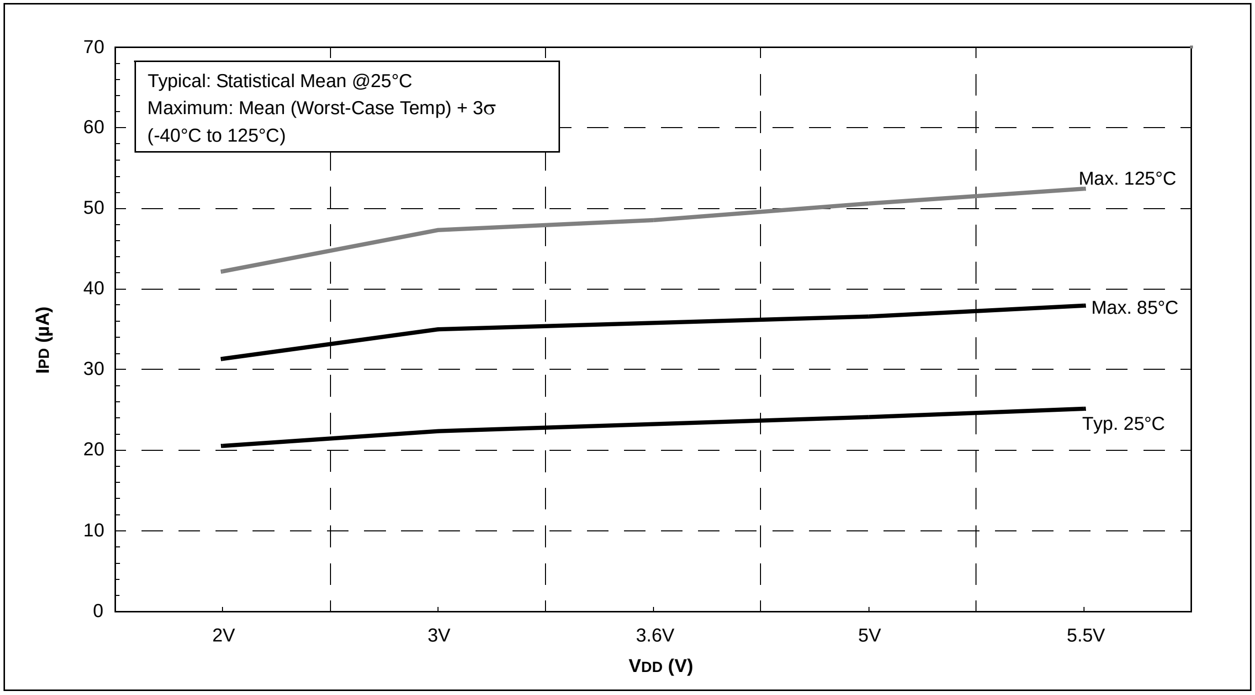


**FIGURE 24-34:** PIC16LF722/3/4/6/7 BOR IPD vs. VDD

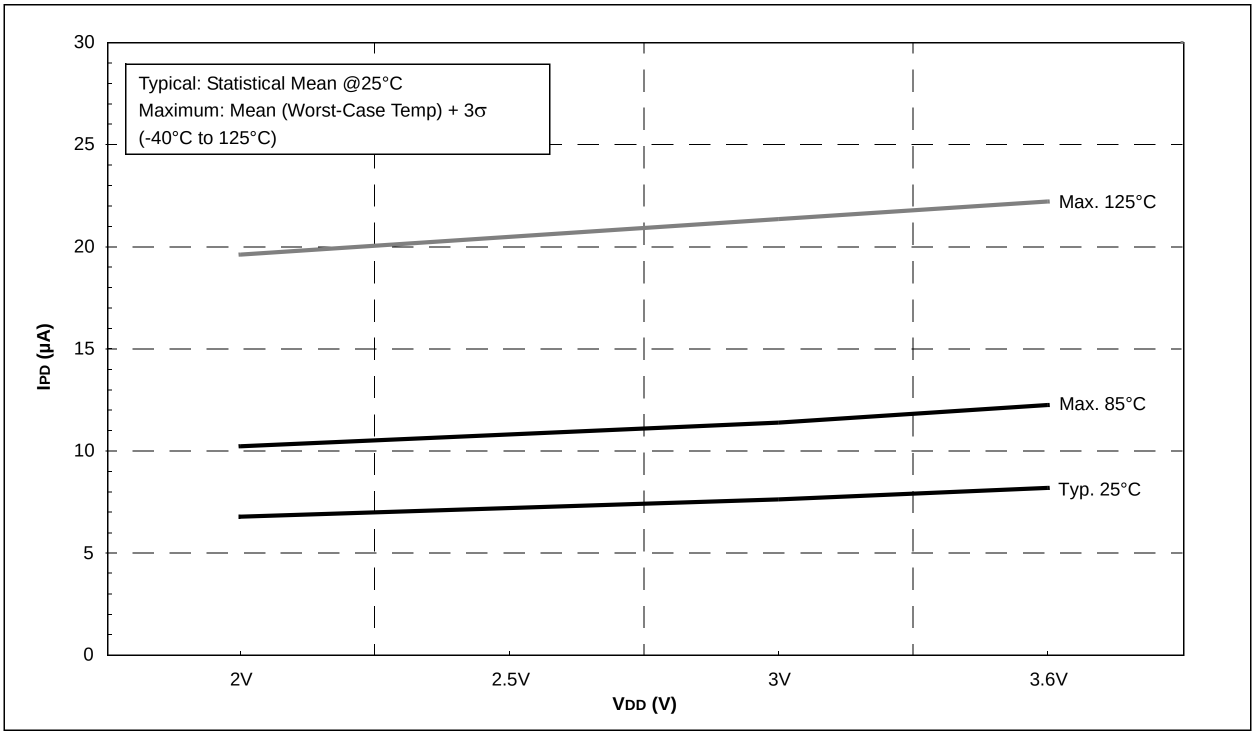


**FIGURE 24-49: TTL INPUT THRESHOLD $V_{IN}$ vs. $V_{DD}$ OVER TEMPERATURE**

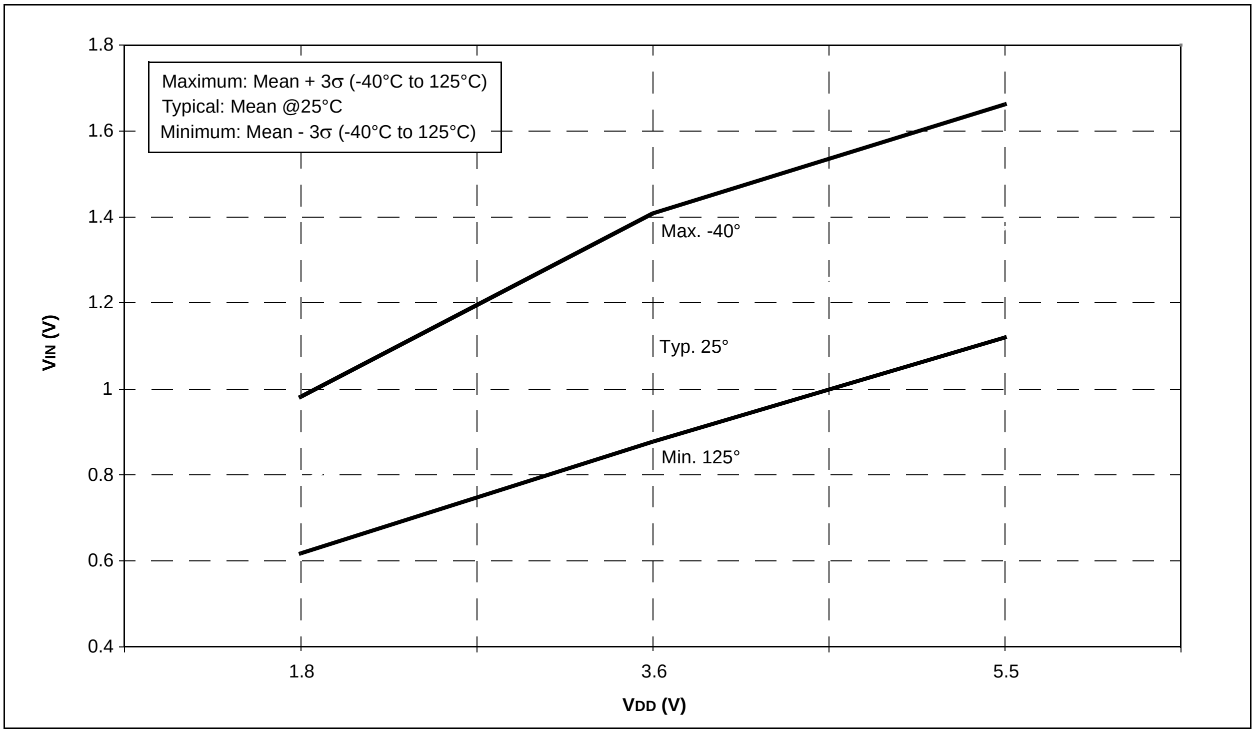


**FIGURE 24-50: SCHMITT TRIGGER INPUT THRESHOLD $V_{IN}$ vs. $V_{DD}$ OVER TEMPERATURE**

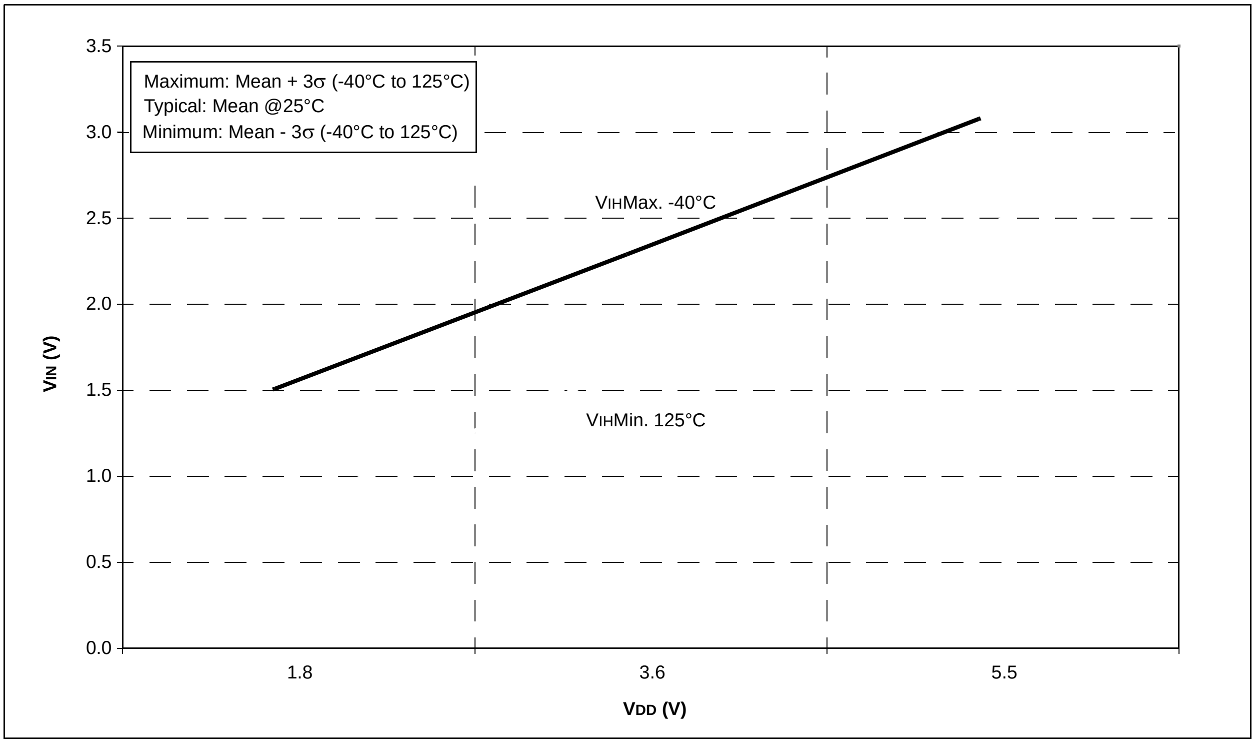


**FIGURE 24-53: VOH vs. IOH OVER TEMPERATURE, VDD = 3.6V**

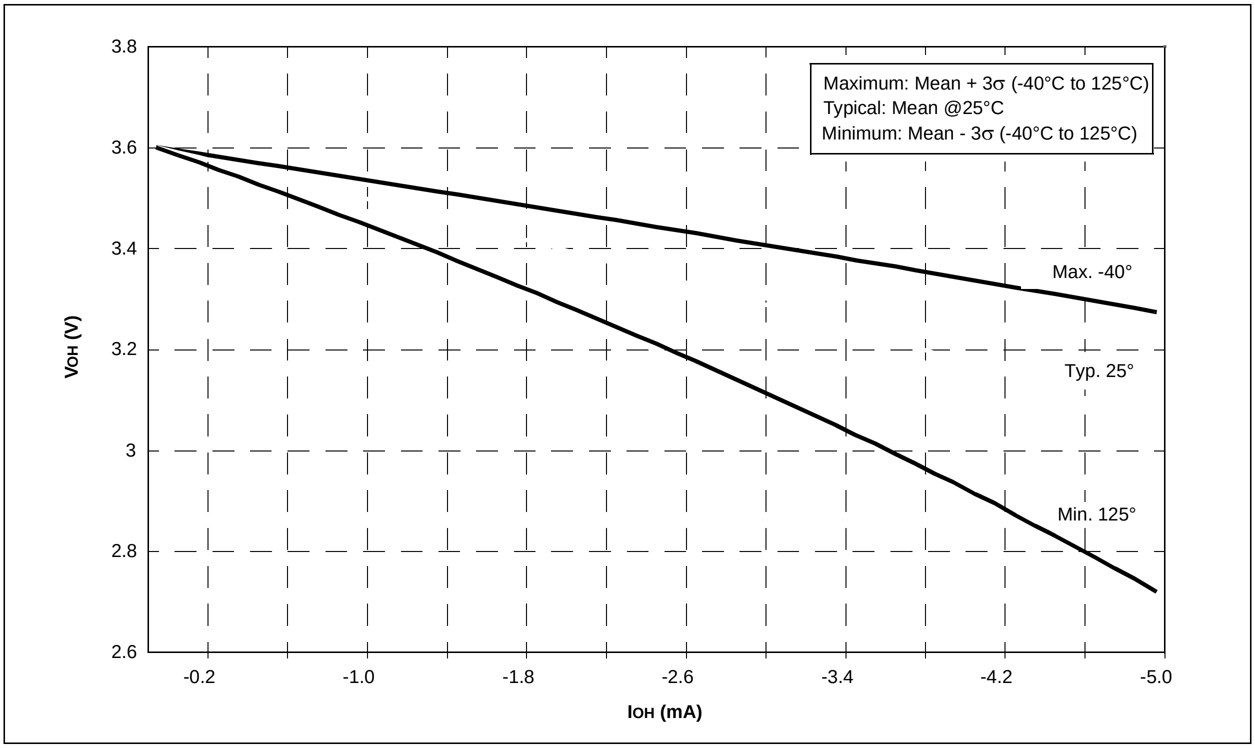


**FIGURE 24-54: VOH vs. IOH OVER TEMPERATURE, VDD = 1.8V**

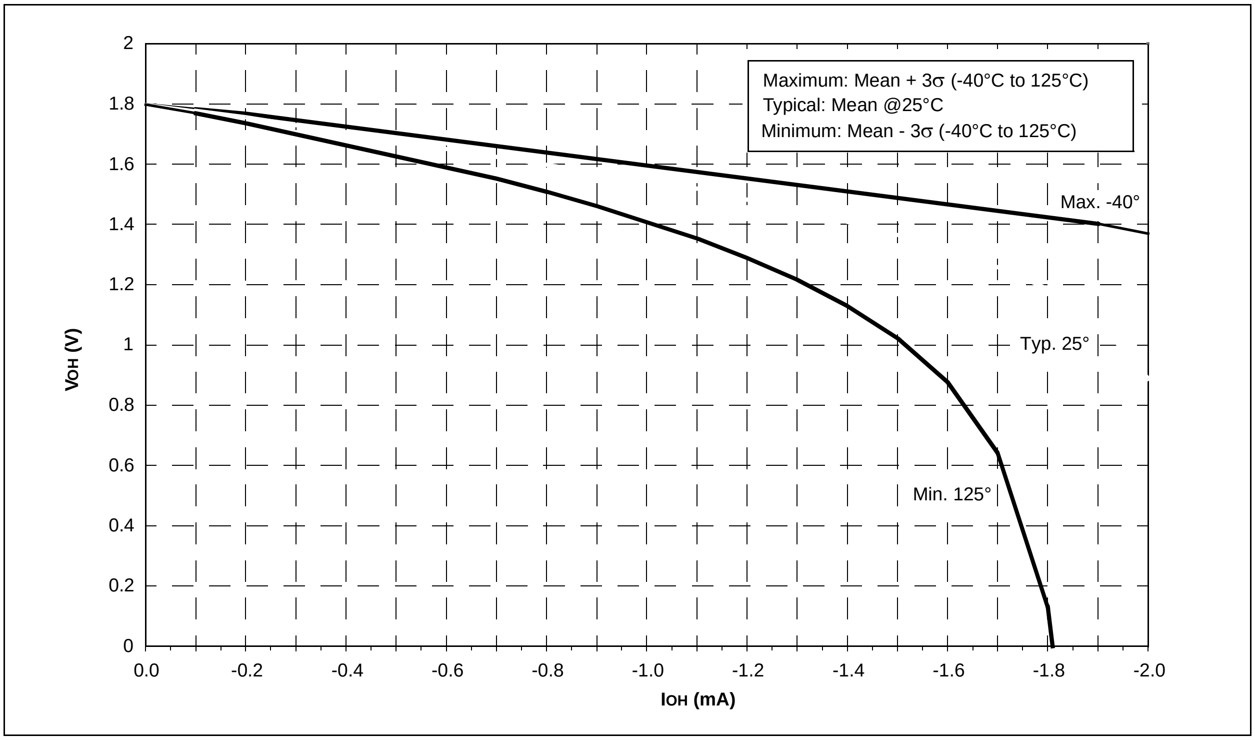


**FIGURE 24-63: PIC16F722/3/4/6/7 CAP SENSE OUTPUT CURRENT, POWER MODE = MEDIUM**

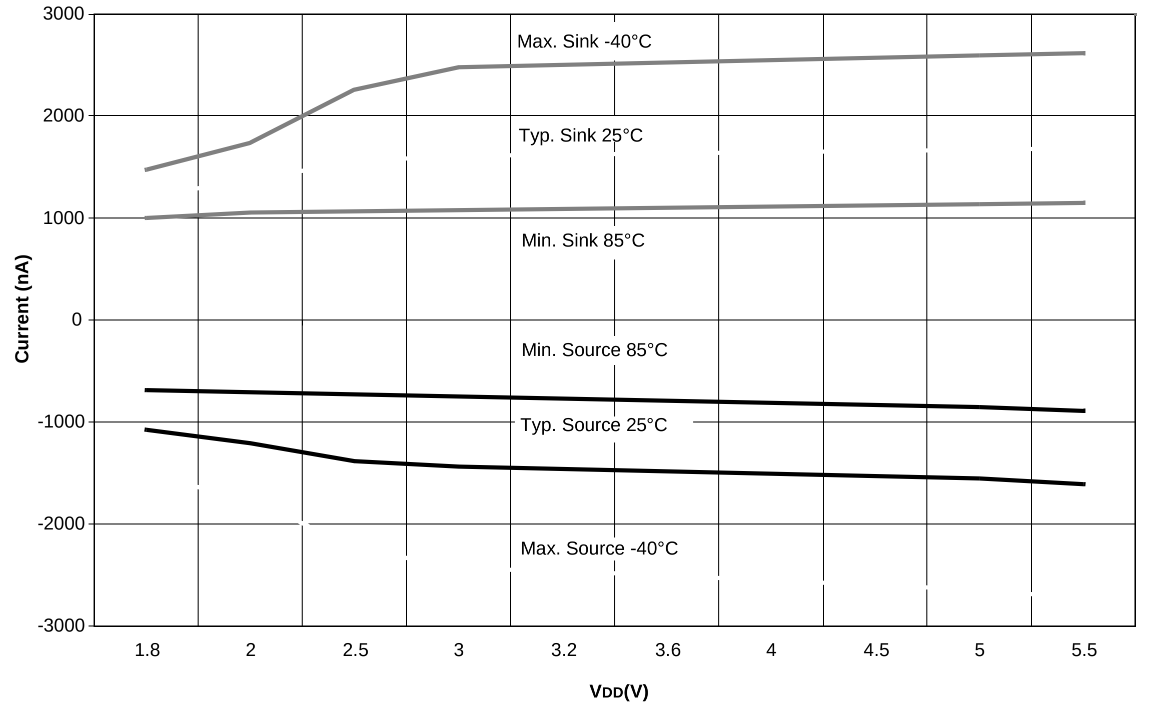


**FIGURE 24-64: PIC16F722/3/4/6/7 CAP SENSE OUTPUT CURRENT, POWER MODE = LOW**

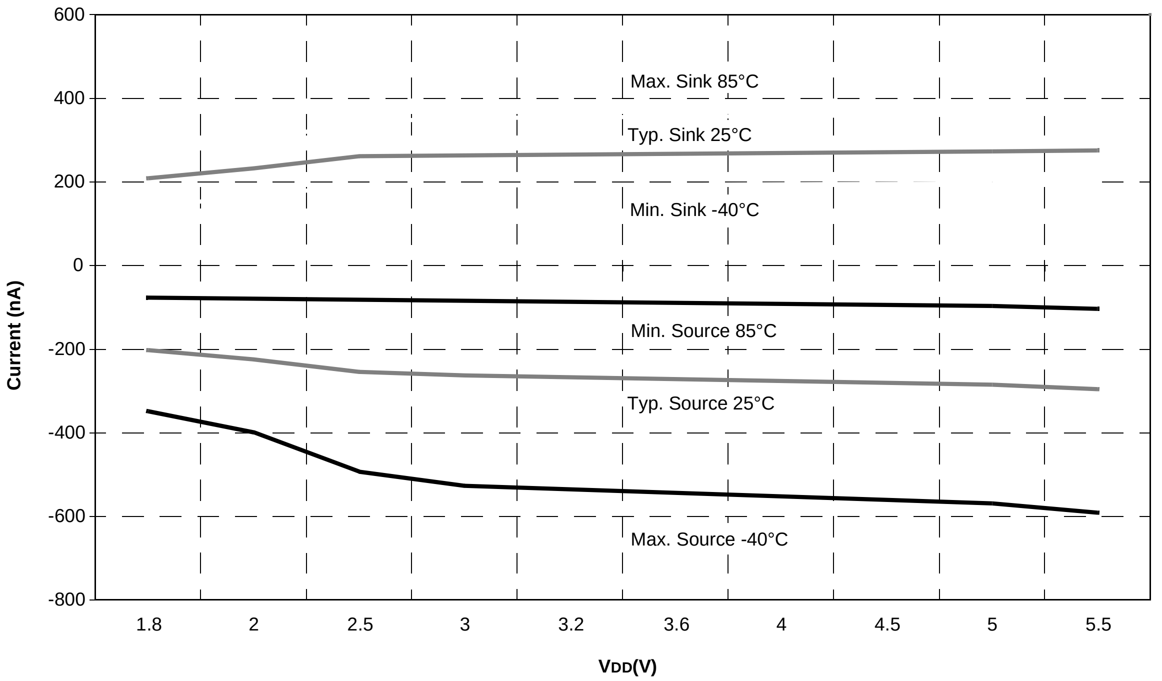
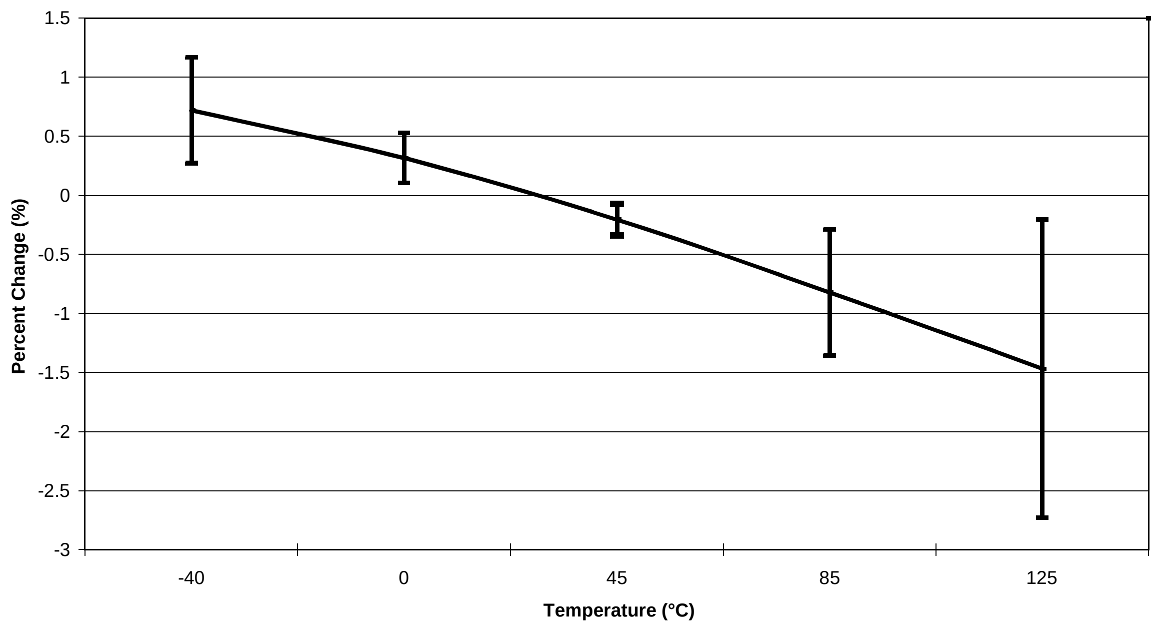


**FIGURE 24-69: TYPICAL FVR CHANGE VS. TEMPERATURE NORMALIZED AT 25°C**



## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | [X](1) | X | /XX | XXX |
|---|---|---|---|---|
| Device | Tape and Reel Option | Temperature Range | Package | Pattern |

**Device:** PIC16F722, PIC16LF722, PIC16F722T, PIC16LF722T(1)
PIC16F723, PIC16LF723, PIC16F723T, PIC16LF723T(1)
PIC16F724, PIC16LF724, PIC16F724T, PIC16LF724T(1)
PIC16F726, PIC16LF726, PIC16F726T, PIC16LF726T(1)
PIC16F727, PIC16LF727, PIC16F727T, PIC16LF727T(1)

**Tape and Reel Option:**
I = -40°C to +85°C
E = -40°C to +125°C
MV = Micro Lead Frame (UQFN)

**Temperature Range:**
I = -40°C to +85°C (Industrial)
E = -40°C to +125°C (Extended)

**Package:**
ML = Micro Lead Frame (QFN)
P = Plastic DIP
PT = TQFP (Thin Quad Flatpack)
SO = SOIC
SP = Skinny Plastic DIP
SS = SSOP

**Examples:**

a) PIC16F722-E/SP 301 = Extended Temp., skinny PDIP package, QTP pattern #301

b) PIC16F722-I/SO = Industrial Temp., SOIC package

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.