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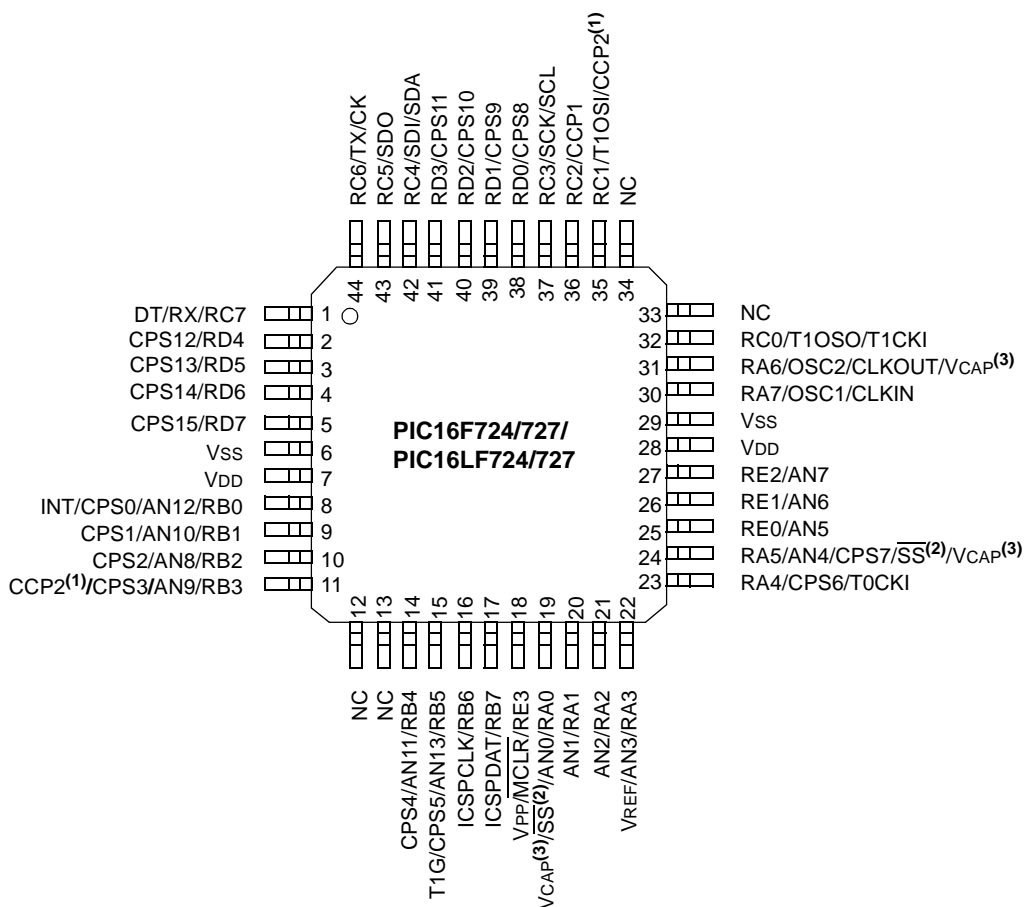
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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 14x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f727-e-pt

PIC16(L)F722/3/4/6/7

Pin Diagrams – 44-PIN TQFP (PIC16F724/727/PIC16LF724/727)



Note 1: CCP2 pin location may be selected as RB3 or RC1.

2: SS pin location may be selected as RA5 or RA0.

3: PIC16F724/727 devices only.

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PIC16(L)F722/3/4/6/7

TABLE 2-1: PIC16(L)F722/3/4/6/7 SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Page
Bank 1											
80h ⁽²⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	29,37
81h	OPTION_REG	RBP _U	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	26,37
82h ⁽²⁾	PCL	Program Counter (PC) Least Significant Byte								0000 0000	28,37
83h ⁽²⁾	STATUS	IRP	RP1	RP0	\overline{TO}	\overline{PD}	Z	DC	C	0001 1xxx	25,37
84h ⁽²⁾	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	29,37
85h	TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111	51,37
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	60,37
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	70,37
88h ⁽³⁾	TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	1111 1111	78,37
89h	TRISE	—	—	—	—	TRISE3 ⁽⁶⁾	TRISE2 ⁽³⁾	TRISE1 ⁽³⁾	TRISE0 ⁽³⁾	---- 1111	81,37
8Ah ^(1, 2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	28,37
8Bh ⁽²⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	44,37
8Ch	PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	45,37
8Dh	PIE2	—	—	—	—	—	—	—	CCP2IE	---- --0	46,37
8Eh	PCON	—	—	—	—	—	—	\overline{POR}	\overline{BOR}	---- --qq	27,38
8Fh	T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/ DONE	T1GVAL	T1GSS1	T1GSS0	0000 0x00	118,38
90h	OSCCON	—	—	IRCF1	IRCF0	ICSL	ICSS	—	—	--10 qq--	87,38
91h	OSCTUNE	—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0	--00 0000	88,38
92h	PR2	Timer2 Period Register								1111 1111	120,38
93h	SSPAD ⁽⁵⁾	Synchronous Serial Port (I ² C mode) Address Register								0000 0000	169,38
93h	SSPMASK ⁽⁴⁾	Synchronous Serial Port (I ² C mode) Address Mask Register								1111 1111	180,38
94h	SSPSTAT	SMP	CKE	D/ \overline{A}	P	S	R/ \overline{W}	UA	BF	0000 0000	179,38
95h	WPUB	WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0	1111 1111	61,38
96h	IOCB	IOCB7	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0	0000 0000	61,38
97h	—	Unimplemented								—	—
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	147,38
99h	SPBRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	0000 0000	149,38
9Ah	—	Unimplemented								—	—
9Bh	—	Unimplemented								—	—
9Ch	APFCON	—	—	—	—	—	—	SSSEL	CCP2SEL	---- --00	50,38
9Dh	FVRCON	FVRRDY	FVREN	—	—	—	—	ADFVR1	ADFVR0	q0-- --00	104,38
9Eh	—	Unimplemented								—	—
9Fh	ADCON1	—	ADCS2	ADCS1	ADCS0	—	—	ADREF1	ADREF0	0000 --00	100,38

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.

Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter.

2: These registers can be addressed from any bank.

3: These registers/bits are not implemented on PIC16F722/723/726/PIC16LF722/723/726 devices, read as '0'.

4: Accessible only when SSPM<3:0> = 1001.

5: Accessible only when SSPM<3:0> ≠ 1001.

6: This bit is always '1' as RE3 is input-only.

--

6.4.1 RC0/T1OSO/T1CKI

Figure 6-13 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- a Timer1 oscillator output
- a Timer1 clock input

6.4.2 RC1/T1OSI/CCP2

Figure 6-14 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- a Timer1 oscillator input
- a Capture 2 input, Compare 2 output, and PWM2 output

Note: CCP2 pin location may be selected as RB3 or RC1.

6.4.3 RC2/CCP1

Figure 6-15 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- a Capture 1 input, Compare 1 output, and PWM1 output

6.4.4 RC3/SCK/SCL

Figure 6-16 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- a SPI clock
- an I²C clock

6.4.5 RC4/SDI/SDA

Figure 6-17 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- a SPI data input
- an I²C data I/O

6.4.6 RC5/SDO

Figure 6-18 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- a SPI data output

6.4.7 RC6/TX/CK

Figure 6-19 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an asynchronous serial output
- a synchronous clock I/O

6.4.8 RC7/RX/DT

Figure 6-20 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an asynchronous serial input
- a synchronous serial data I/O

7.6 External Clock Modes

7.6.1 OSCILLATOR START-UP TIMER (OST)

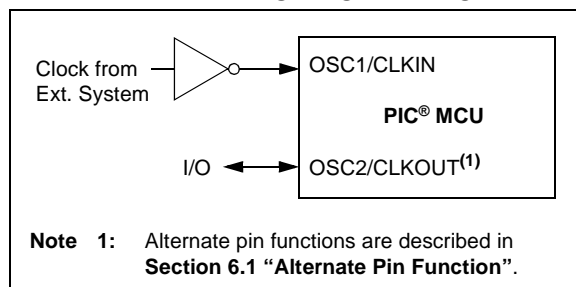
If the oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations on the OSC1 pin before the device is released from Reset. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the oscillator module.

7.6.2 EC MODE

The External Clock (EC) mode allows an externally generated logic level as the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input and the OSC2 is available for general purpose I/O. Figure 7-2 shows the pin connections for EC mode.

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 7-2: EXTERNAL CLOCK (EC) MODE OPERATION



7.6.3 LP, XT, HS MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 7-3). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

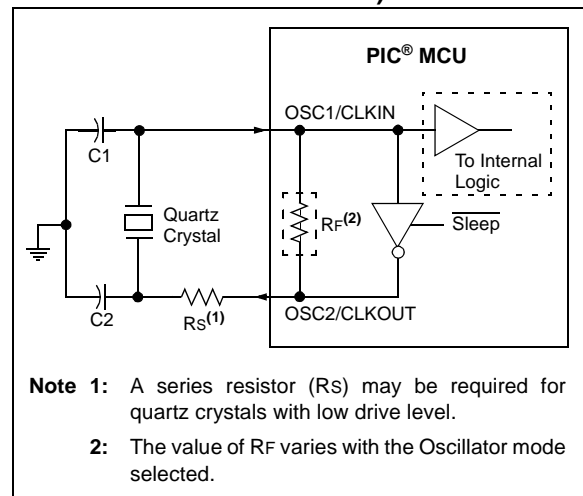
LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is best suited to drive resonators with a low drive level specification, for example, tuning fork type crystals.

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 7-3 and Figure 7-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

FIGURE 7-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)



Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

2: Always verify oscillator performance over the V_{DD} and temperature range that is expected for the application.

3: For oscillator design assistance, reference the following Microchip Applications Notes:

- AN826, *Crystal Oscillator Basics and Crystal Selection for $rPIC^{\circ}$ and PIC° Devices* (DS00826)
- AN849, *Basic PIC° Oscillator Design* (DS00849)
- AN943, *Practical PIC° Oscillator Analysis and Design* (DS00943)
- AN949, *Making Your Oscillator Work* (DS00949).

PIC16(L)F722/3/4/6/7

TABLE 9-1: ADC CLOCK PERIOD (T_{AD}) Vs. DEVICE OPERATING FREQUENCIES

ADC Clock Period (T _{AD})		Device Frequency (F _{osc})				
ADC Clock Source	ADCS<2:0>	20 MHz	16 MHz	8 MHz	4 MHz	1 MHz
Fosc/2	000	100 ns ⁽²⁾	125 ns ⁽²⁾	250 ns ⁽²⁾	500 ns ⁽²⁾	2.0 μs
Fosc/4	100	200 ns ⁽²⁾	250 ns ⁽²⁾	500 ns ⁽²⁾	1.0 μs	4.0 μs
Fosc/8	001	400 ns ⁽²⁾	0.5 μs ⁽²⁾	1.0 μs	2.0 μs	8.0 μs ⁽³⁾
Fosc/16	101	800 ns	1.0 μs	2.0 μs	4.0 μs	16.0 μs ⁽³⁾
Fosc/32	010	1.6 μs	2.0 μs	4.0 μs	8.0 μs ⁽³⁾	32.0 μs ⁽³⁾
Fosc/64	110	3.2 μs	4.0 μs	8.0 μs ⁽³⁾	16.0 μs ⁽³⁾	64.0 μs ⁽³⁾
FRC	x11	1.0-6.0 μs ^(1,4)	1.0-6.0 μs ^(1,4)	1.0-6.0 μs ^(1,4)	1.0-6.0 μs ^(1,4)	1.0-6.0 μs ^(1,4)

Legend: Shaded cells are outside of recommended range.

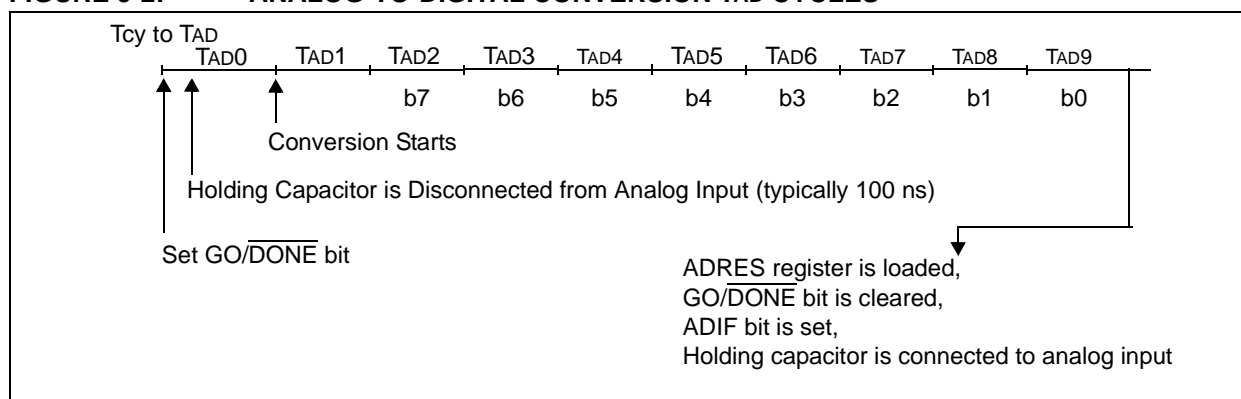
Note 1: The FRC source has a typical T_{AD} time of 1.6 μs for V_{DD}.

2: These values violate the minimum required T_{AD} time.

3: For faster conversion times, the selection of another clock source is recommended.

4: When the device frequency is greater than 1 MHz, the FRC clock source is only recommended if the conversion will be performed during Sleep.

FIGURE 9-2: ANALOG-TO-DIGITAL CONVERSION T_{AD} CYCLES



PIC16(L)F722/3/4/6/7

11.1.3 SOFTWARE PROGRAMMABLE PRESCALER

A single software programmable prescaler is available for use with either Timer0 or the Watchdog Timer (WDT), but not both simultaneously. The prescaler assignment is controlled by the PSA bit of the OPTION register. To assign the prescaler to Timer0, the PSA bit must be cleared to a '0'.

There are eight prescaler options for the Timer0 module ranging from 1:2 to 1:256. The prescale values are selectable via the PS<2:0> bits of the OPTION register. In order to have a 1:1 prescaler value for the Timer0 module, the prescaler must be assigned to the WDT module.

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register will clear the prescaler.

Note: When the prescaler is assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT.

11.1.4 TIMER0 INTERRUPT

Timer0 will generate an interrupt when the TMR0 register overflows from FFh to 00h. The T0IF interrupt flag bit of the INTCON register is set every time the TMR0 register overflows, regardless of whether or not the Timer0 interrupt is enabled. The T0IF bit can only be cleared in software. The Timer0 interrupt enable is the T0IE bit of the INTCON register.

Note: The Timer0 interrupt cannot wake the processor from Sleep since the timer is frozen during Sleep.
--

11.1.5 8-BIT COUNTER MODE SYNCHRONIZATION

When in 8-Bit Counter mode, the incrementing edge on the T0CKI pin must be synchronized to the instruction clock. Synchronization can be accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the instruction clock. The high and low periods of the external clocking source must meet the timing requirements as shown in **Section 23.0 “Electrical Specifications”**.

PIC16(L)F722/3/4/6/7

TABLE 16-2: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
RCREG	AUSART Receive Data Register								0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SPBRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	0000 0000	0000 0000
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Asynchronous Reception.

16.4 AUSART Operation During Sleep

The AUSART will remain active during Sleep only in the Synchronous Slave mode. All other modes require the system clock and therefore cannot generate the necessary signals to run the Transmit or Receive Shift registers during Sleep.

Synchronous Slave mode uses an externally generated clock to run the Transmit and Receive Shift registers.

16.4.1 SYNCHRONOUS RECEIVE DURING SLEEP

To receive during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for Synchronous Slave Reception (refer to **Section 16.3.2.4 “Synchronous Slave Reception Setup:”**).
- If interrupts are desired, set the RCIE bit of the PIE1 register and the PEIE bit of the INTCON register.
- The RCIF interrupt flag must be cleared by reading RCREG to unload any pending characters in the receive buffer.

Upon entering Sleep mode, the device will be ready to accept data and clocks on the RX/DT and TX/CK pins, respectively. When the data word has been completely clocked in by the external device, the RCIF interrupt flag bit of the PIR1 register will be set. Thereby, waking the processor from Sleep.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the GIE global interrupt enable bit of the INTCON register is also set, then the Interrupt Service Routine at address 0004h will be called.

16.4.2 SYNCHRONOUS TRANSMIT DURING SLEEP

To transmit during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for Synchronous Slave Transmission (refer to **Section 16.3.2.2 “Synchronous Slave Transmission Setup:”**).
- The TXIF interrupt flag must be cleared by writing the output data to the TXREG, thereby filling the TSR and transmit buffer.
- If interrupts are desired, set the TXIE bit of the PIE1 register and the PEIE bit of the INTCON register.

Upon entering Sleep mode, the device will be ready to accept clocks on TX/CK pin and transmit data on the RX/DT pin. When the data word in the TSR has been completely clocked out by the external device, the pending byte in the TXREG will transfer to the TSR and the TXIF flag will be set. Thereby, waking the processor from Sleep. At this point, the TXREG is available to accept another character for transmission, which will clear the TXIF flag.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the GIE global interrupt enable bit is also set then the Interrupt Service Routine at address 0004h will be called.

PIC16(L)F722/3/4/6/7

FIGURE 17-4: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 0)

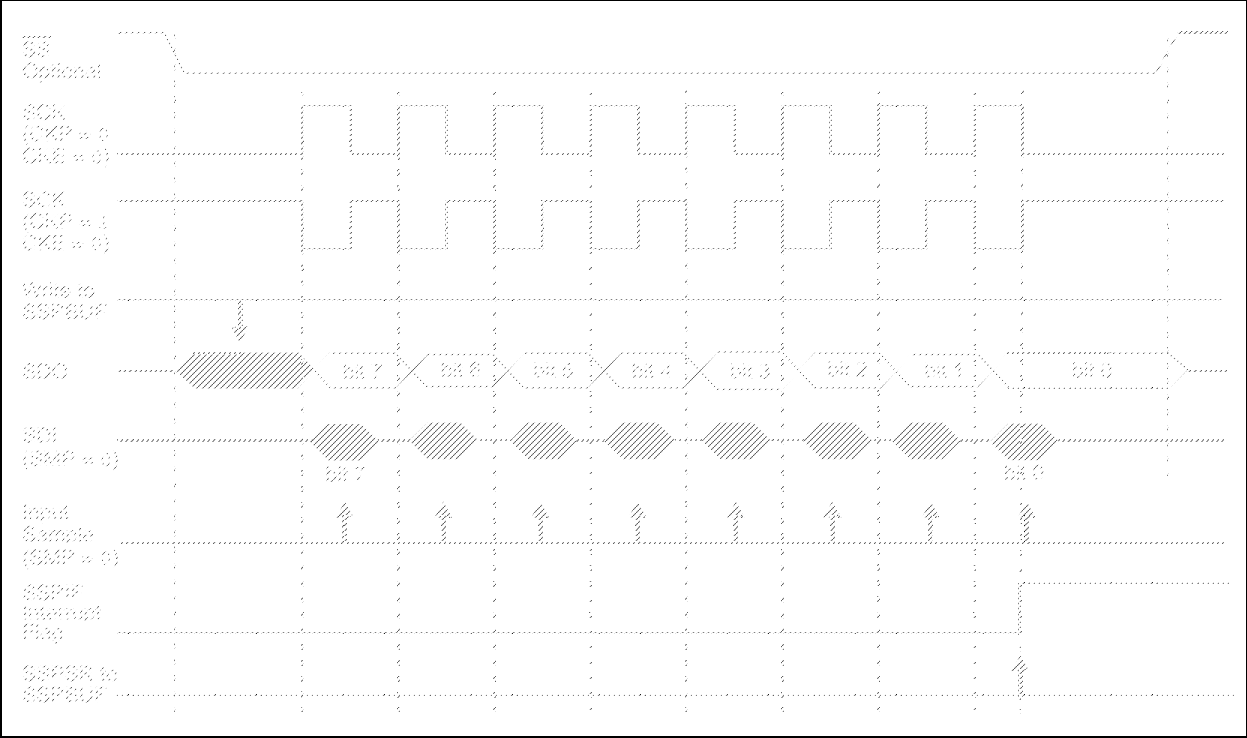
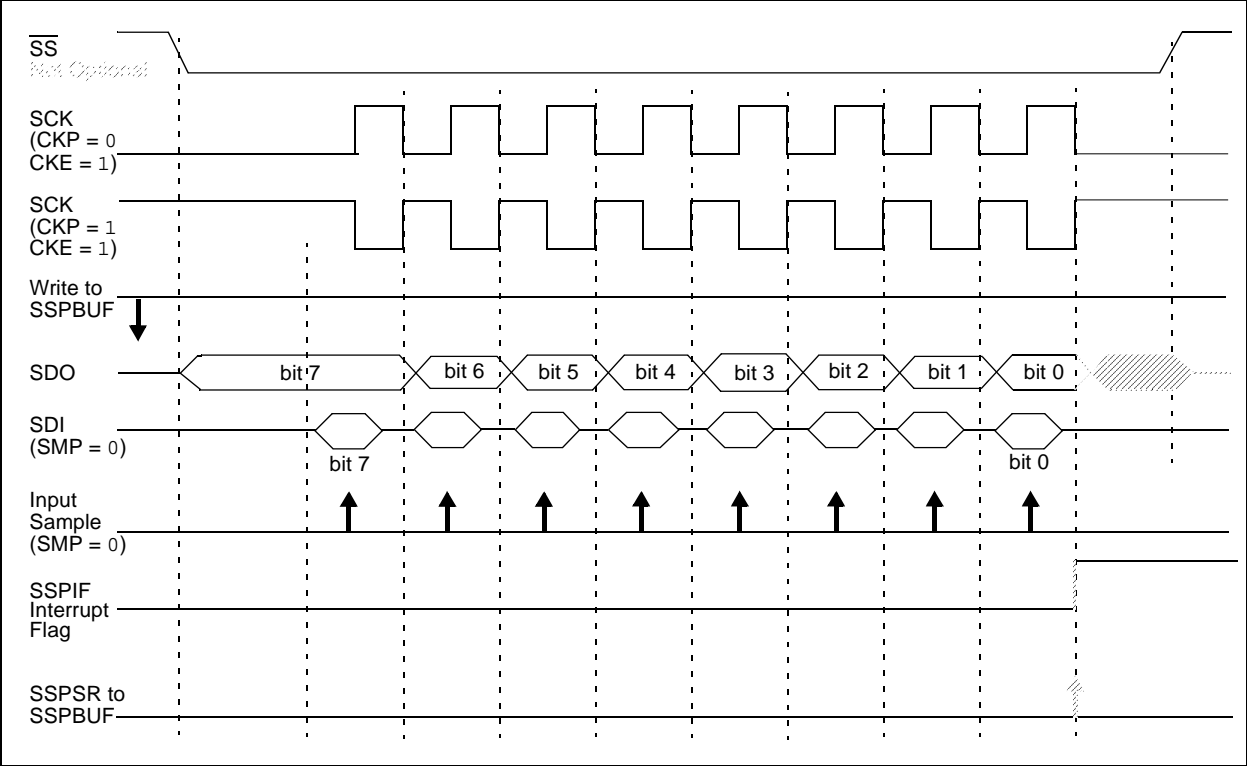


FIGURE 17-5: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)



PIC16(L)F722/3/4/6/7

TABLE 17-1: SUMMARY OF REGISTERS ASSOCIATED WITH SPI OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	--11 1111	--11 1111
APFCON	—	—	—	—	—	—	SSSEL	CCP2SEL	---- --00	---- --00
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PR2	Timer2 Period Register								1111 1111	1111 1111
SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
SSPSTAT	SMP	CKE	D/A	P	S	R/W	UA	BF	0000 0000	0000 0000
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111	1111 1111
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the SSP in SPI mode.

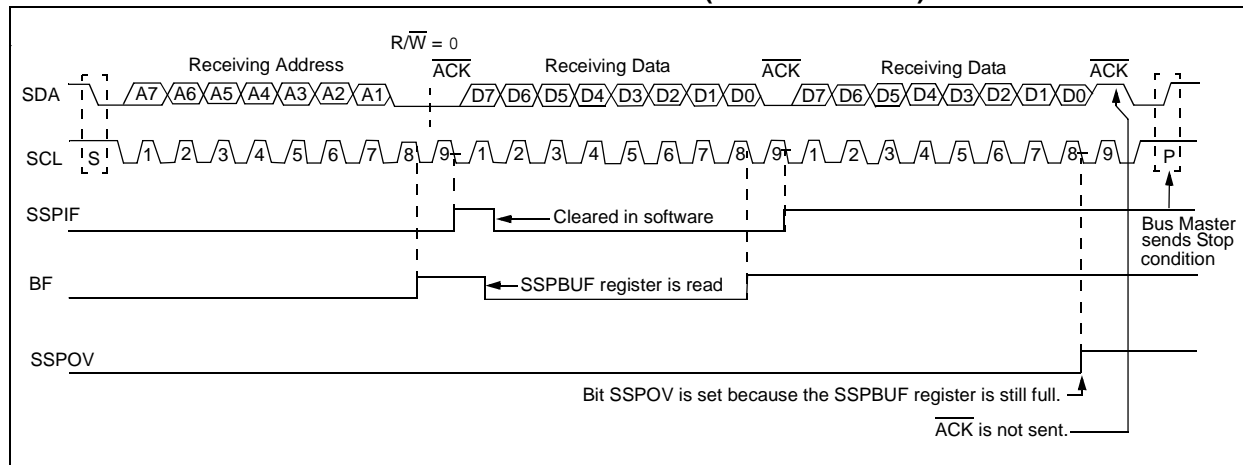
PIC16(L)F722/3/4/6/7

17.2.5 RECEPTION

When the R/\overline{W} bit of the received address byte is clear, the master will write data to the slave. If an address match occurs, the received address is loaded into the SSPBUF register. An address byte overflow will occur if that loaded address is not read from the SSPBUF before the next complete byte is received.

An SSP interrupt is generated for each data transfer byte. The BF, R/W and D/A bits of the SSPSTAT register are used to determine the status of the last received byte.

FIGURE 17-10: I²C WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)



SUBWF Subtract W from f

Syntax: [*label*] SUBWF f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) - (W) \rightarrow (\text{destination})$

Status Affected: C, DC, Z

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

C = 0	$W > f$
C = 1	$W \leq f$
DC = 0	$W<3:0> > f<3:0>$
DC = 1	$W<3:0> \leq f<3:0>$

XORLW Exclusive OR literal with W

Syntax: [*label*] XORLW k

Operands: $0 \leq k \leq 255$

Operation: $(W) .XOR. k \rightarrow (W)$

Status Affected: Z

Description: The contents of the W register are XOR'ed with the 8-bit literal 'k'. The result is placed in the W register.

SWAPF Swap Nibbles in f

Syntax: [*label*] SWAPF f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f<3:0>) \rightarrow (\text{destination}<7:4>)$,
 $(f<7:4>) \rightarrow (\text{destination}<3:0>)$

Status Affected: None

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

XORWF Exclusive OR W with f

Syntax: [*label*] XORWF f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(W) .XOR. (f) \rightarrow (\text{destination})$

Status Affected: Z

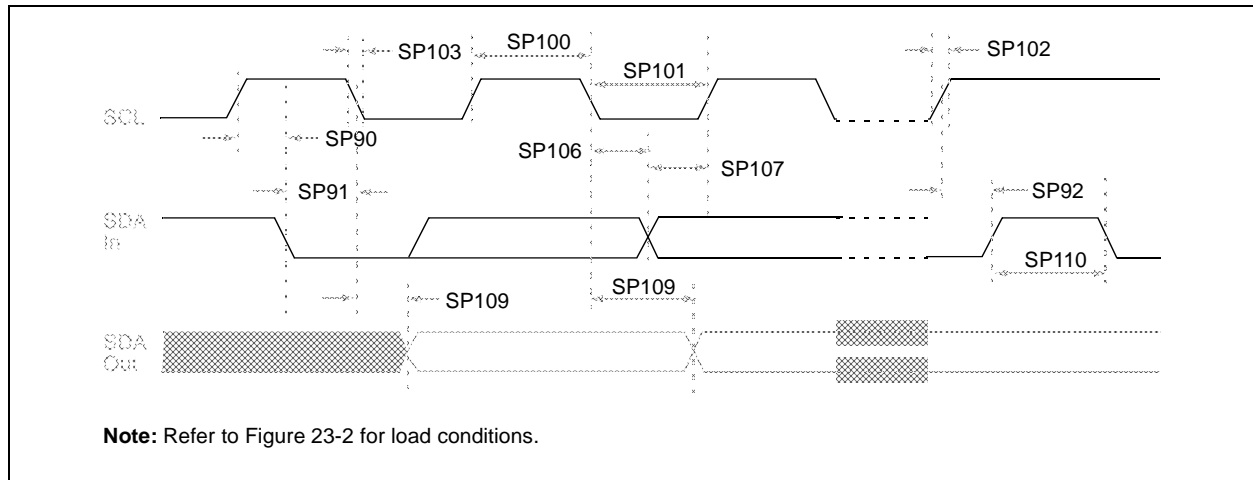
Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

TABLE 23-12: I²C BUS START/STOP BITS REQUIREMENTS

Param No.	Symbol	Characteristic		Min.	Typ	Max.	Units	Conditions
SP90*	TSU:STA	Start condition Setup time	100 kHz mode	4700	—	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	600	—	—		
SP91*	THD:STA	Start condition Hold time	100 kHz mode	4000	—	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—	—		
SP92*	TSU:STO	Stop condition Setup time	100 kHz mode	4700	—	—	ns	
			400 kHz mode	600	—	—		
SP93	THD:STO	Stop condition Hold time	100 kHz mode	4000	—	—	ns	
			400 kHz mode	600	—	—		

* These parameters are characterized but not tested.

FIGURE 23-21: I²C BUS DATA TIMING



PIC16(L)F722/3/4/6/7

FIGURE 24-5: PIC16F722/3/4/6/7 MAXIMUM I_{DD} vs. V_{DD} OVER F_{osc} , EXTRC MODE, $V_{CAP} = 0.1 \mu F$

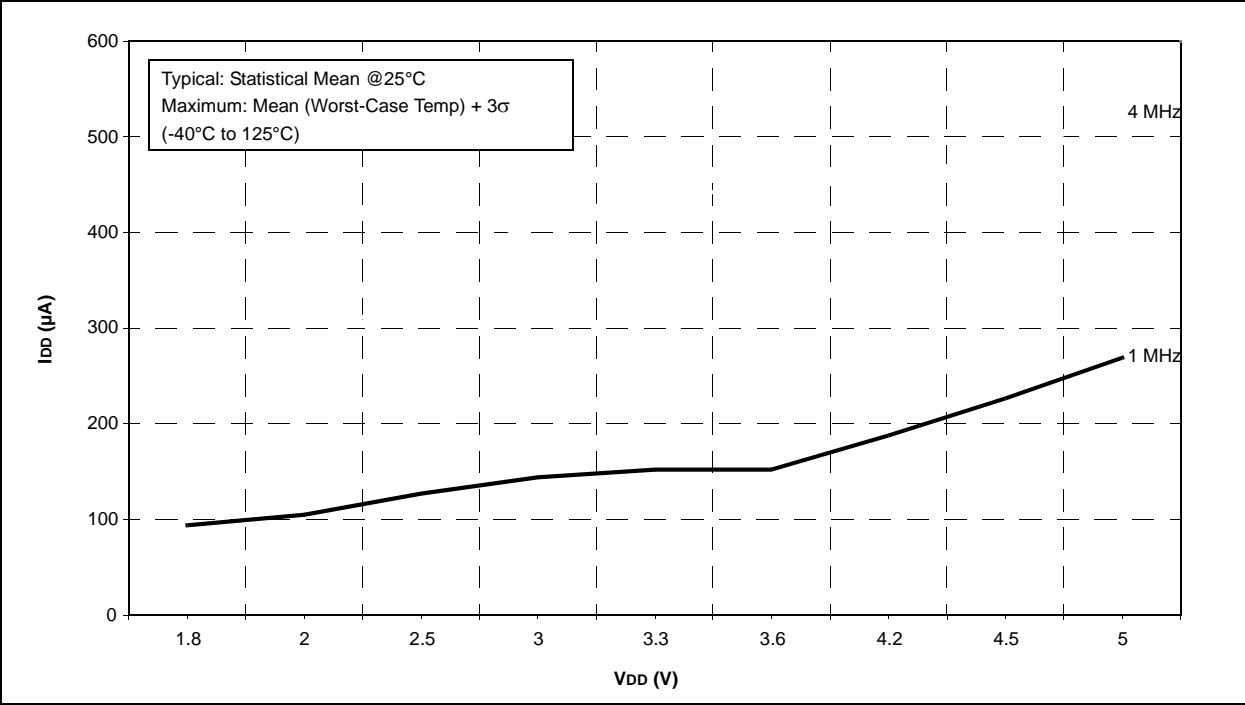
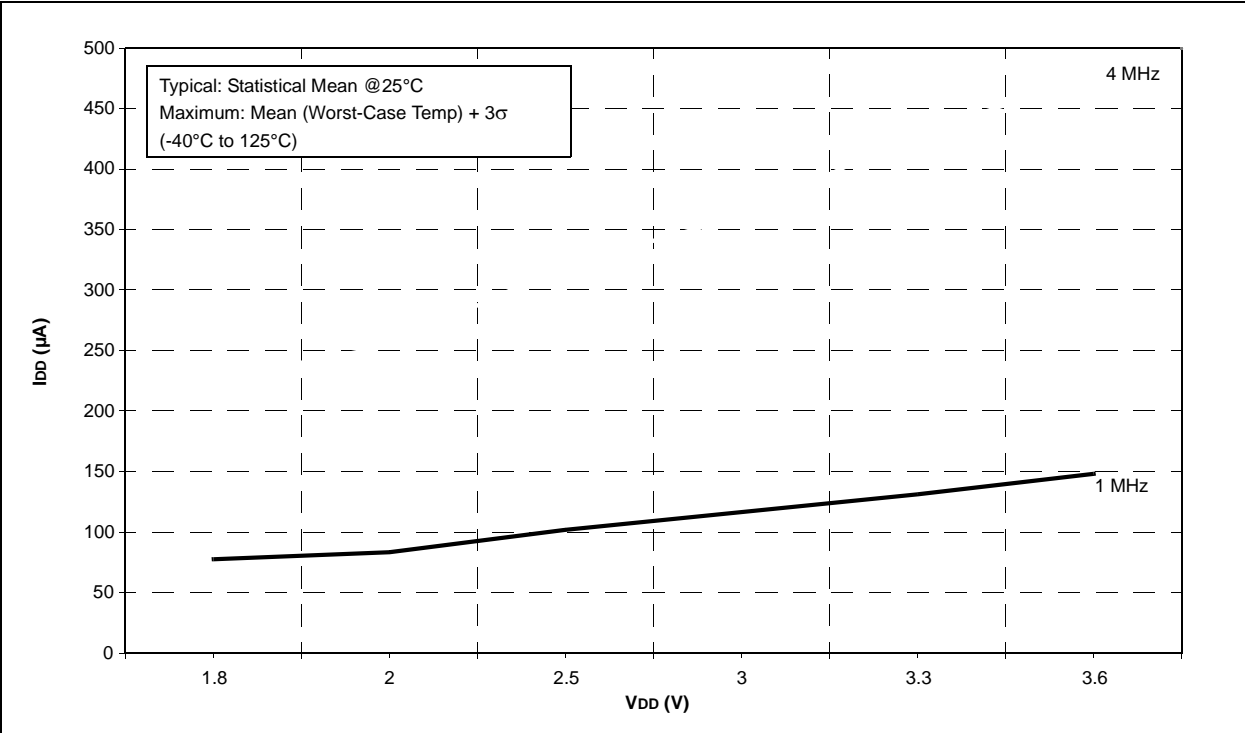


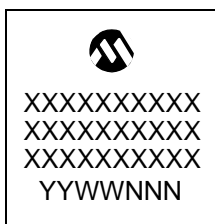
FIGURE 24-6: PIC16LF722/3/4/6/7 MAXIMUM I_{DD} vs. V_{DD} OVER F_{osc} , EXTRC MODE



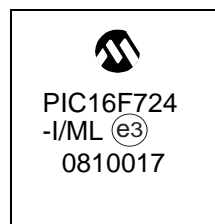
PIC16(L)F722/3/4/6/7

Package Marking Information (Continued)

44-Lead QFN



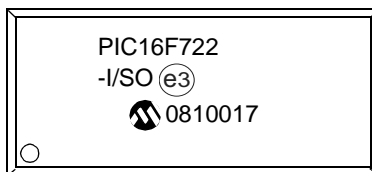
Example



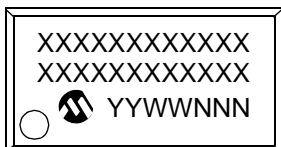
28-Lead SOIC



Example



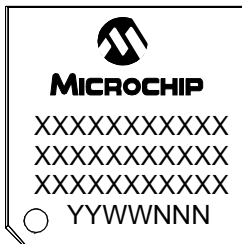
28-Lead SSOP



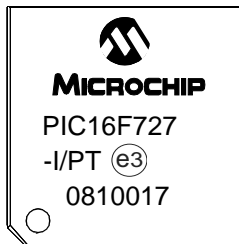
Example



44-Lead TQFP

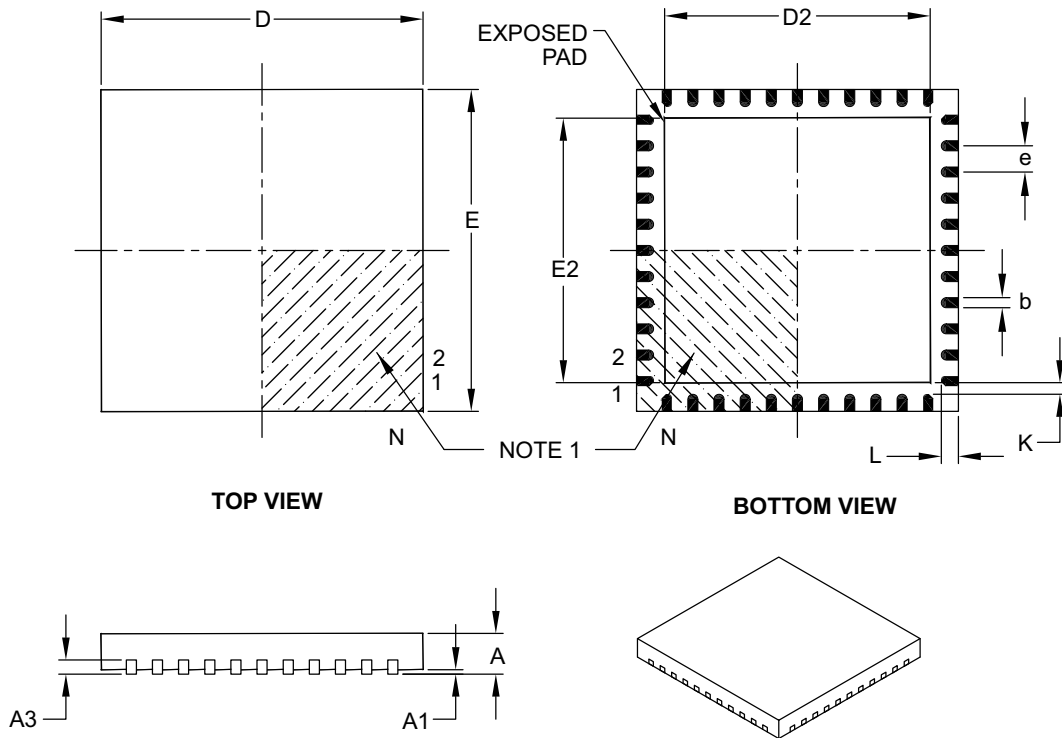


Example



44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		44		
Pitch	e		0.65 BSC		
Overall Height	A		0.80	0.90	1.00
Standoff	A1		0.00	0.02	0.05
Contact Thickness	A3		0.20 REF		
Overall Width	E		8.00 BSC		
Exposed Pad Width	E2		6.30	6.45	6.80
Overall Length	D		8.00 BSC		
Exposed Pad Length	D2		6.30	6.45	6.80
Contact Width	b		0.25	0.30	0.38
Contact Length	L		0.30	0.40	0.50
Contact-to-Exposed Pad	K		0.20	–	–

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103B

APPENDIX A: DATA SHEET REVISION HISTORY

Revision A (12/2007)

Original release.

Revision B (08/2008)

Electrical Specification updates; Package Drawings; miscellaneous updates.

Revision C (04/2009)

Revised data sheet title; Revised Low-Power Features section; Revised Section 6.2.2.4 RA3/AN3/VREF; Revised Figure 16-8 Synchronous Reception.

Revision D (07/2009)

Removed the Preliminary Label; Updated the "Electrical Characteristics" section; Added charts in the "Char. Data" section; Deleted "Based 8-Bit CMOS" from title; Updated the "Special Microcontroller Features" section and the "Peripheral Features" section; Changed the title of the "Low Power Features" section into "Extreme Low-Power Management PIC16LF72X with nanoWatt XLP" and updated this section; Inserted new section – "Analog Features" (page 1); Changed the title of the "Peripheral Features" section into "Peripheral Highlights" and updated the section.

Revision E (10/2009)

Added paragraph to section 5.0 (LDO Voltage Regulator); Updated the Electrical Specifications section (Added another absolute Maximum Rating; Updated section 23.1 and Table 23-4); Updated the Pin Diagrams with the UQFN package; Updated Table 1, adding UQFN; Updated section 23.5 (Thermal Considerations); Updated the Packaging Information section adding the UQFN Package; Updated the Product Identification System section.

Revision F (12/2015)

Updated Table 2; Updated 23.1, 23.3 and 9.2.4 Sections; Updated Figure 23-9; Other minor corrections.

APPENDIX B: MIGRATING FROM OTHER PIC[®] DEVICES

This discusses some of the issues in migrating from other PIC[®] devices to the PIC16F72X family of devices.

B.1 PIC16F77 to PIC16F72X

TABLE B-1: FEATURE COMPARISON

Feature	PIC16F77	PIC16F727
Max. Operating Speed	20 MHz	20 MHz
Max. Program Memory (Words)	8K	8K
Max. SRAM (Bytes)	368	368
A/D Resolution	8-bit	8-bit
Timers (8/16-bit)	2/1	2/1
Oscillator Modes	4	8
Brown-out Reset	Y	Y
Internal Pull-ups	RB<7:0>	RB<7:0>
Interrupt-on-change	RB<7:4>	RB<7:0>
Comparator	0	0
USART	Y	Y
Extended WDT	N	N
Software Control Option of WDT/BOR	N	N
INTOSC Frequencies	None	500 kHz - 16 MHz
Clock Switching	N	N

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>IXI⁽¹⁾</u>	<u>X</u>	<u>XX</u>	<u>XXX</u>
Device	Tape and Reel Option	Temperature Range	Package	Pattern
Device: PIC16F722, PIC16LF722, PIC16F722T, PIC16LF722T ⁽¹⁾ PIC16F723, PIC16LF723, PIC16F723T, PIC16LF723T ⁽¹⁾ PIC16F724, PIC16LF724, PIC16F724T, PIC16LF724T ⁽¹⁾ PIC16F726, PIC16LF726, PIC16F726T, PIC16LF726T ⁽¹⁾ PIC16F727, PIC16LF727, PIC16F727T, PIC16LF727T ⁽¹⁾				
Tape and Reel Option: I = -40°C to +85°C E = -40°C to +125°C MV = Micro Lead Frame (UQFN)				
Temperature Range: I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)				
Package: ML = Micro Lead Frame (QFN) P = Plastic DIP PT = TQFP (Thin Quad Flatpack) SO = SOIC SP = Skinny Plastic DIP SS = SSOP				

Examples:

a) PIC16F722-E/SP 301 = Extended Temp., skinny PDIP package, QTP pattern #301

b) PIC16F722-I/SO = Industrial Temp., SOIC package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.