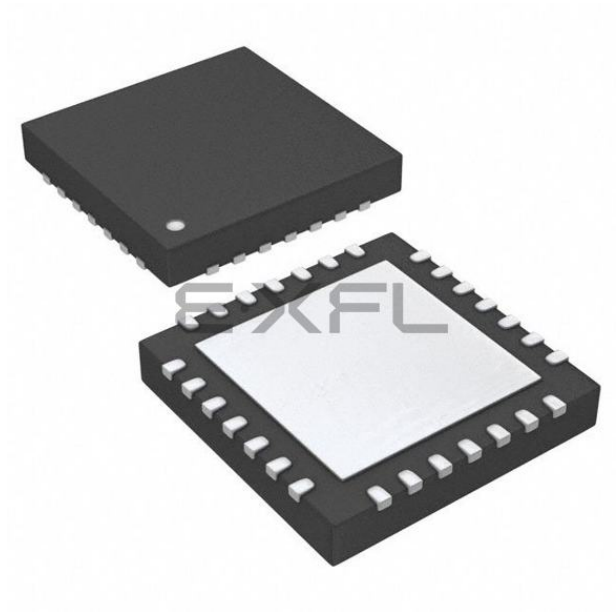

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf723-e-ml

TABLE 1-1: PIC16(L)F722/3/4/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RD3/CPS11	RD3	ST	CMOS	General purpose I/O.
	CPS11	AN	—	Capacitive sensing input 11.
RD4/CPS12	RD4	ST	CMOS	General purpose I/O.
	CPS12	AN	—	Capacitive sensing input 12.
RD5/CPS13	RD5	ST	CMOS	General purpose I/O.
	CPS13	AN	—	Capacitive sensing input 13.
RD6/CPS14	RD6	ST	CMOS	General purpose I/O.
	CPS14	AN	—	Capacitive sensing input 14.
RD7/CPS15	RD7	ST	CMOS	General purpose I/O.
	CPS15	AN	—	Capacitive sensing input 15.
RE0/AN5	RE0	ST	CMOS	General purpose I/O.
	AN5	AN	—	A/D Channel 5 input.
RE1/AN6	RE1	ST	CMOS	General purpose I/O.
	AN6	AN	—	A/D Channel 6 input.
RE2/AN7	RE2	ST	CMOS	General purpose I/O.
	AN7	AN	—	A/D Channel 7 input.
RE3/$\overline{MCLR}$/V_{PP}	RE3	TTL	—	General purpose input.
	$\overline{MCLR}$	ST	—	Master Clear with internal pull-up.
	V_{PP}	HV	—	Programming voltage.
V_{DD}	V_{DD}	Power	—	Positive supply.
V_{SS}	V_{SS}	Power	—	Ground reference.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note: The PIC16F722/3/4/6/7 devices have an internal low dropout voltage regulator. An external capacitor must be connected to one of the available V_{CAP} pins to stabilize the regulator. For more information, see **Section 5.0 "Low Dropout (LDO) Voltage Regulator"**. The PIC16LF722/3/4/6/7 devices do not have the voltage regulator and therefore no external capacitor is required.

2.2.2.3 PCON Register

The Power Control (PCON) register contains flag bits (refer to Table 3-2) to differentiate between a:

- Power-on Reset ($\overline{POR}$)
- Brown-out Reset ($\overline{BOR}$)
- Watchdog Timer Reset (WDT)
- External $\overline{MCLR}$ Reset

The PCON register also controls the software enable of the BOR.

The PCON register bits are shown in Register 2-3.

REGISTER 2-3: PCON: POWER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-q	R/W-q
—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown
q = Value depends on condition			

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **$\overline{POR}$:** Power-on Reset Status bit
- 1 = No Power-on Reset occurred
- 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit
- 1 = No Brown-out Reset occurred
- 0 = A Brown-out Reset occurred (must be set in software after a Power-on Reset or Brown-out Reset occurs)

Note 1: Set BOREN<1:0> = 01 in the Configuration Word register for this bit to control the $\overline{BOR}$.

4.3 Interrupts During Sleep

Some interrupts can be used to wake from Sleep. To wake from Sleep, the peripheral must be able to operate without the system clock. The interrupt source must have the appropriate Interrupt Enable bit(s) set prior to entering Sleep.

On waking from Sleep, if the GIE bit is also set, the processor will branch to the interrupt vector. Otherwise, the processor will continue executing instructions after the SLEEP instruction. The instruction directly after the SLEEP instruction will always be executed before branching to the ISR. Refer to the **Section 19.0 "Power-Down Mode (Sleep)"** for more details.

4.4 INT Pin

The external interrupt, INT pin, causes an asynchronous, edge-triggered interrupt. The INTEDG bit of the OPTION register determines on which edge the interrupt will occur. When the INTEDG bit is set, the rising edge will cause the interrupt. When the INTEDG bit is clear, the falling edge will cause the interrupt. The INTF bit of the INTCON register will be set when a valid edge appears on the INT pin. If the GIE and INTE bits are also set, the processor will redirect program execution to the interrupt vector. This interrupt is disabled by clearing the INTE bit of the INTCON register.

4.5 Context Saving

When an interrupt occurs, only the return PC value is saved to the stack. If the ISR modifies or uses an instruction that modifies key registers, their values must be saved at the beginning of the ISR and restored when the ISR completes. This prevents instructions following the ISR from using invalid data. Examples of key registers include the W, STATUS, FSR and PCLATH registers.

Note:	The microcontroller does not normally require saving the PCLATH register. However, if computed GOTO's are used, the PCLATH register must be saved at the beginning of the ISR and restored when the ISR is complete to ensure correct program flow.

The code shown in Example 4-1 can be used to do the following.

- Save the W register
- Save the STATUS register
- Save the PCLATH register
- Execute the ISR program
- Restore the PCLATH register
- Restore the STATUS register
- Restore the W register

Since most instructions modify the W register, it must be saved immediately upon entering the ISR. The SWAPF instruction is used when saving and restoring the W and STATUS registers because it will not affect any bits in the STATUS register. It is useful to place W_TEMP in shared memory because the ISR cannot predict which bank will be selected when the interrupt occurs.

The processor will branch to the interrupt vector by loading the PC with 0004h. The PCLATH register will remain unchanged. This requires the ISR to ensure that the PCLATH register is set properly before using an instruction that causes PCLATH to be loaded into the PC. See **Section 2.3 "PCL and PCLATH"** for details on PC operation.

4.5.2 PIE1 REGISTER

The PIE1 register contains the interrupt enable bits, as shown in Register 4-2.

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 4-2: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TMR1GIE:** Timer1 Gate Interrupt Enable bit
1 = Enable the Timer1 Gate Acquisition complete interrupt
0 = Disable the Timer1 Gate Acquisition complete interrupt

bit 6 **ADIE:** A/D Converter (ADC) Interrupt Enable bit
1 = Enables the ADC interrupt
0 = Disables the ADC interrupt

bit 5 **RCIE:** USART Receive Interrupt Enable bit
1 = Enables the USART receive interrupt
0 = Disables the USART receive interrupt

bit 4 **TXIE:** USART Transmit Interrupt Enable bit
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt

bit 3 **SSPIE:** Synchronous Serial Port (SSP) Interrupt Enable bit
1 = Enables the SSP interrupt
0 = Disables the SSP interrupt

bit 2 **CCP1IE:** CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 1 **TMR2IE:** TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the Timer2 to PR2 match interrupt
0 = Disables the Timer2 to PR2 match interrupt

bit 0 **TMR1IE:** Timer1 Overflow Interrupt Enable bit
1 = Enables the Timer1 overflow interrupt
0 = Disables the Timer1 overflow interrupt

4.5.5 PIR2 REGISTER

The PIR2 register contains the interrupt flag bits, as shown in Register 4-5.

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 4-5: PIR2: PERIPHERAL INTERRUPT REQUEST REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	CCP2IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-1 **Unimplemented:** Read as '0'

bit 0 **CCP2IF:** CCP2 Interrupt Flag bit

Capture Mode:

1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred

Compare Mode:

1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred

PWM mode:

Unused in this mode

TABLE 4-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
OPTION_REG	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIE2	—	—	—	—	—	—	—	CCP2IE	---- ---0	---- ---0
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIR2	—	—	—	—	—	—	—	CCP2IF	---- ---0	---- ---0

Legend: - = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Capture, Compare and PWM.

FIGURE 6-19: BLOCK DIAGRAM OF RC6

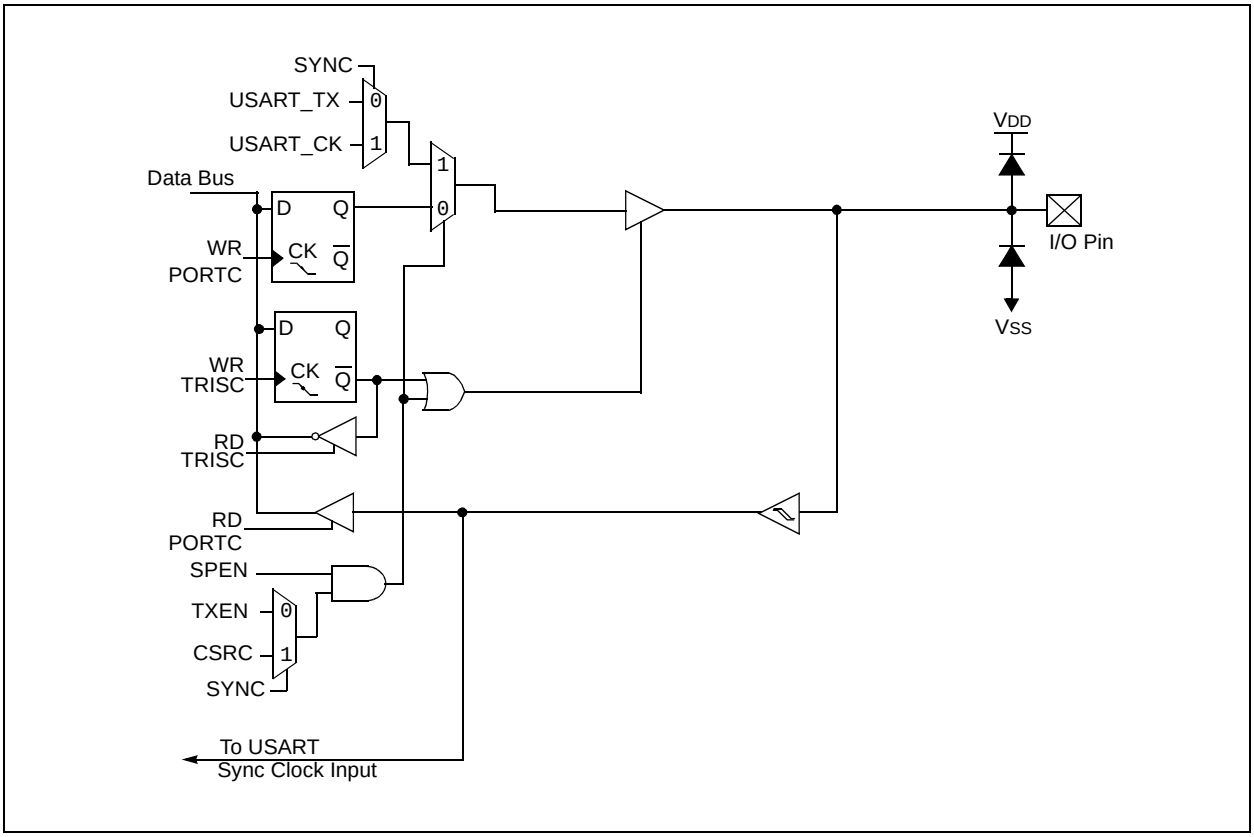
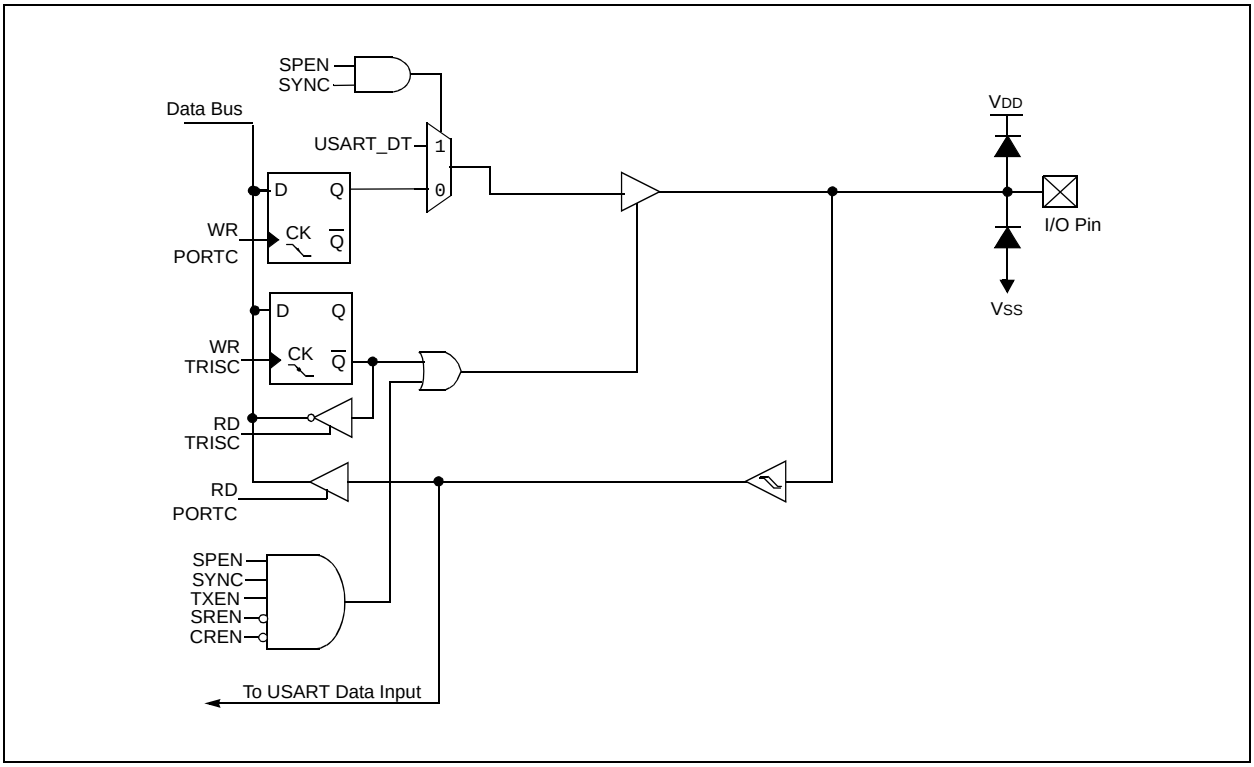


FIGURE 6-20: BLOCK DIAGRAM OF RC7



7.2 Clock Source Modes

Clock source modes can be classified as external or internal.

- Internal clock source (INTOSC) is contained within the oscillator module and derived from a 500 kHz high precision oscillator. The oscillator module has eight selectable output frequencies, with a maximum internal frequency of 16 MHz.
- External clock modes rely on external circuitry for the clock source. Examples are: oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes) and Resistor-Capacitor (RC) mode circuits.

The system clock can be selected between external or internal clock sources via the FOSC bits of the Configuration Word 1.

7.3 Internal Clock Modes

The oscillator module has eight output frequencies derived from a 500 kHz high precision oscillator. The IRCF bits of the OSCCON register select the postscaler applied to the clock source dividing the frequency by 1, 2, 4 or 8. Setting the PLLEN bit of the Configuration Word 1 locks the internal clock source to 16 MHz before the postscaler is selected by the IRCF bits. The PLLEN bit must be set or cleared at the time of programming; therefore, only the upper or low four clock source frequencies are selectable in software.

7.3.1 INTOSC AND INTOSCIO MODES

The INTOSC and INTOSCIO modes configure the internal oscillators as the system clock source when the device is programmed using the oscillator selection or the FOSC<2:0> bits in the CONFIG1 register. See **Section 8.0 “Device Configuration”** for more information.

In INTOSC mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT outputs the selected internal oscillator frequency divided by 4. The CLKOUT signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements.

In INTOSCIO mode, OSC1/CLKIN and OSC2/CLKOUT are available for general purpose I/O.

7.3.2 FREQUENCY SELECT BITS (IRCF)

The output of the 500 kHz INTOSC and 16 MHz INTOSC, with Phase-Locked Loop enabled, connect to a postscaler and multiplexer (see Figure 7-1). The Internal Oscillator Frequency Select bits (IRCF) of the OSCCON register select the frequency output of the internal oscillator. Depending upon the PLLEN bit, one of four frequencies of two frequency sets can be selected via software:

If PLLEN = 1, frequency selection is as follows:

- 16 MHz
- 8 MHz (default after Reset)
- 4 MHz
- 2 MHz

If PLLEN = 0, frequency selection is as follows:

- 500 kHz
- 250 kHz (default after Reset)
- 125 kHz
- 62.5 kHz

Note:	Following any Reset, the IRCF<1:0> bits of the OSCCON register are set to ‘10’ and the frequency selection is set to 8 MHz or 250 kHz. The user can modify the IRCF bits to select a different frequency.

There is no start-up delay before a new frequency selected in the IRCF bits takes effect. This is because the old and new frequencies are derived from INTOSC via the postscaler and multiplexer.

Start-up delay specifications are located in the Table 23-2 in **Section 23.0 “Electrical Specifications”**.

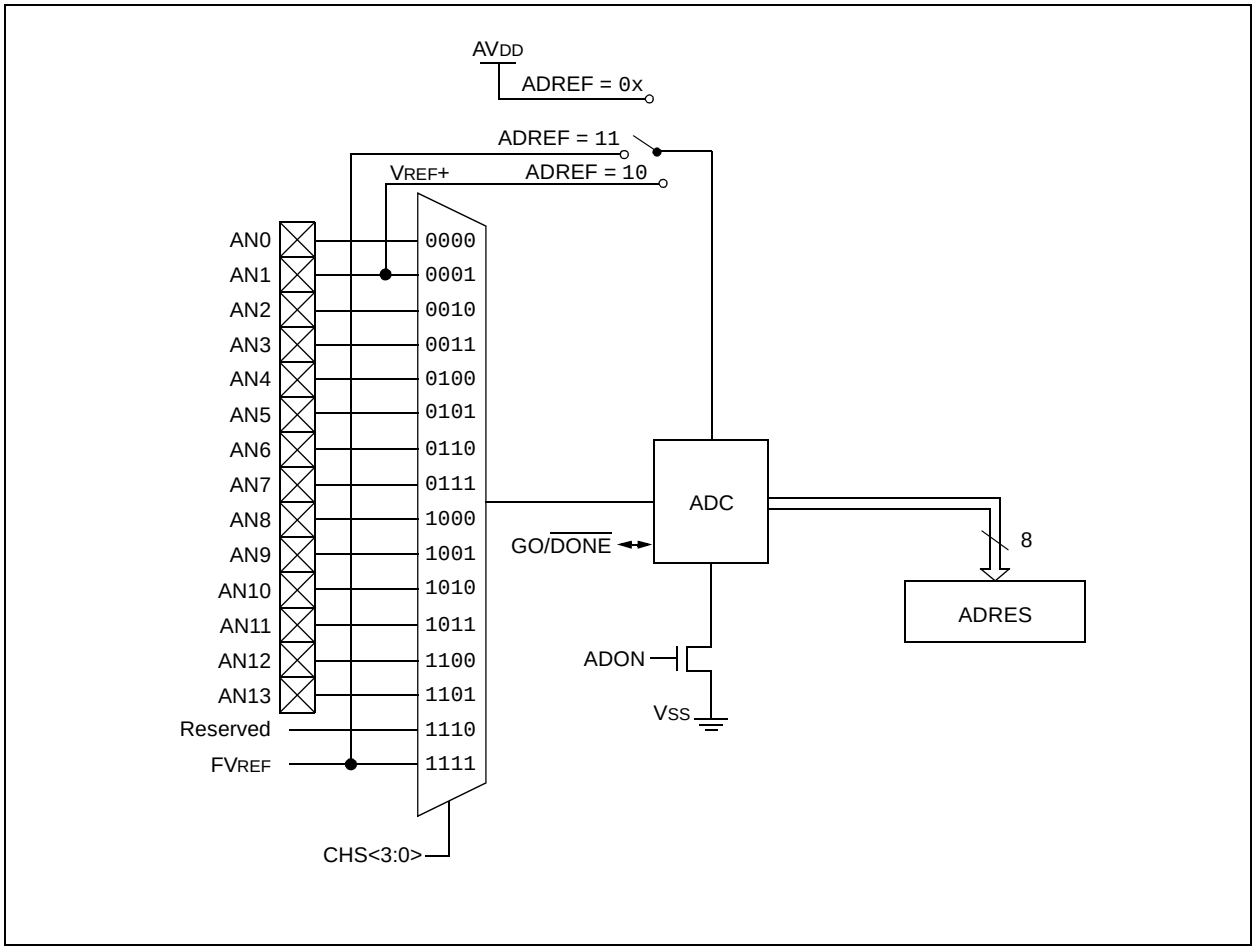
9.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 8-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 8-bit binary result via successive approximation and stores the conversion result into the ADC result register (ADRES). Figure 9-1 shows the block diagram of the ADC.

The ADC voltage reference is software selectable to be either internally generated or externally supplied.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

FIGURE 9-1: ADC BLOCK DIAGRAM



12.7 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt on rollover, you must set these bits:

- TMR1ON bit of the T1CON register
- TMR1IE bit of the PIE1 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

Note:	The TMR1H:TMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

12.8 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- TMR1ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set
- $\overline{\text{T1SYNC}}$ bit of the T1CON register must be set
- TMR1CS bits of the T1CON register must be configured
- T1OSCEN bit of the T1CON register must be configured
- TMR1GIE bit of the T1GCON register must be configured

The device will wake-up on an overflow and execute the next instructions. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine (0004h).

12.9 CCP Capture/Compare Time Base

The CCP module uses the TMR1H:TMR1L register pair as the time base when operating in Capture or Compare mode.

In Capture mode, the value in the TMR1H:TMR1L register pair is copied into the CCPR1H:CCPR1L register pair on a configured event.

In Compare mode, an event is triggered when the value CCPR1H:CCPR1L register pair matches the value in the TMR1H:TMR1L register pair. This event can be a Special Event Trigger.

For more information, see **Section 15.0 "Capture/Compare/PWM (CCP) Module"**.

12.10 CCP Special Event Trigger

When the CCP is configured to trigger a special event, the trigger will clear the TMR1H:TMR1L register pair. This special event does not cause a Timer1 interrupt. The CCP module may still be configured to generate a CCP interrupt.

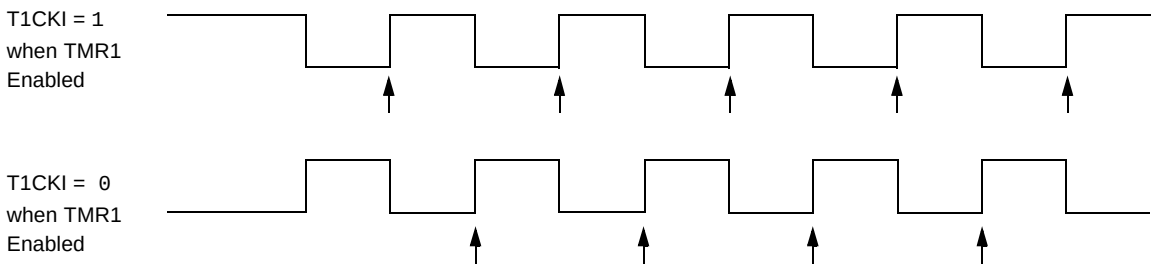
In this mode of operation, the CCPR1H:CCPR1L register pair becomes the period register for Timer1.

Timer1 should be synchronized to the FOSC/4 to utilize the Special Event Trigger. Asynchronous operation of Timer1 can cause a Special Event Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with a Special Event Trigger from the CCP, the write will take precedence.

For more information, see **Section 9.2.5 "Special Event Trigger"**.

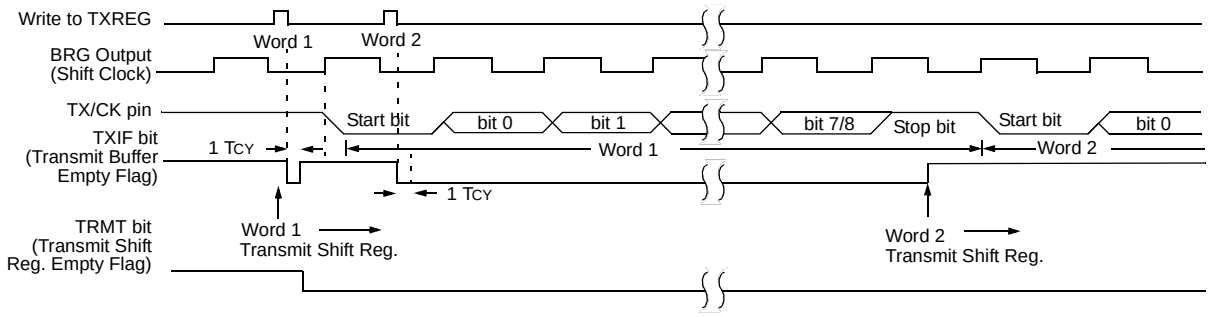
FIGURE 12-2: TIMER1 INCREMENTING EDGE



Note 1: Arrows indicate counter increments.

2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

FIGURE 16-4: ASYNCHRONOUS TRANSMISSION (BACK-TO-BACK)



Note: This timing diagram shows two consecutive transmissions.

TABLE 16-1: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SPBRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	0000 0000	0000 0000
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
TXREG	AUSART Transmit Data Register								0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Asynchronous Transmission.

16.1.2 AUSART ASYNCHRONOUS RECEIVER

The Asynchronous mode is typically used in RS-232 systems. The receiver block diagram is shown in Figure 16-2. The data is received on the RX/DT pin and drives the data recovery block. The data recovery block is actually a high-speed shifter operating at 16 times the baud rate, whereas the serial Receive Shift Register (RSR) operates at the bit rate. When all eight or nine bits of the character have been shifted in, they are immediately transferred to a two character First-In First-Out (FIFO) memory. The FIFO buffering allows reception of two complete characters and the start of a third character before software must start servicing the AUSART receiver. The FIFO and RSR registers are not directly accessible by software. Access to the received data is via the RCREG register.

16.1.2.1 Enabling the Receiver

The AUSART receiver is enabled for asynchronous operation by configuring the following three control bits:

- CREN = 1
- SYNC = 0
- SPEN = 1

All other AUSART control bits are assumed to be in their default state.

Setting the CREN bit of the RCSTA register enables the receiver circuitry of the AUSART. Clearing the SYNC bit of the TXSTA register configures the AUSART for asynchronous operation. Setting the SPEN bit of the RCSTA register enables the AUSART and automatically configures the RX/DT I/O pin as an input.

Note:	When the SPEN bit is set the TX/CK I/O pin is automatically configured as an output, regardless of the state of the corresponding TRIS bit and whether or not the AUSART transmitter is enabled. The PORT latch is disconnected from the output driver so it is not possible to use the TX/CK pin as a general purpose output.

16.1.2.2 Receiving Data

The receiver data recovery circuit initiates character reception on the falling edge of the first bit. The first bit, also known as the Start bit, is always a zero. The data recovery circuit counts one-half bit time to the center of the Start bit and verifies that the bit is still a zero. If it is not a zero then the data recovery circuit aborts character reception, without generating an error, and resumes looking for the falling edge of the Start bit. If the Start bit zero verification succeeds then the data recovery circuit counts a full bit time to the center of the next bit. The bit is then sampled by a majority detect circuit and the resulting '0' or '1' is shifted into the RSR. This repeats until all data bits have been sampled and shifted into the RSR. One final bit time is measured and the level sampled. This is the Stop bit, which is always a '1'. If the data recovery circuit samples a '0' in the Stop bit position then a framing error is set for this character, otherwise the framing error is cleared for this character. Refer to **Section 16.1.2.4 "Receive Framing Error"** for more information on framing errors.

Immediately after all data bits and the Stop bit have been received, the character in the RSR is transferred to the AUSART receive FIFO and the RCIF interrupt flag bit of the PIR1 register is set. The top character in the FIFO is transferred out of the FIFO by reading the RCREG register.

Note:	If the receive FIFO is overrun, no additional characters will be received until the overrun condition is cleared. Refer to **Section 16.1.2.5 "Receive Overrun Error"** for more information on overrun errors.

16.1.2.3 Receive Interrupts

The RCIF interrupt flag bit of the PIR1 register is set whenever the AUSART receiver is enabled and there is an unread character in the receive FIFO. The RCIF interrupt flag bit is read-only, it cannot be set or cleared by software.

RCIF interrupts are enabled by setting all of the following bits:

- RCIE interrupt enable bit of the PIE1 register
- PEIE peripheral interrupt enable bit of the INTCON register
- GIE global interrupt enable bit of the INTCON register

The RCIF interrupt flag bit of the PIR1 register will be set when there is an unread character in the FIFO, regardless of the state of interrupt enable bits.

RETFIE	Return from Interrupt
Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a 2-cycle instruction.
Words:	1
Cycles:	2
Example:	`RETFIE` After Interrupt PC = TOS GIE = 1

RETLW	Return with literal in W
Syntax:	[*label*] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the 8-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.
Words:	1
Cycles:	2

Example:	`CALL TABLE;W contains table`
	`;offset value`
	`TABLE ;W now has table value`
	`•`
	`•`
	`ADDWF PC ;W = offset`
	`RETLW k1 ;Begin table`
	`RETLW k2 ;`
	`•`
	`•`
	`•`
	`RETLW kn ; End of table`
	
	Before Instruction
	W = 0x07
	After Instruction
	W = value of k8

RETURN	Return from Subroutine
Syntax:	[*label*] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a 2-cycle instruction.

23.4 DC Characteristics: PIC16(L)F722/3/4/6/7-I/E (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
D130	EP	Cell Endurance	100	1k	—	E/W	Temperature during programming: 10°C ≤ TA ≤ 40°C
D131		VDD for Read	VMIN	—	—	V	
		Voltage on $\overline{\text{MCLR}}$/VPP during Erase/Program	8.0	—	9.0	V	Temperature during programming: 10°C ≤ TA ≤ 40°C
		VDD for Bulk Erase	2.7	3	—	V	Temperature during programming: 10°C ≤ TA ≤ 40°C
D132	VPEW	VDD for Write or Row Erase	2.7	—	—	V	VMIN = Minimum operating voltage VMAX = Maximum operating voltage
	IPPPGM	Current on $\overline{\text{MCLR}}$/VPP during Erase/Write	—	—	5.0	mA	Temperature during programming: 10°C ≤ TA ≤ 40°C
	IDDPGM	Current on VDD during Erase/ Write	—		5.0	mA	Temperature during programming: 10°C ≤ TA ≤ 40°C
D133	TPEW	Erase/Write cycle time	—		2.8	ms	Temperature during programming: 10°C ≤ TA ≤ 40°C
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
		VCAP Capacitor Charging					
D135		Charging current	—	200	—	µA	
D135A		Source/sink capability when charging complete	—	0.0	—	mA	

Legend: TBD = To Be Determined

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: Including OSC2 in CLKOUT mode.

TABLE 23-7: PIC16F722/3/4/6/7 A/D CONVERTER (ADC) CHARACTERISTICS:

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
AD01	NR	Resolution	—	—	8	bit	
AD02	EIL	Integral Error	—	—	±1.7	LSb	VREF = 3.0V
AD03	EDL	Differential Error	—	—	±1	LSb	No missing codes VREF = 3.0V
AD04	EOFF	Offset Error	—	—	±2.2	LSb	VREF = 3.0V
AD05	EGN	Gain Error	—	—	±1.5	LSb	VREF = 3.0V
AD06	VREF	Reference Voltage(3)	1.8	—	VDD	V	
AD07	VAIN	Full-Scale Range	VSS	—	VREF	V	
AD08	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	50	kΩ	Can go higher if external 0.01µF capacitor is present on input pin.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error includes integral, differential, offset and gain errors.

2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

3: When ADC is off, it will not consume any current other than leakage current. The power-down current specification includes any such leakage from the ADC module.

TABLE 23-8: PIC16F722/3/4/6/7 A/D CONVERSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
AD130*	TAD	A/D Clock Period	1.0	—	9.0	µs	TOSC-based
		A/D Internal RC Oscillator Period	1.0	2.0	6.0	µs	ADCS<1:0> = 11 (ADRC mode)
AD131	TCNV	Conversion Time (not including Acquisition Time)(1)	—	10.5	—	TAD	Set GO/$\overline{\text{DONE}}$ bit to conversion complete
AD132*	TACQ	Acquisition Time	—	1.0	—	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The ADRES register may be read on the following TCY cycle.

FIGURE 24-21: PIC16F722/3/4/6/7 MAXIMUM IDD vs. FOSC OVER VDD, INTOSC MODE, VCAP =1µF

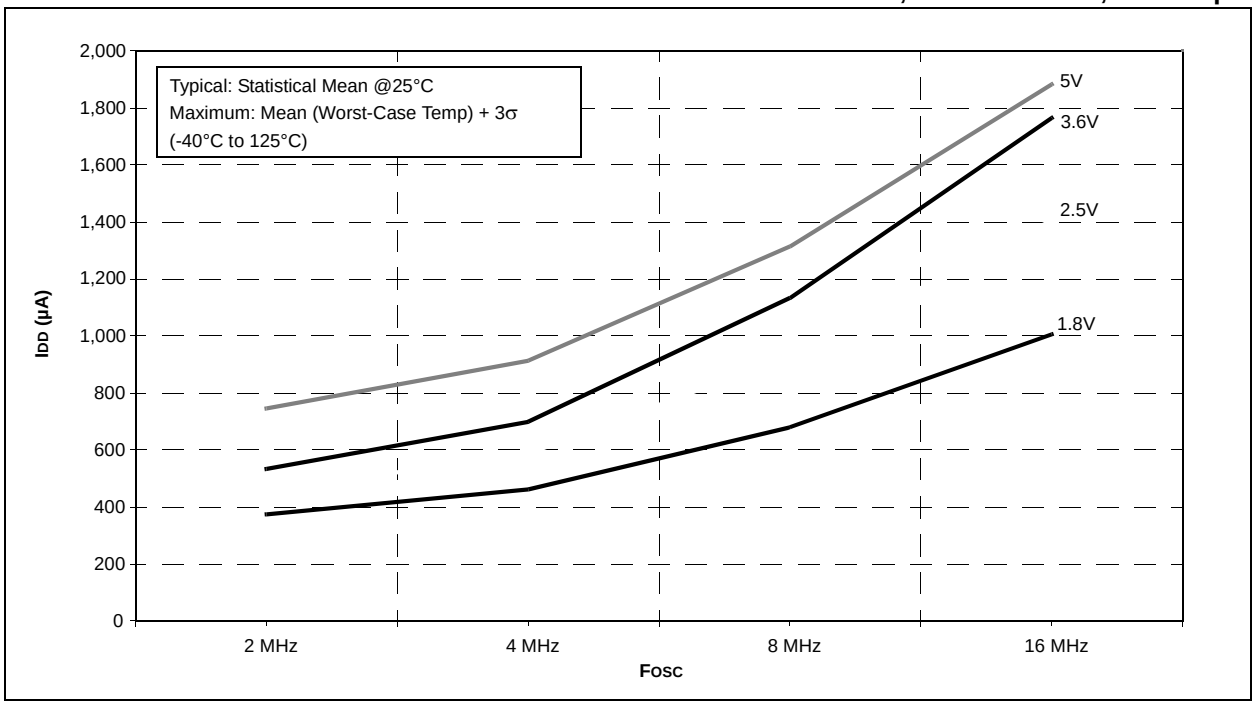


FIGURE 24-22: PIC16LF722/3/4/6/7 MAXIMUM IDD vs. FOSC OVER VDD, INTOSC MODE

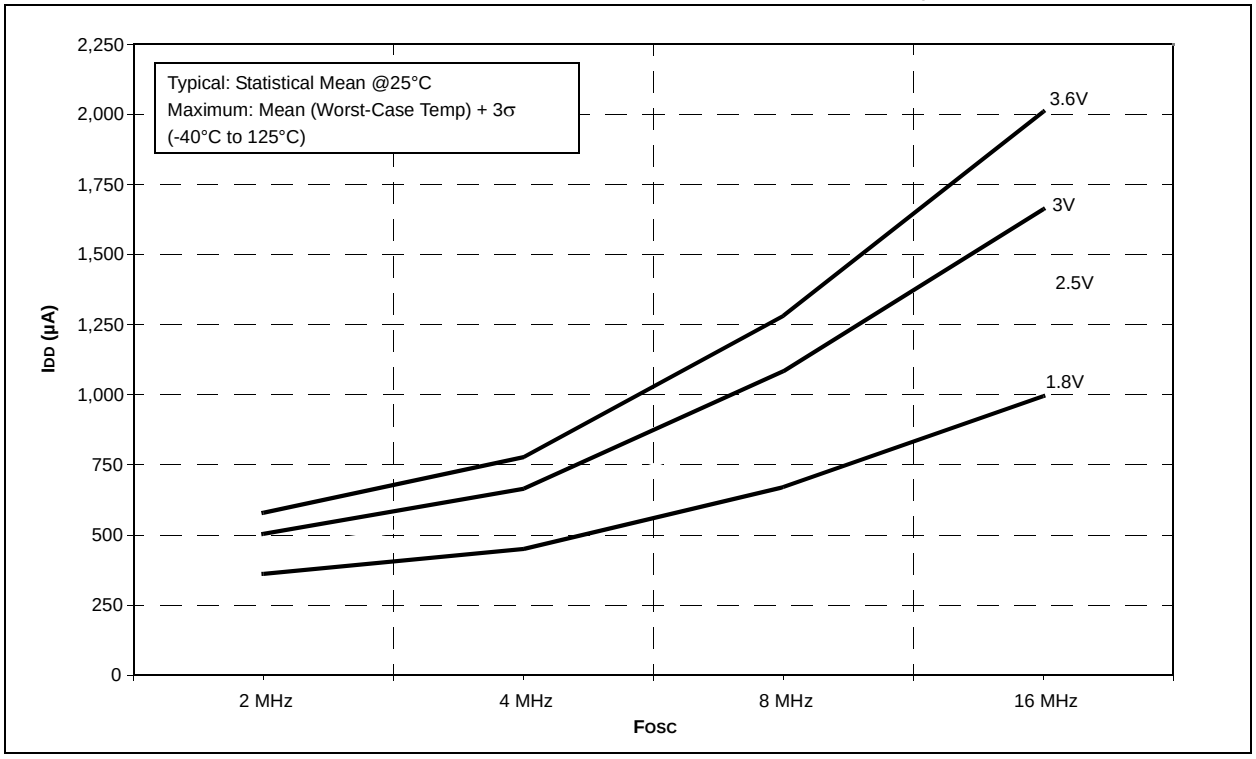


FIGURE 24-35: PIC16F722/3/4/6/7 CAP SENSE HIGH POWER IPD vs. VDD, VCAP = 0.1 µF

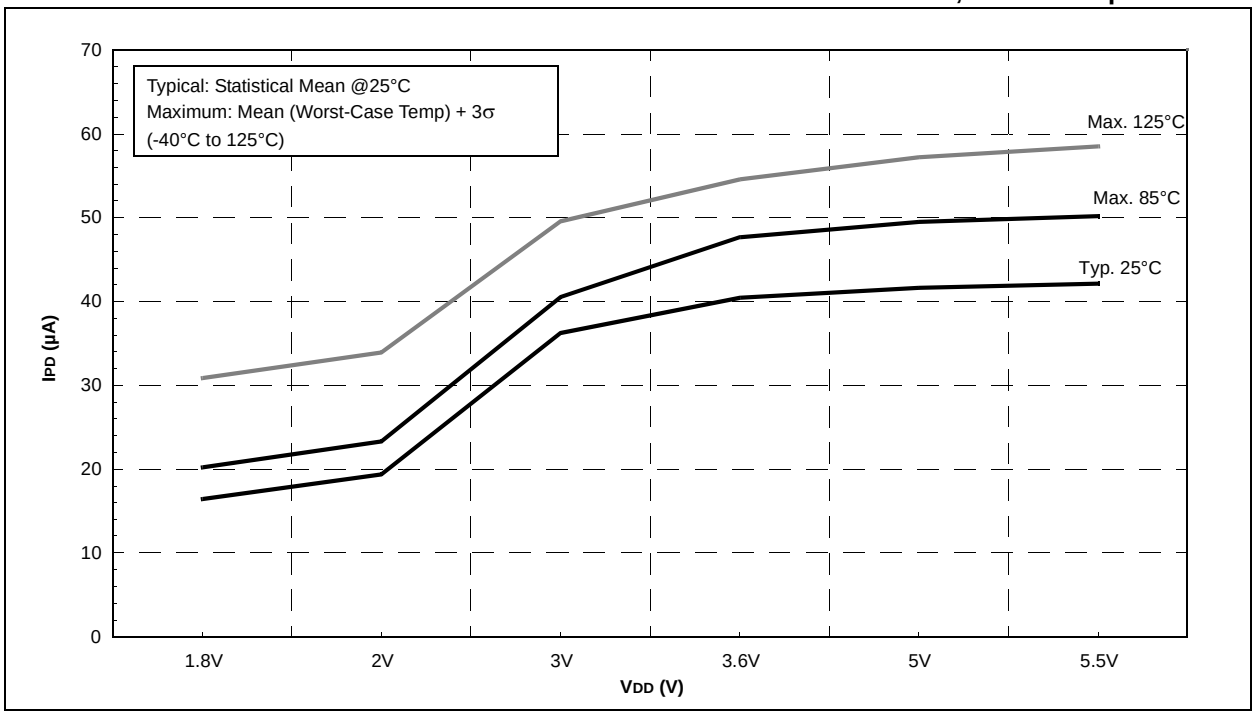


FIGURE 24-36: PIC16LF722/3/4/6/7 CAP SENSE HIGH POWER IPD vs. VDD

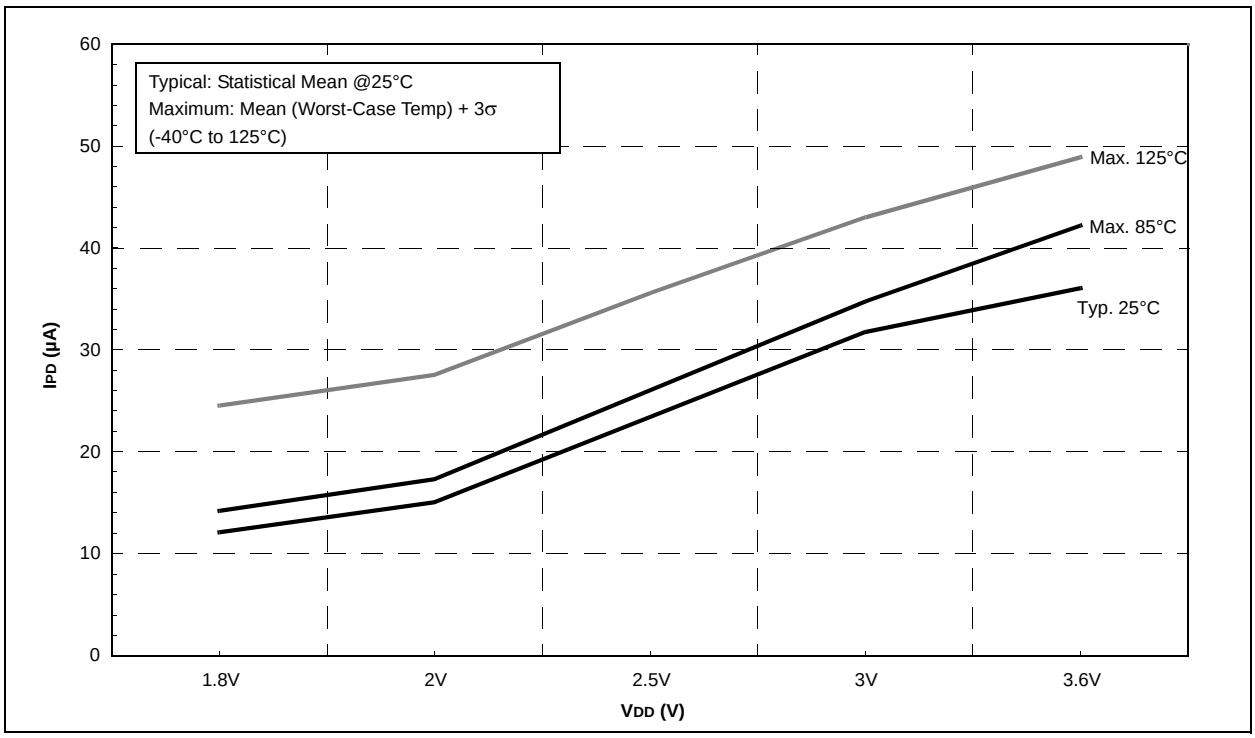


FIGURE 24-65: PIC16F722/3/4/6/7 CAP SENSOR HYSTERESIS, POWER MODE = HIGH

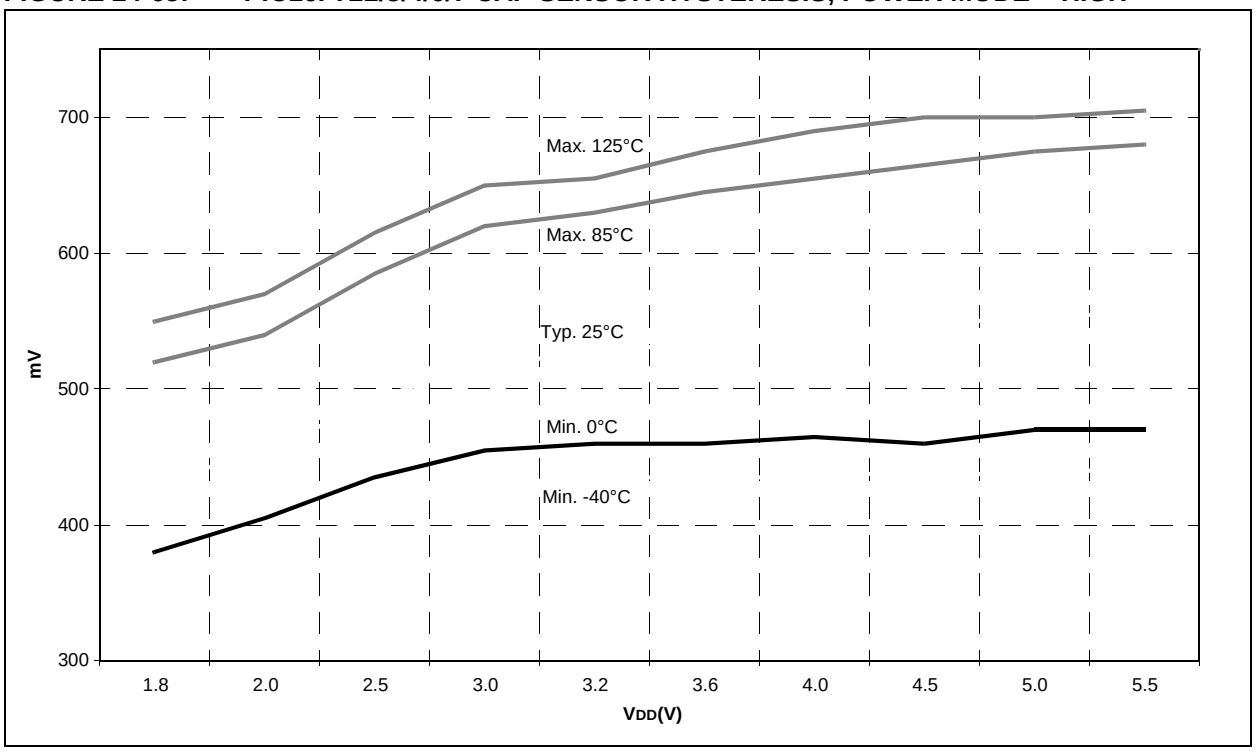
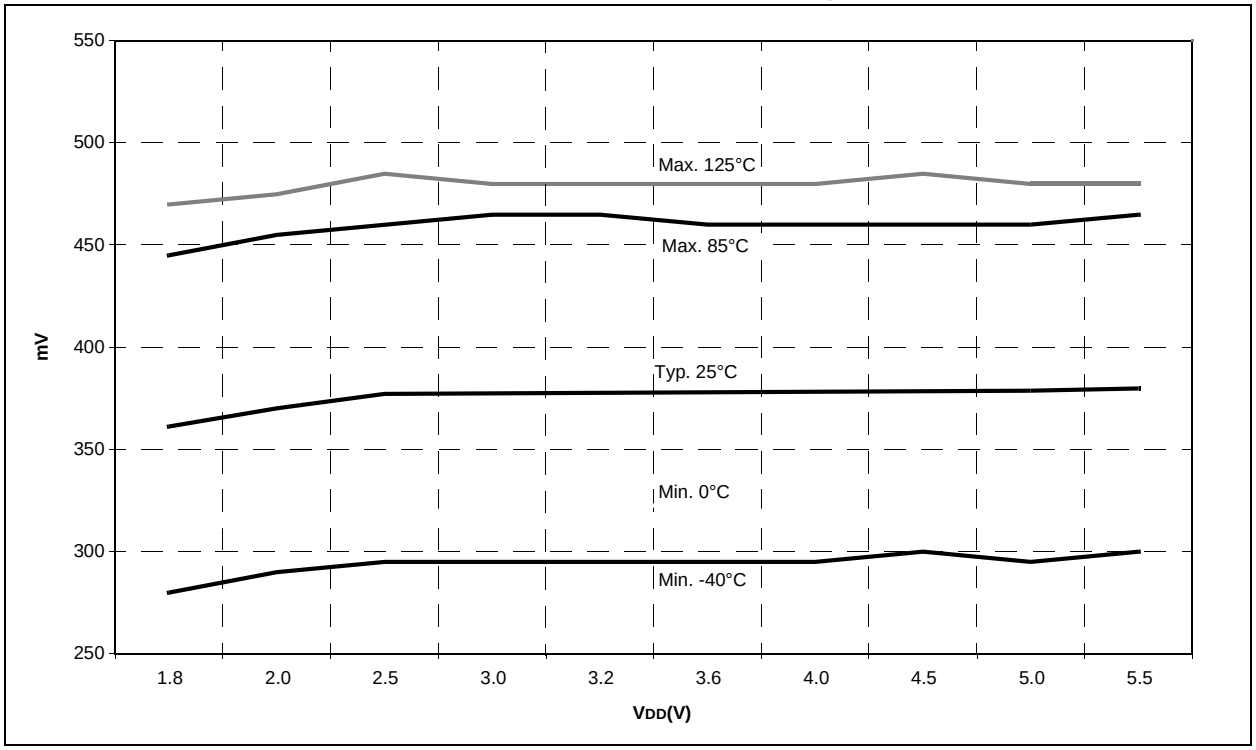
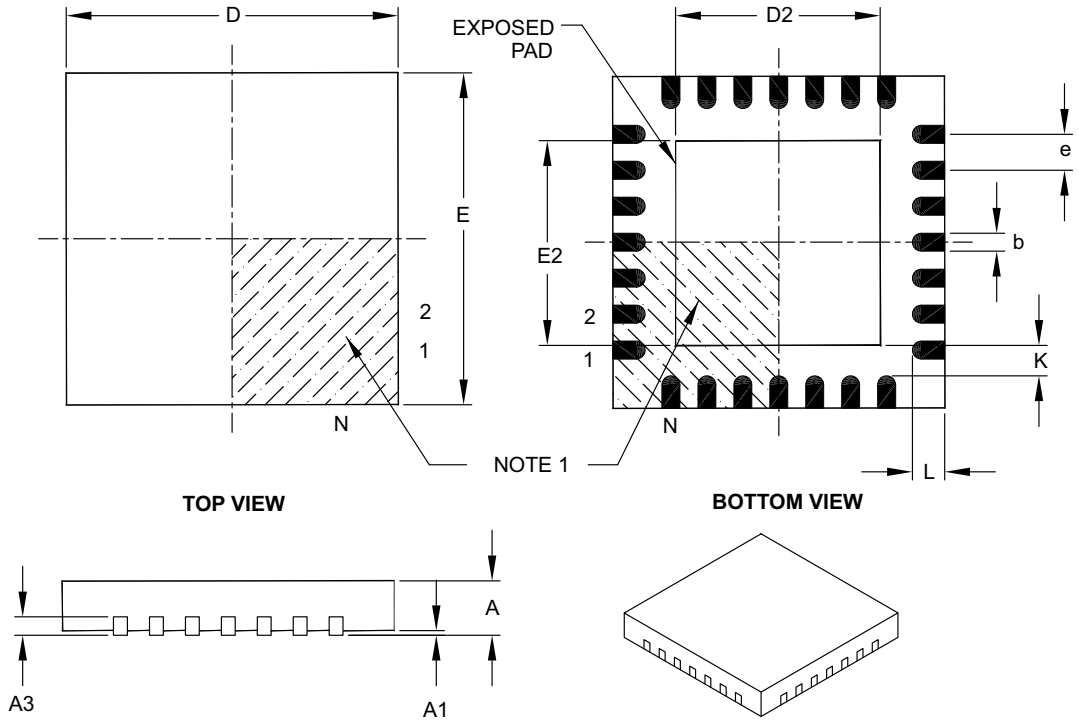


FIGURE 24-66: PIC16F722/3/4/6/7 CAP SENSOR HYSTERESIS, POWER MODE = MEDIUM



28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.20
Contact Width	b	0.23	0.30	0.35
Contact Length	L	0.50	0.55	0.70
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

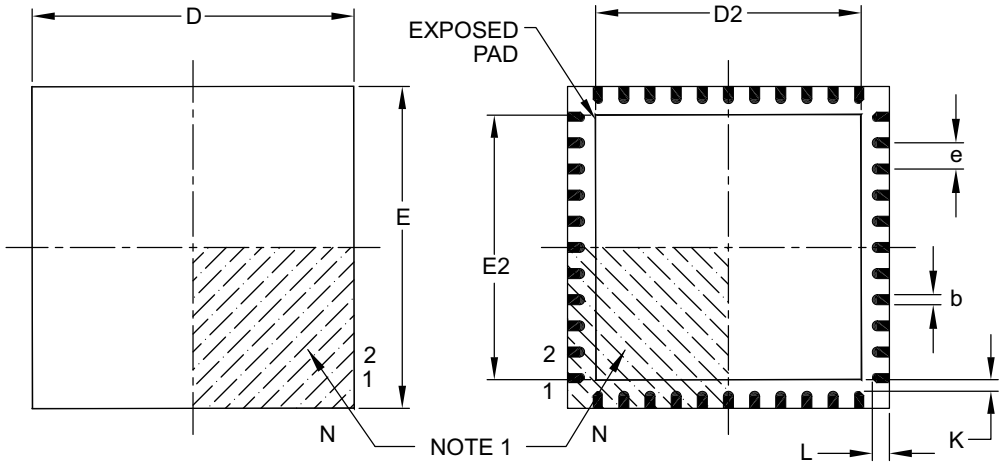
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

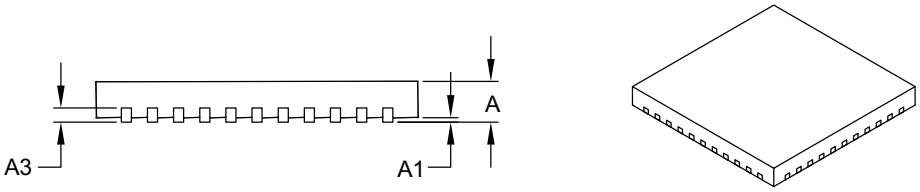
Microchip Technology Drawing C04-105B

44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW **BOTTOM VIEW**



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.30	6.45	6.80
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.30	6.45	6.80
Contact Width	b	0.25	0.30	0.38
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103B

APPENDIX A: DATA SHEET REVISION HISTORY

Revision A (12/2007)

Original release.

Revision B (08/2008)

Electrical Specification updates; Package Drawings; miscellaneous updates.

Revision C (04/2009)

Revised data sheet title; Revised Low-Power Features section; Revised Section 6.2.2.4 RA3/AN3/VREF; Revised Figure 16-8 Synchronous Reception.

Revision D (07/2009)

Removed the Preliminary Label; Updated the “Electrical Characteristics” section; Added charts in the “Char. Data” section; Deleted “Based 8-Bit CMOS” from title; Updated the “Special Microcontroller Features” section and the “Peripheral Features” section; Changed the title of the “Low Power Features” section into “Extreme Low-Power Management PIC16LF72X with nanoWatt XLP” and updated this section; Inserted new section – “Analog Features” (page 1); Changed the title of the “Peripheral Features” section into “Peripheral Highlights” and updated the section.

Revision E (10/2009)

Added paragraph to section 5.0 (LDO Voltage Regulator); Updated the Electrical Specifications section (Added another absolute Maximum Rating; Updated section 23.1 and Table 23-4); Updated the Pin Diagrams with the UQFN package; Updated Table 1, adding UQFN; Updated section 23.5 (Thermal Considerations); Updated the Packaging Information section adding the UQFN Package; Updated the Product Identification System section.

Revision F (12/2015)

Updated Table 2; Updated 23.1, 23.3 and 9.2.4 Sections; Updated Figure 23-9; Other minor corrections.

APPENDIX B: MIGRATING FROM OTHER PIC® DEVICES

This discusses some of the issues in migrating from other PIC® devices to the PIC16F72X family of devices.

B.1 PIC16F77 to PIC16F72X

TABLE B-1: FEATURE COMPARISON

Feature	PIC16F77	PIC16F727
Max. Operating Speed	20 MHz	20 MHz
Max. Program Memory (Words)	8K	8K
Max. SRAM (Bytes)	368	368
A/D Resolution	8-bit	8-bit
Timers (8/16-bit)	2/1	2/1
Oscillator Modes	4	8
Brown-out Reset	Y	Y
Internal Pull-ups	RB<7:0>	RB<7:0>
Interrupt-on-change	RB<7:4>	RB<7:0>
Comparator	0	0
USART	Y	Y
Extended WDT	N	N
Software Control Option of WDT/BOR	N	N
INTOSC Frequencies	None	500 kHz - 16 MHz
Clock Switching	N	N