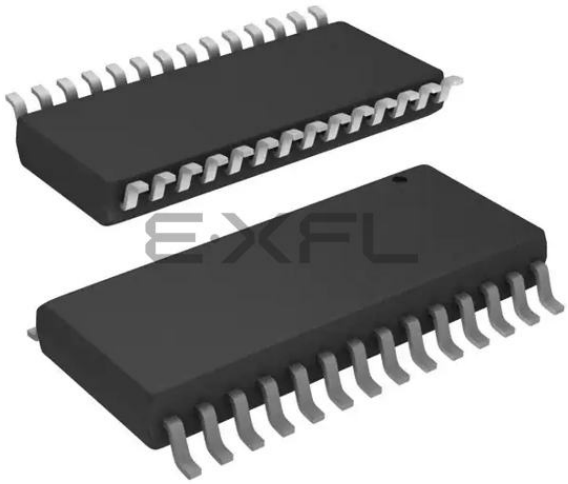

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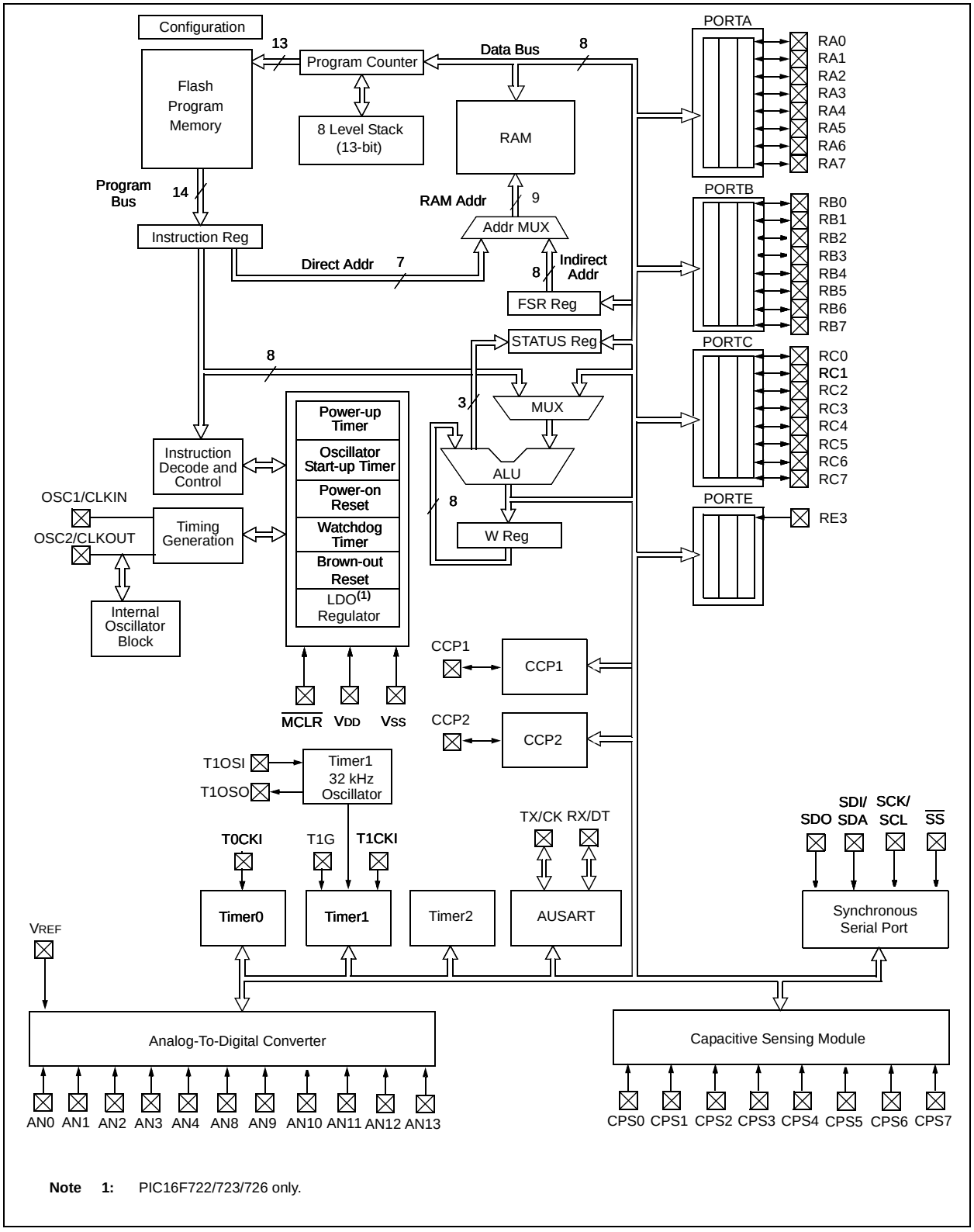
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf723-e-so

FIGURE 1-1: PIC16F722/723/726/PIC16LF722/723/726 BLOCK DIAGRAM



Note 1: PIC16F722/723/726 only.

5.0 LOW DROPOUT (LDO) VOLTAGE REGULATOR

The PIC16F722/3/4/6/7 devices differ from the PIC16LF722/3/4/6/7 devices due to an internal Low Dropout (LDO) voltage regulator. The PIC16F722/3/4/6/7 devices contain an internal LDO, while the PIC16LF722/3/4/6/7 ones do not.

The lithography of the die allows a maximum operating voltage of 3.6V on the internal digital logic. In order to continue to support 5.0V designs, a LDO voltage regulator is integrated on the die. The LDO voltage regulator allows for the internal digital logic to operate at 3.2V, while I/O's operate at 5.0V (V_{DD}).

The LDO voltage regulator requires an external bypass capacitor for stability. One of three pins, denoted as V_{CAP}, can be configured for the external bypass capacitor. It is recommended that the capacitor be a ceramic cap between 0.1 to 1.0 µF. The V_{CAP} pin is not intended to supply power to external loads. An external voltage regulator should be used if this functionality is required. In addition, external devices should not supply power to the V_{CAP} pin.

On power-up, the external capacitor will look like a large load on the LDO voltage regulator. To prevent erroneous operation, the device is held in Reset while a constant current source charges the external capacitor. After the cap is fully charged, the device is released from Reset. For more information, refer to **Section 23.0 "Electrical Specifications"**.

See Configuration Word 2 register (Register 8-2) for V_{CAP} enable bits.

6.2 PORTA and the TRISA Registers

PORTA is a 8-bit wide, bidirectional port. The corresponding data direction register is TRISA (Register 6-3). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., disable the output driver). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). Example 6-1 shows how to initialize PORTA.

Reading the PORTA register (Register 6-2) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch.

The TRISA register (Register 6-3) controls the PORTA pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

Note:	The ANSELA register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

EXAMPLE 6-1: INITIALIZING PORTA

```
BANKSEL PORTA       ;
CLRF    PORTA       ;Init PORTA
BANKSEL ANSELA      ;
CLRF    ANSELA      ;digital I/O
BANKSEL TRISA       ;
MOVLW   0Ch         ;Set RA<3:2> as inputs
MOVWF   TRISA       ;and set RA<7:4,1:0>
                    ;as outputs
```

REGISTER 6-2: PORTA: PORTA REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **RA<7:0>**: PORTA I/O Pin bit
1 = Port pin is > V_{IH}
0 = Port pin is < V_{IL}

REGISTER 6-3: TRISA: PORTA TRI-STATE REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **TRISA<7:0>:** PORTA Tri-State Control bit
1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

6.2.1 ANSELA REGISTER

The ANSELA register (Register 6-4) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no affect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

REGISTER 6-4: ANSELA: PORTA ANALOG SELECT REGISTER

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **ANSA<5:0>**: Analog Select between Analog or Digital Function on pins RA<5:0>, respectively

0 = Digital I/O. Pin is assigned to port or Digital special function.

1 = Analog input. Pin is assigned as analog input**(1)**. Digital Input buffer disabled.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 6-13: TRISD: PORTD TRI-STATE REGISTER(1)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **TRISD<7:0>:** PORTD Tri-State Control bits
1 = PORTD pin configured as an input (tri-stated)
0 = PORTD pin configured as an output

Note 1: TRISD is not implemented on PIC16F722/723/726/PIC16LF722/723/726 devices, read as '0'.

REGISTER 6-14: ANSELD: PORTD ANALOG SELECT REGISTER(2)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANSD7	ANSD6	ANSD5	ANSD4	ANSD3	ANSD2	ANSD1	ANSD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ANSD<7:0>**: Analog Select between Analog or Digital Function on Pins RD<7:0>, respectively
0 = Digital I/O. Pin is assigned to port or Digital special function.
1 = Analog input. Pin is assigned as analog input(1). Digital Input buffer disabled.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.
2: ANSELD register is not implemented on the PIC16F722/723/726/PIC16LF722/723/726. Read as '0'.

Note: PORTD is available on PIC16F724/LF724 and PIC16F727/LF727 only.

6.5.2 RD0/CPS8

Figure 6-21 shows the diagram for these pins. They are configurable to function as one of the following:

- a general purpose I/O
- a capacitive sensing input

6.5.3 RD1/CPS9

Figure 6-21 shows the diagram for these pins. They are configurable to function as one of the following:

- a general purpose I/O
- a capacitive sensing input

6.5.4 RD2/CPS10

Figure 6-21 shows the diagram for these pins. They are configurable to function as one of the following:

- a general purpose I/O
- a capacitive sensing input

6.5.5 RD3/CPS11

Figure 6-21 shows the diagram for these pins. They are configurable to function as one of the following:

- a general purpose I/O
- a capacitive sensing input

REGISTER 6-15: PORTE: PORTE REGISTER

U-0	U-0	U-0	U-0	R-x	R/W-x	R/W-x	R/W-x
—	—	—	—	RE3	RE2(1)	RE1(1)	RE0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented**: Read as '0'

bit 3-0 **RE<3:0>**: PORTE I/O Pin bits(1)
1 = Port pin is > VIH
0 = Port pin is < VIL

Note 1: RE<2:0> are not implemented on the PIC16F722/723/726/PIC16LF722/723/726. Read as '0'.

REGISTER 6-16: TRISE: PORTE TRI-STATE REGISTER

U-0	U-0	U-0	U-0	R-1	R/W-1	R/W-1	R/W-1
—	—	—	—	TRISE3	TRISE2(1)	TRISE1(1)	TRISE0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented**: Read as '0'

bit 3 **TRISE3:** RE3 Port Tri-state Control bit
This bit is always '1' as RE3 is an input only

bit 2-0 **TRISE<2:0>:** RE<2:0> Tri-State Control bits(1)
1 = PORTE pin configured as an input (tri-stated)
0 = PORTE pin configured as an output

Note 1: TRISE<2:0> are not implemented on the PIC16F722/723/726/PIC16LF722/723/726. Read as '0'.

6.6.1 RE0/AN5(1)

Figure 6-22 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC

Note 1:	RE0/AN5 is available on PIC16F724/LF724 and PIC16F727/LF727 only.

6.6.2 RE1/AN6(1)

Figure 6-22 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC

Note 1:	RE0/AN5 is available on PIC16F724/LF724 and PIC16F727/LF727 only.

6.6.3 RE2/AN7(1)

Figure 6-22 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC

Note 1:	RE0/AN5 is available on PIC16F724/LF724 and PIC16F727/LF727 only.

6.6.4 RE3/$\overline{\text{MCLR}}$/VPP

Figure 6-23 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose input
- as Master Clear Reset with weak pull-up
- a programming voltage reference input

REGISTER 8-1: CONFIG1: CONFIGURATION WORD REGISTER 1 (CONTINUED)

bit 4 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
111 = RC oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, RC on RA7/OSC1/CLKIN
110 = RCIO oscillator: I/O function on RA6/OSC2/CLKOUT pin, RC on RA7/OSC1/CLKIN
101 = INTOSC oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN
100 = INTOSCIO oscillator: I/O function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN
011 = EC: I/O function on RA6/OSC2/CLKOUT pin, CLKIN on RA7/OSC1/CLKIN
010 = HS oscillator: High-speed crystal/resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN
001 = XT oscillator: Crystal/resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN
000 = LP oscillator: Low-power crystal on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
2: The entire program memory will be erased when the code protection is turned off.
3: When $\overline{\text{MCLR}}$ is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.
4: MPLAB® X IDE masks unimplemented Configuration bits to '0'.

REGISTER 8-2: CONFIG2: CONFIGURATION WORD REGISTER 2

		U-1(1)	U-1(1)	U-1(1)	U-1(1)	U-1(1)	U-1(1)
—	—	—	—	—	—	—	—
bit 15							bit 8

U-1(1)	U-1(1)	R/P-1	R/P-1	U-1(1)	U-1(1)	U-1(1)	U-1(1)
—	—	VCAPEN1	VCAPEN0	—	—	—	—
bit 7							bit 0

Legend:	P = Programmable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

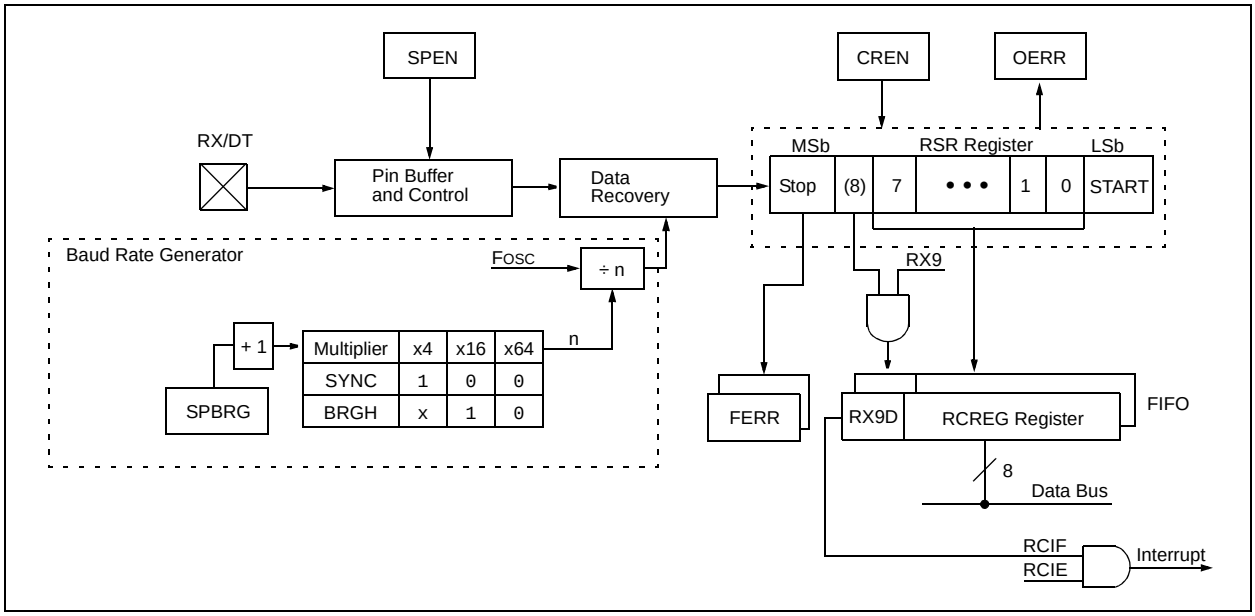
bit 13-6 **Unimplemented**: Read as '1'

bit 5-4 **VCAPEN<1:0>:** Voltage Regulator Capacitor Enable bits
For the PIC16LF72X:
These bits are ignored. All VCAP pin functions are disabled.
For the PIC16F72X:
00 = VCAP functionality is enabled on RA0
01 = VCAP functionality is enabled on RA5
10 = VCAP functionality is enabled on RA6
11 = All VCAP functions are disabled (not recommended)

bit 3-0 **Unimplemented**: Read as '1'

Note 1: MPLAB® X IDE masks unimplemented Configuration bits to '0'.

FIGURE 16-2: AUSART RECEIVE BLOCK DIAGRAM



The operation of the AUSART module is controlled through two registers:

- Transmit Status and Control (TXSTA)
- Receive Status and Control (RCSTA)

These registers are detailed in Register 16-1 and Register 16-2, respectively.

16.1 AUSART Asynchronous Mode

The AUSART transmits and receives data using the standard non-return-to-zero (NRZ) format. NRZ is implemented with two levels: a VOH Mark state which represents a '1' data bit, and a VOL Space state which represents a '0' data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port idles in the Mark state. Each character transmission consists of one Start bit followed by eight or nine data bits and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is 8 bits. Each transmitted bit persists for a period of 1/(Baud Rate). An on-chip dedicated 8-bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. Refer to Table 16-5 for examples of baud rate Configurations.

The AUSART transmits and receives the LSb first. The AUSART's transmitter and receiver are functionally independent, but share the same data format and baud rate. Parity is not supported by the hardware, but can be implemented in software and stored as the ninth data bit.

16.1.1 AUSART ASYNCHRONOUS TRANSMITTER

The AUSART transmitter block diagram is shown in Figure 16-1. The heart of the transmitter is the serial Transmit Shift Register (TSR), which is not directly accessible by software. The TSR obtains its data from the transmit buffer, which is the TXREG register.

16.1.1.1 Enabling the Transmitter

The AUSART transmitter is enabled for asynchronous operations by configuring the following three control bits:

- TXEN = 1
- SYNC = 0
- SPEN = 1

All other AUSART control bits are assumed to be in their default state.

Setting the TXEN bit of the TXSTA register enables the transmitter circuitry of the AUSART. Clearing the SYNC bit of the TXSTA register configures the AUSART for asynchronous operation. Setting the SPEN bit of the RCSTA register enables the AUSART and automatically configures the TX/CK I/O pin as an output.

Note 1: When the SPEN bit is set the RX/DT I/O pin is automatically configured as an input, regardless of the state of the corresponding TRIS bit and whether or not the AUSART receiver is enabled. The RX/DT pin data can be read via a normal PORT read but PORT latch data output is precluded.

2: The TXIF transmitter interrupt flag is set when the TXEN enable bit is set.

16.1.1.2 Transmitting Data

A transmission is initiated by writing a character to the TXREG register. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the TXREG until the Stop bit of the previous character has been transmitted. The pending character in the TXREG is then transferred to the TSR in one TCY immediately following the Stop bit transmission. The transmission of the Start bit, data bits and Stop bit sequence commences immediately following the transfer of the data to the TSR from the TXREG.

16.1.1.3 Transmit Interrupt Flag

The TXIF interrupt flag bit of the PIR1 register is set whenever the AUSART transmitter is enabled and no character is being held for transmission in the TXREG. In other words, the TXIF bit is only clear when the TSR is busy with a character and a new character has been queued for transmission in the TXREG. The TXIF flag bit is not cleared immediately upon writing TXREG. TXIF becomes valid in the second instruction cycle following the write execution. Polling TXIF immediately following the TXREG write will return invalid results. The TXIF bit is read-only, it cannot be set or cleared by software.

The TXIF interrupt can be enabled by setting the TXIE interrupt enable bit of the PIE1 register. However, the TXIF flag bit will be set whenever the TXREG is empty, regardless of the state of TXIE enable bit.

To use interrupts when transmitting data, set the TXIE bit only when there is more data to send. Clear the TXIE interrupt enable bit upon writing the last character of the transmission to the TXREG.

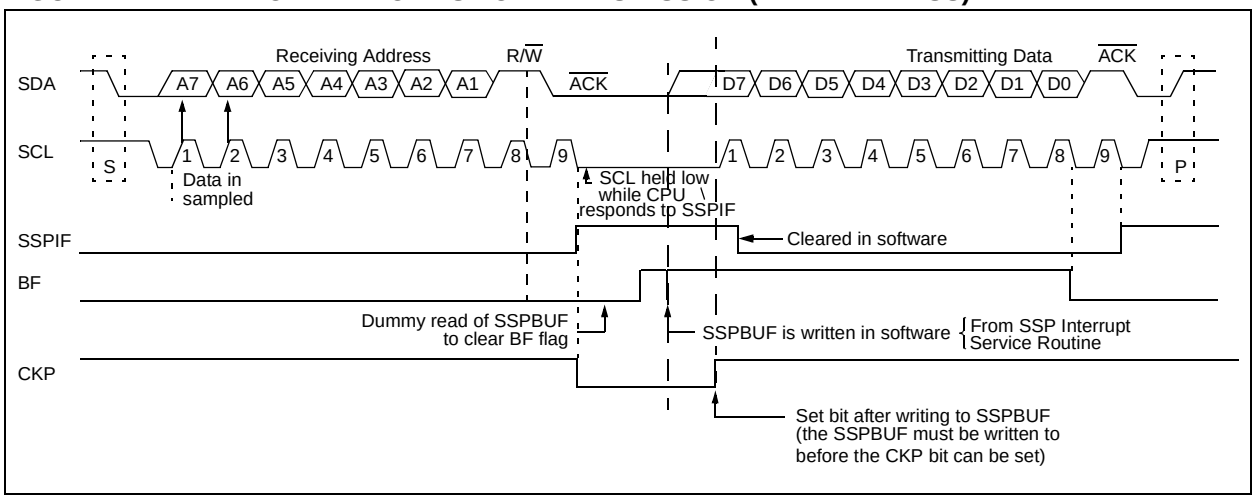
17.2.6 TRANSMISSION

When the R/$\overline{W}$ bit of the received address byte is set and an address match occurs, the R/$\overline{W}$ bit of the SSPSTAT register is set and the slave will respond to the master by reading out data. After the address match, an $\overline{ACK}$ pulse is generated by the slave hardware and the SCL pin is held low (clock is automatically stretched) until the slave is ready to respond. See **Section 17.2.7 "Clock Stretching"**. The data the slave will transmit must be loaded into the SSPBUF register, which sets the BF bit. The SCL line is released by setting the CKP bit of the SSPCON register.

An SSP interrupt is generated for each transferred data byte. The SSPIF flag bit of the PIR1 register initiates an SSP interrupt, and must be cleared by software before the next byte is transmitted. The BF bit of the SSPSTAT register is cleared on the falling edge of the eighth received clock pulse. The SSPIF flag bit is set on the falling edge of the ninth clock pulse.

Following the eighth falling clock edge, control of the SDA line is released back to the master so that the master can acknowledge or not acknowledge the response. If the master sends a not acknowledge, the slave's transmission is complete and the slave must monitor for the next Start condition. If the master acknowledges, control of the bus is returned to the slave to transmit another byte of data. Just as with the previous byte, the clock is stretched by the slave, data must be loaded into the SSPBUF and CKP must be set to release the clock line (SCL).

FIGURE 17-12: I^{2}C WAVEFORMS FOR TRANSMISSION (7-BIT ADDRESS)



18.0 PROGRAM MEMORY READ

The Flash program memory is readable during normal operation over the full VDD range of the device. To read data from Program Memory, five Special Function Registers (SFRs) are used:

- PMCON1
- PMDATL
- PMDATH
- PMADRL
- PMADRH

The value written to the PMADRH:PMADRL register pair determines which program memory location is read. The read operation will be initiated by setting the RD bit of the PMCON1 register. The program memory flash controller takes two instructions to complete the read, causing the second instruction after the setting the RD bit will be ignored. To avoid conflict with program execution, it is recommended that the two instructions following the setting of the RD bit are NOP. When the read completes, the result is placed in the PMDATLH:PMDATL register pair. Refer to Example 18-1 for sample code.

Note:	Code-protect does not effect the CPU from performing a read operation on the program memory. For more information, refer to **Section 8.2 “Code Protection”**.

EXAMPLE 18-1: PROGRAM MEMORY READ

```
                BANKSEL  PMADRL          ;
                MOVF     MS_PROG_ADDR, W;
                MOVWF    PMADRH          ;MS Byte of Program Address to read
                MOVF     LS_PROG_ADDR, W;
                MOVWF    PMADRL          ;LS Byte of Program Address to read
                BANKSEL  PMCON1          ;
Required        BSF      PMCON1, RD      ;Initiate Read
Sequence        NOP
                NOP                      ;Any instructions here are ignored as program
                                         ;memory is read in second cycle after BSF
                BANKSEL  PMDATL          ;
                MOVF     PMDATL, W       ;W = LS Byte of Program Memory Read
                MOVWF    LOWPMBYTE       ;
                MOVF     PMDATH, W       ;W = MS Byte of Program Memory Read
                MOVWF    HIGHPMBYTE      ;
```

TABLE 21-2: PIC16(L)F722/3/4/6/7 INSTRUCTION SET

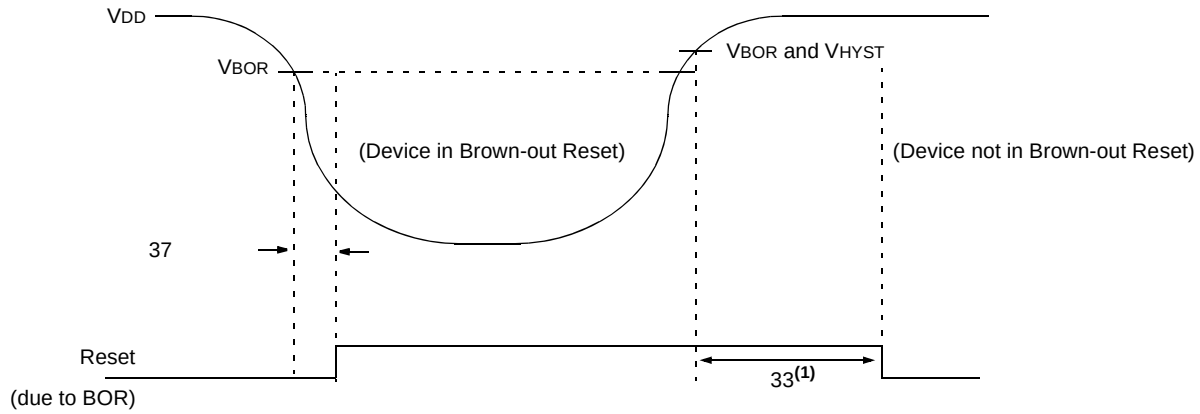
Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb			LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C, DC, Z	**1, 2**
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	**1, 2**
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	**2**
CLRW	–	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	**1, 2**
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	**1, 2**
DECFSZ	f, d	Decrement f, Skip if 0	1**(2)**	00	1011	dfff	ffff		**1, 2, 3**
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	**1, 2**
INCFSZ	f, d	Increment f, Skip if 0	1**(2)**	00	1111	dfff	ffff		**1, 2, 3**
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	**1, 2**
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	**1, 2**
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	–	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	**1, 2**
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	**1, 2**
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C, DC, Z	**1, 2**
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		**1, 2**
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	**1, 2**
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		**1, 2**
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		**1, 2**
BTFSC	f, b	Bit Test f, Skip if Clear	1 **(2)**	01	10bb	bfff	ffff		**3**
BTFSS	f, b	Bit Test f, Skip if Set	1 **(2)**	01	11bb	bfff	ffff		**3**
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C, DC, Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call Subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	–	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}$, $\overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	–	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	–	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	–	Go into Standby mode	1	00	0000	0110	0011	$\overline{TO}$, $\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C, DC, Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTA, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

3: If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

FIGURE 23-9: BROWN-OUT RESET TIMING AND CHARACTERISTICS



Note 1: 64 ms delay only if $\overline{\text{PWRTE}}$ bit in the Configuration Word register is programmed to '0'.

TABLE 23-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET PARAMETERS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
30	TMCL	$\overline{MCLR}$ Pulse Width (low)	2 5	— —	— —	µs µs	VDD = 3.3-5V, -40°C to +85°C VDD = 3.3-5V
31	TWDTLP	Low Power Watchdog Timer Time-out Period (No Prescaler)	10	18	27	ms	VDD = 3.3V-5V
32	TOST	Oscillator Start-up Timer Period(1), (2)	—	1024	—	Tosc	**(Note 3)**
33*	TPWRT	Power-up Timer Period, $\overline{PWRTE}$ = 0	40	65	140	ms	
34*	TIOZ	I/O high-impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset	—	—	2.0	µs	
35	VBOR	Brown-out Reset Voltage	2.38 1.80	2.5 1.9	2.73 2.11	V	BORV=2.5V BORV=1.9V
36*	VHYST	Brown-out Reset Hysteresis	0	25	50	mV	-40°C to +85°C
37*	TBORDC	Brown-out Reset DC Response Time	1	3	5 10	µs	VDD ≤ VBOR, -40°C to +85°C VDD ≤ VBOR

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: By design.

3: Period of the slower clock.

4: To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

FIGURE 23-10: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

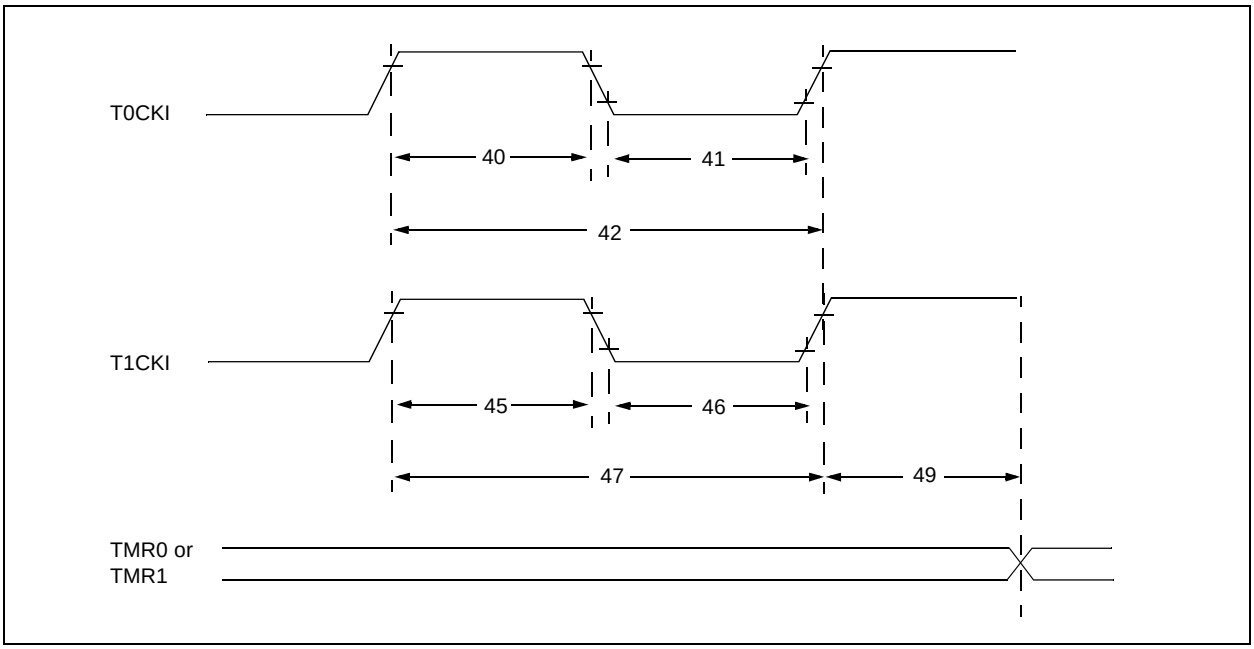


TABLE 23-14: CAP SENSE OSCILLATOR SPECIFICATIONS

Param. No.	Symbol	Characteristic		Min.	Typ†	Max.	Units	Conditions
CS01	ISRC	Current Source	High	—	-5.8	-6	µA	-40, -85°C
			Medium	—	-1.1	-3.2	µA	
			Low	—	-0.2	-0.9	µA	
CS02	ISNK	Current Sink	High	—	6.6	6	µA	-40, -85°C
			Medium	—	1.3	3.2	µA	
			Low	—	0.24	0.9	µA	
CS03	VCHYST	Cap Hysteresis	High	—	525	—	mV	VCTH-VCTL
			Medium	—	375	—	mV	
			Low	—	280	—	mV	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 23-22: CAP SENSE OSCILLATOR

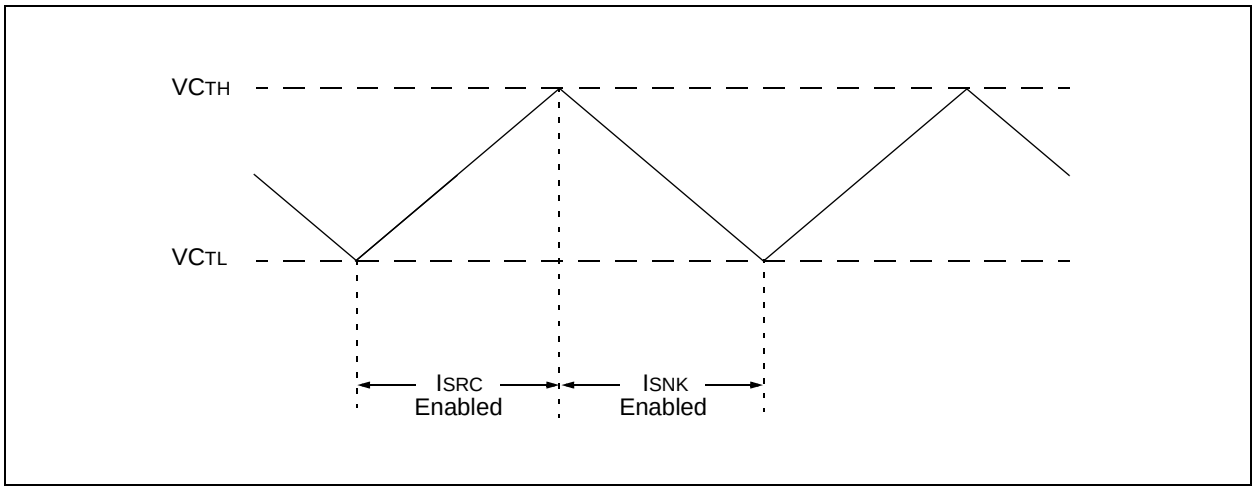


FIGURE 24-41: PIC16F722/3/4/6/7 T1OSC 32 KHZ IPD VS. VDD, VCAP = 0.1 µF

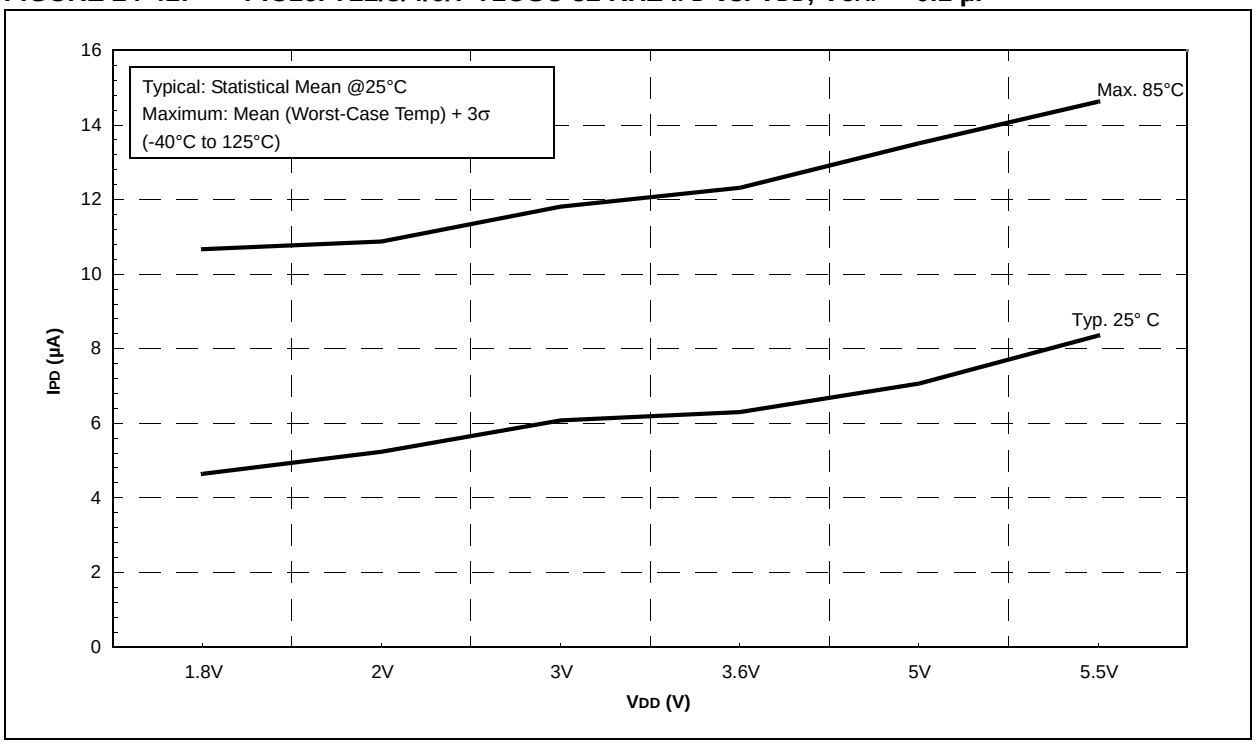


FIGURE 24-42: PIC16LF722/3/4/6/7 T1OSC 32 kHz IPD VS. VDD

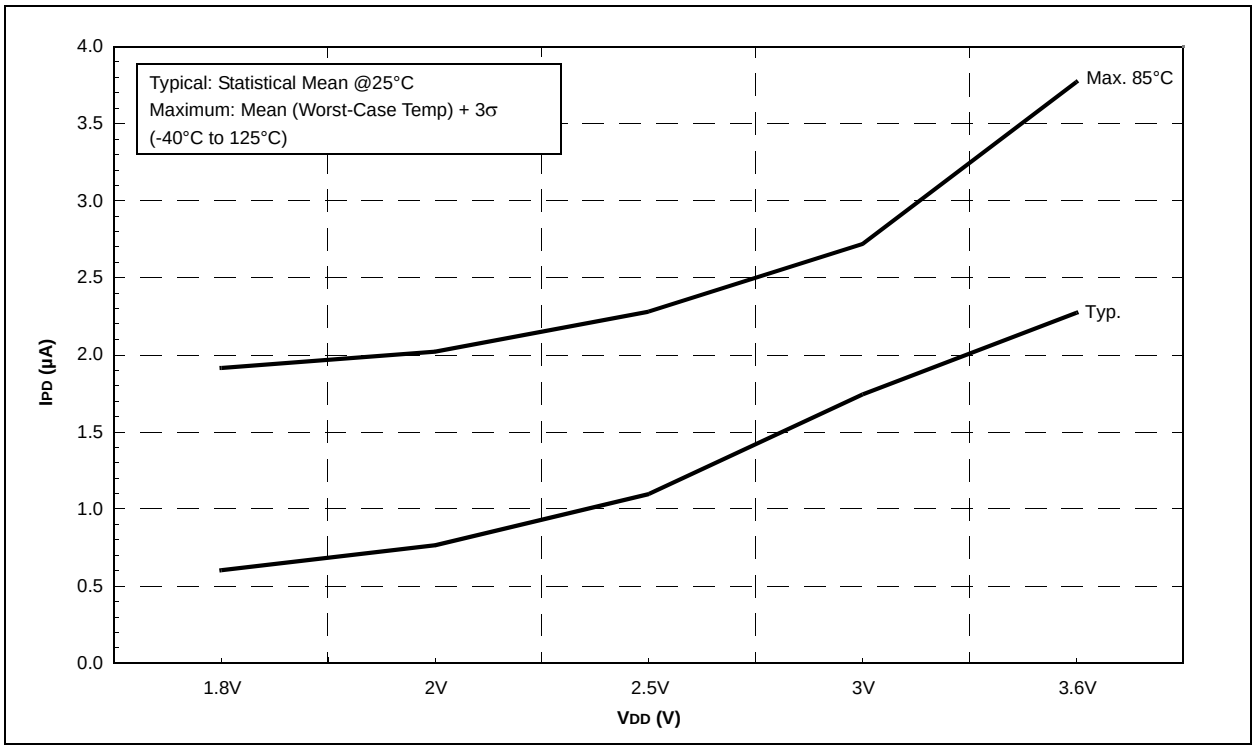


FIGURE 24-57: V_{OL} vs. I_{OL} OVER TEMPERATURE, V_{DD} = 1.8V

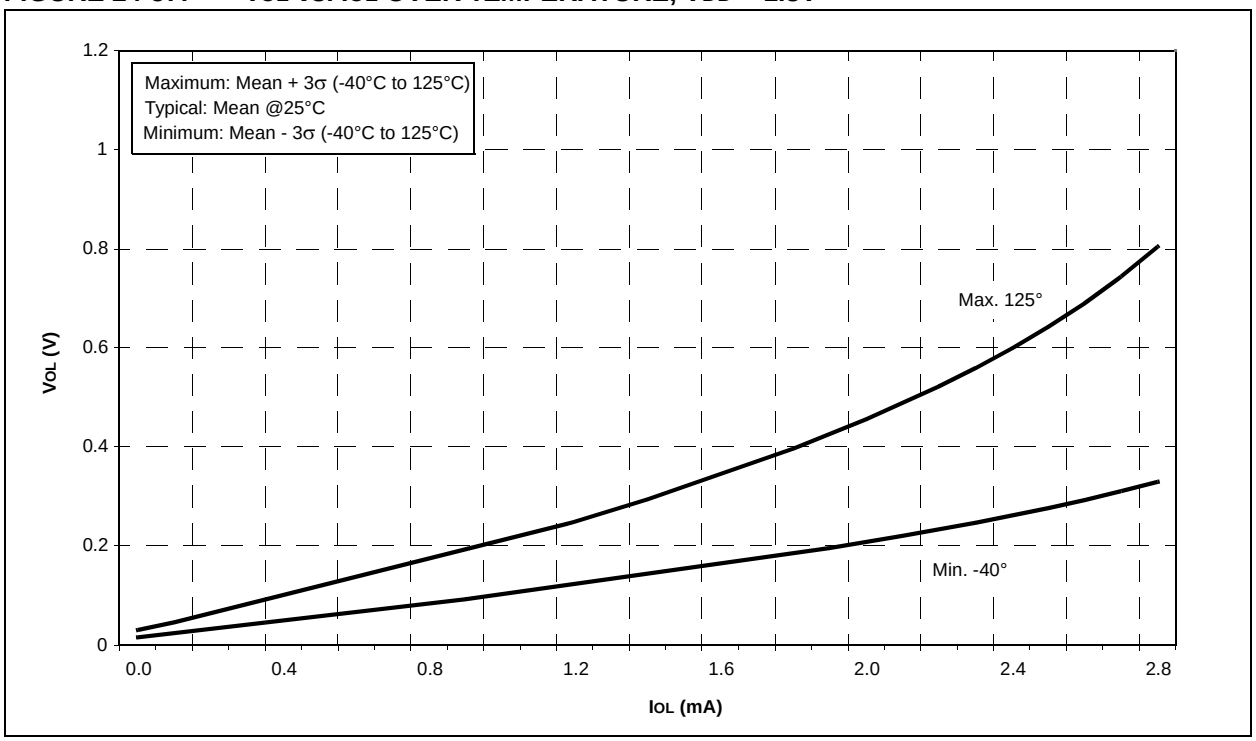
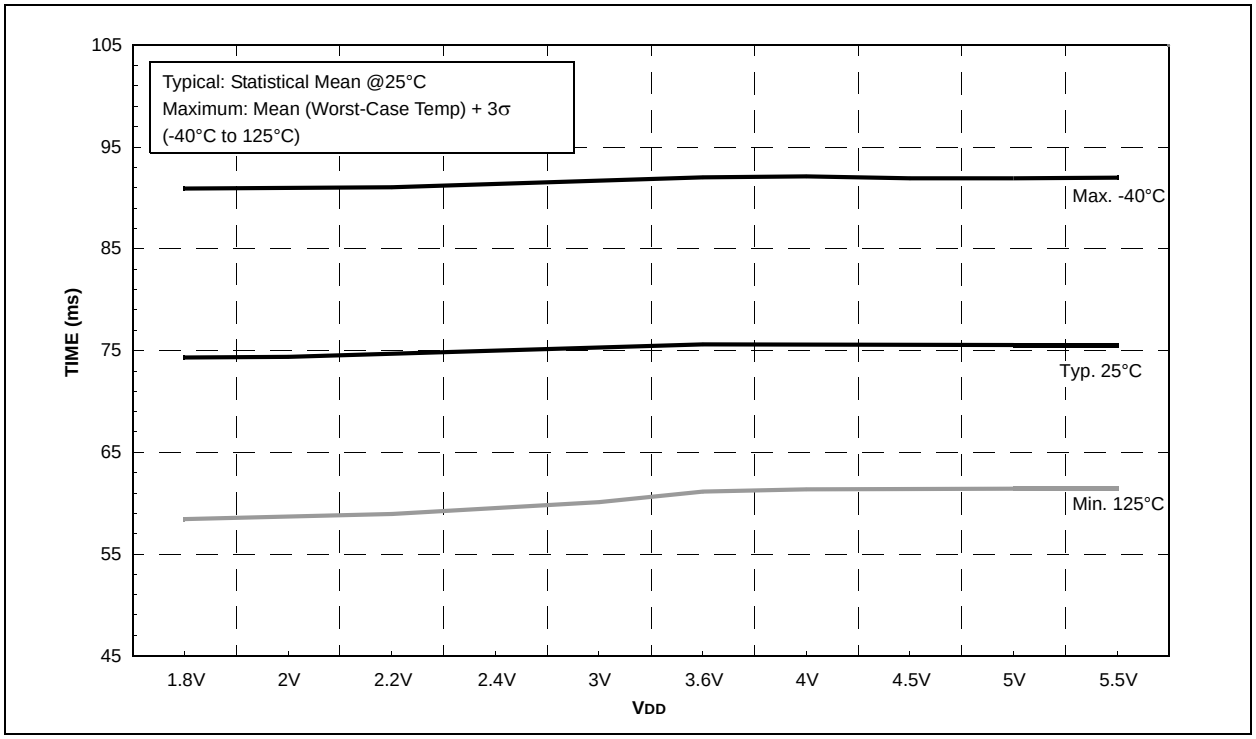


FIGURE 24-58: PIC16F722/3/4/6/7 PWRT PERIOD

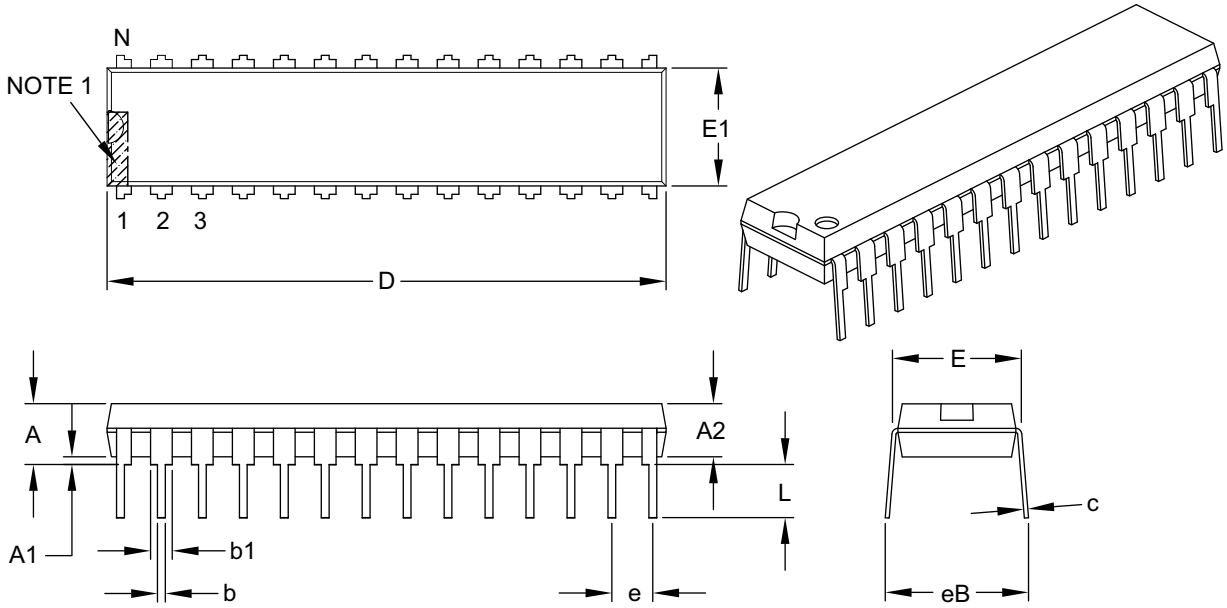


25.2 Package Details

The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

APPENDIX A: DATA SHEET REVISION HISTORY

Revision A (12/2007)

Original release.

Revision B (08/2008)

Electrical Specification updates; Package Drawings; miscellaneous updates.

Revision C (04/2009)

Revised data sheet title; Revised Low-Power Features section; Revised Section 6.2.2.4 RA3/AN3/VREF; Revised Figure 16-8 Synchronous Reception.

Revision D (07/2009)

Removed the Preliminary Label; Updated the “Electrical Characteristics” section; Added charts in the “Char. Data” section; Deleted “Based 8-Bit CMOS” from title; Updated the “Special Microcontroller Features” section and the “Peripheral Features” section; Changed the title of the “Low Power Features” section into “Extreme Low-Power Management PIC16LF72X with nanoWatt XLP” and updated this section; Inserted new section – “Analog Features” (page 1); Changed the title of the “Peripheral Features” section into “Peripheral Highlights” and updated the section.

Revision E (10/2009)

Added paragraph to section 5.0 (LDO Voltage Regulator); Updated the Electrical Specifications section (Added another absolute Maximum Rating; Updated section 23.1 and Table 23-4); Updated the Pin Diagrams with the UQFN package; Updated Table 1, adding UQFN; Updated section 23.5 (Thermal Considerations); Updated the Packaging Information section adding the UQFN Package; Updated the Product Identification System section.

Revision F (12/2015)

Updated Table 2; Updated 23.1, 23.3 and 9.2.4 Sections; Updated Figure 23-9; Other minor corrections.

APPENDIX B: MIGRATING FROM OTHER PIC® DEVICES

This discusses some of the issues in migrating from other PIC® devices to the PIC16F72X family of devices.

B.1 PIC16F77 to PIC16F72X

TABLE B-1: FEATURE COMPARISON

Feature	PIC16F77	PIC16F727
Max. Operating Speed	20 MHz	20 MHz
Max. Program Memory (Words)	8K	8K
Max. SRAM (Bytes)	368	368
A/D Resolution	8-bit	8-bit
Timers (8/16-bit)	2/1	2/1
Oscillator Modes	4	8
Brown-out Reset	Y	Y
Internal Pull-ups	RB<7:0>	RB<7:0>
Interrupt-on-change	RB<7:4>	RB<7:0>
Comparator	0	0
USART	Y	Y
Extended WDT	N	N
Software Control Option of WDT/BOR	N	N
INTOSC Frequencies	None	500 kHz - 16 MHz
Clock Switching	N	N