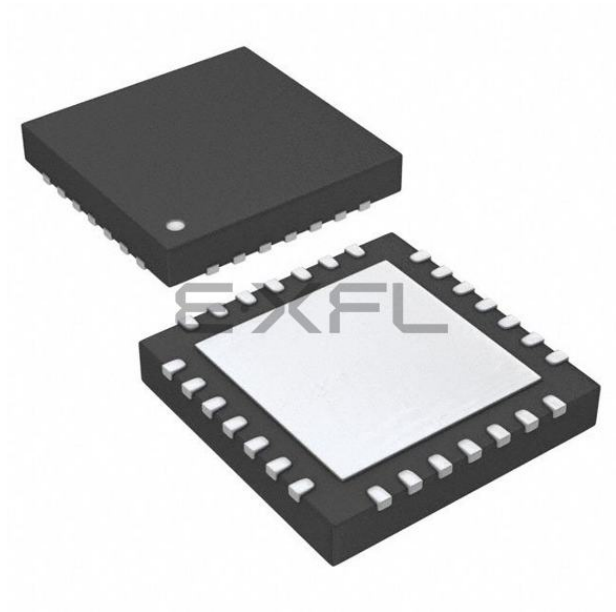

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf723-i-ml

PIC16(L)F72X Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data SRAM (bytes)	High-Endurance Flash Memory (bytes)	I/O's(2)	8-bit ADC (ch)	CapSense (ch)	Timers (8/16-bit)	AUSART	SSP (I^2C/SPI)	CCP	Debug(1)	XLP
PIC16(L)F707	(1)	8192	363	0	36	14	32	4/2	1	1	2	I	Y
PIC16(L)F720	(2)	2048	128	128	18	12	—	2/1	1	1	1	I	Y
PIC16(L)F721	(2)	4096	256	128	18	12	—	2/1	1	1	1	I	Y
PIC16(L)F722	(4)	2048	128	0	25	11	8	2/1	1	1	2	I	Y
PIC16(L)F722A	(3)	2048	128	0	25	11	8	2/1	1	1	2	I	Y
PIC16(L)F723	(4)	4096	192	0	25	11	8	2/1	1	1	2	I	Y
PIC16(L)F723A	(3)	4096	192	0	25	11	8	2/1	1	1	2	I	Y
PIC16(L)F724	(4)	4096	192	0	36	14	16	2/1	1	1	2	I	Y
PIC16(L)F726	(4)	8192	368	0	25	11	8	2/1	1	1	2	I	Y
PIC16(L)F727	(4)	8192	368	0	36	14	16	2/1	1	1	2	I	Y

Note 1: I - Debugging, Integrated on Chip; H - Debugging, Requires Debug Header.

2: One pin is input-only.

Data Sheet Index: (Unshaded devices are described in this document.)

1: DS41418 PIC16(L)F707 Data Sheet, 40/44-Pin Flash, 8-bit Microcontrollers

2: DS41430 PIC16(L)F720/721 Data Sheet, 20-Pin Flash, 8-bit Microcontrollers

3: DS41417 PIC16(L)F722A/723A Data Sheet, 28-Pin Flash, 8-bit Microcontrollers

4: DS41341 PIC16(L)F72X Data Sheet, 28/40/44-Pin Flash, 8-bit Microcontrollers

2.2.2.3 PCON Register

The Power Control (PCON) register contains flag bits (refer to Table 3-2) to differentiate between a:

- Power-on Reset ($\overline{POR}$)
- Brown-out Reset ($\overline{BOR}$)
- Watchdog Timer Reset (WDT)
- External $\overline{MCLR}$ Reset

The PCON register also controls the software enable of the BOR.

The PCON register bits are shown in Register 2-3.

REGISTER 2-3: PCON: POWER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-q	R/W-q
—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown
q = Value depends on condition			

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **$\overline{POR}$:** Power-on Reset Status bit
- 1 = No Power-on Reset occurred
- 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit
- 1 = No Brown-out Reset occurred
- 0 = A Brown-out Reset occurred (must be set in software after a Power-on Reset or Brown-out Reset occurs)

Note 1: Set BOREN<1:0> = 01 in the Configuration Word register for this bit to control the $\overline{BOR}$.

TABLE 3-4: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset/ Brown-out Reset(1)	$\overline{\text{MCLR}}$ Reset/ WDT Reset	Wake-up from Sleep through Interrupt/Time out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h/80h/ 100h/180h	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMR0	01h/101h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h/ 102h/182h	0000 0000	0000 0000	PC + 1(3)
STATUS	03h/83h/ 103h/183h	0001 1xxx	000q quuu(4)	uuuq quuu(4)
FSR	04h/84h/ 104h/184h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	xxxx xxxx	xxxx xxxx	uuuu uuuu
PORTB	06h	xxxx xxxx	xxxx xxxx	uuuu uuuu
PORTC	07h	xxxx xxxx	xxxx xxxx	uuuu uuuu
PORTD(6)	08h	xxxx xxxx	xxxx xxxx	uuuu uuuu
PORTE	09h	---- xxxx	---- xxxx	---- uuuu
PCLATH	0Ah/8Ah/ 10Ah/18Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh/8Bh/ 10Bh/18Bh	0000 000x	0000 000x	uuuu uuuu(2)
PIR1	0Ch	0000 0000	0000 0000	uuuu uuuu(2)
PIR2	0Dh	---- ---0	---- ---0	---- ---u
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	10h	0000 00-0	uuuu uu-u	uuuu uu-u
TMR2	11h	0000 0000	0000 0000	uuuu uuuu
T2CON	12h	-000 0000	-000 0000	-uuu uuuu
SSPBUF	13h	xxxx xxxx	xxxx xxxx	uuuu uuuu
SSPCON	14h	0000 0000	0000 0000	uuuu uuuu
CCPR1L	15h	xxxx xxxx	xxxx xxxx	uuuu uuuu
CCPR1H	16h	xxxx xxxx	xxxx xxxx	uuuu uuuu
CCP1CON	17h	--00 0000	--00 0000	--uu uuuu
RCSTA	18h	0000 000x	0000 000x	uuuu uuuu
TXREG	19h	0000 0000	0000 0000	uuuu uuuu
RCREG	1Ah	0000 0000	0000 0000	uuuu uuuu
CCPR2L	1Bh	xxxx xxxx	xxxx xxxx	uuuu uuuu
CCPR2H	1Ch	xxxx xxxx	xxxx xxxx	uuuu uuuu
CCP2CON	1Dh	--00 0000	--00 0000	--uu uuuu
ADRES	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	1Fh	--00 0000	--00 0000	--uu uuuu
OPTION_REG	81h/181h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	1111 1111	1111 1111	uuuu uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
TRISC	87h	1111 1111	1111 1111	uuuu uuuu
TRISD(6)	88h	1111 1111	1111 1111	uuuu uuuu
TRISE	89h	---- 1111	---- 1111	---- uuuu
PIE1	8Ch	0000 0000	0000 0000	uuuu uuuu
PIE2	8Dh	---- ---0	---- ---0	---- ---u

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 and PIR2 will be affected (to cause wake-up).

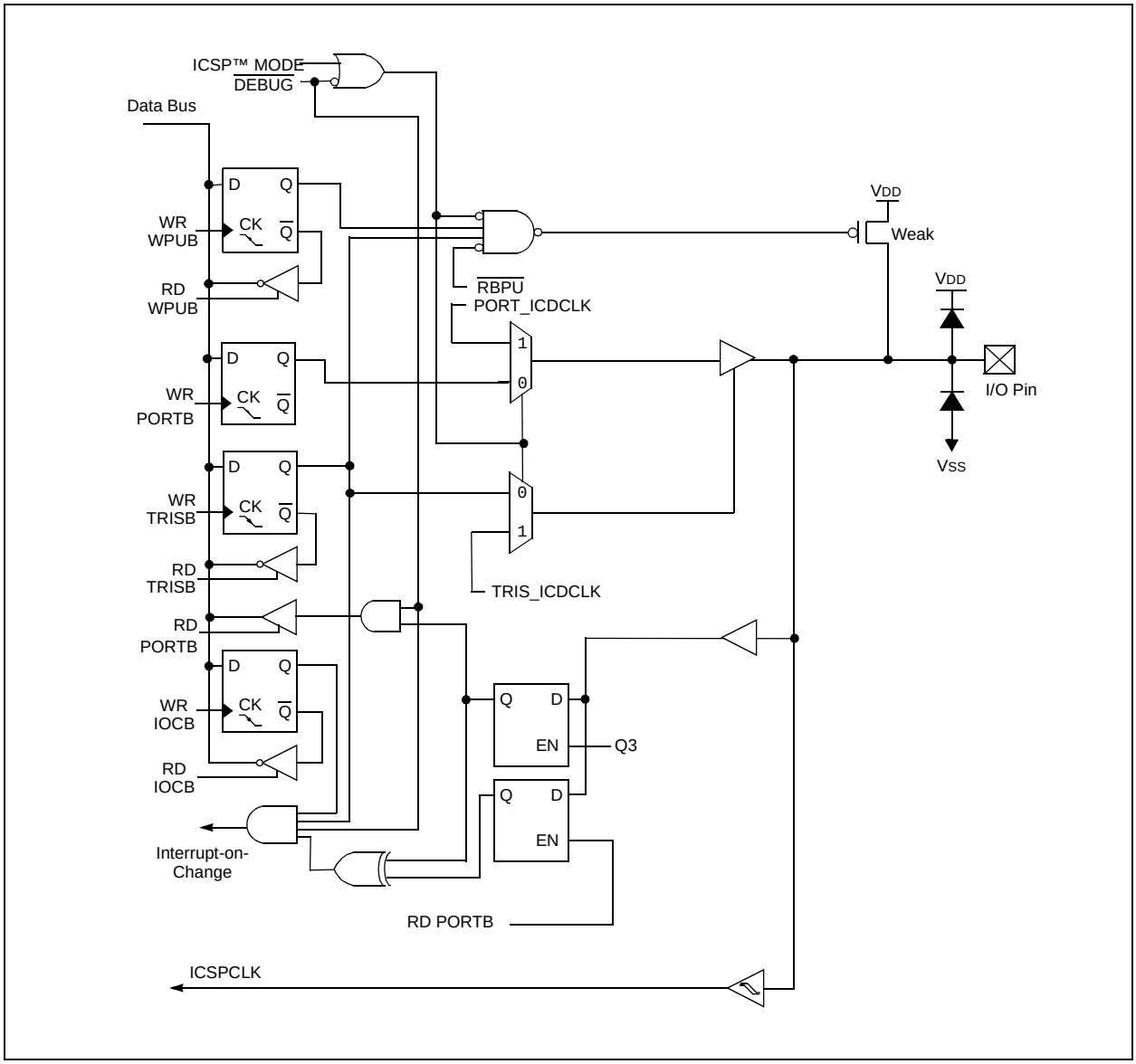
3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 3-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

6: PIC16F724/727/PIC16LF724/727 only.

FIGURE 6-11: BLOCK DIAGRAM OF RB6



7.0 OSCILLATOR MODULE

7.1 Overview

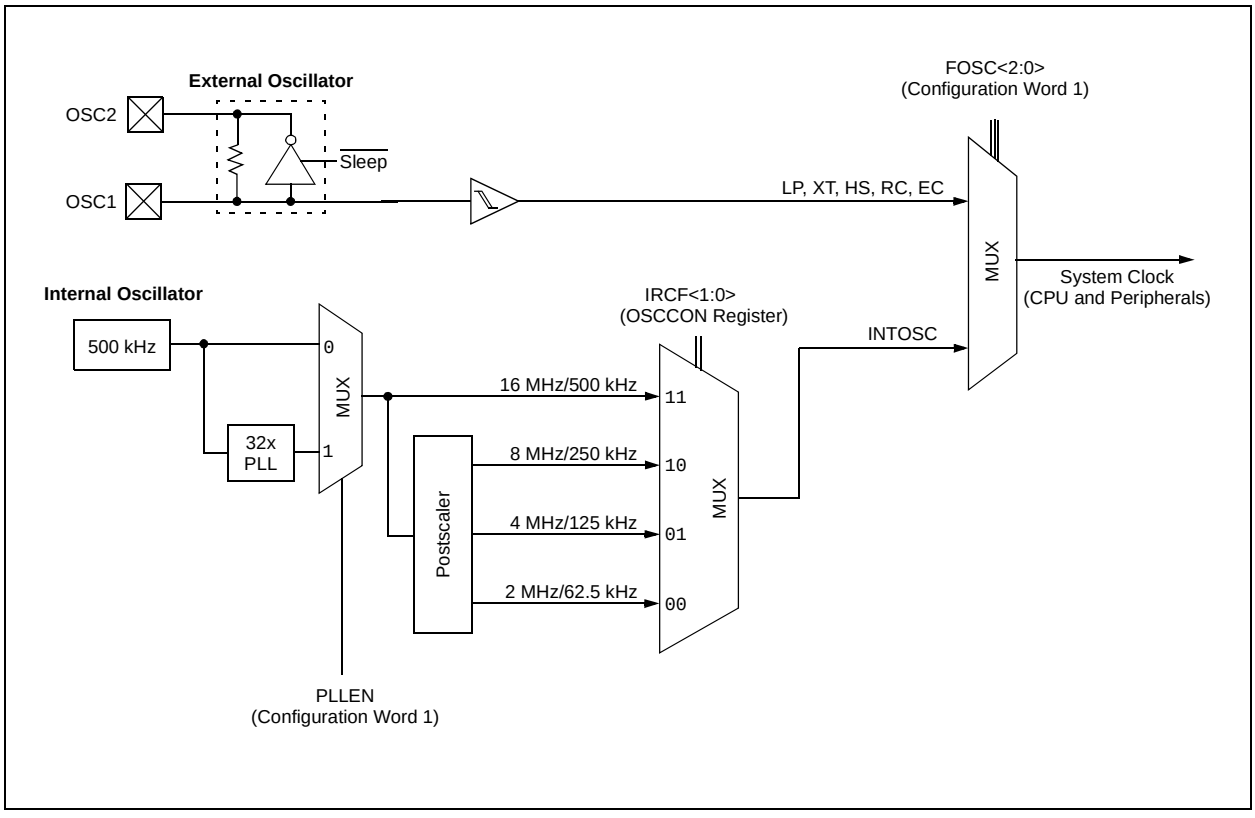
The oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 7-1 illustrates a block diagram of the oscillator module.

Clock sources can be configured from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system can be configured to use an internal calibrated high-frequency oscillator as clock source, with a choice of selectable speeds via software.

Clock source modes are configured by the FOSC bits in Configuration Word 1 (CONFIG1). The oscillator module can be configured for one of eight modes of operation.

1. RC – External Resistor-Capacitor (RC) with FOSC/4 output on OSC2/CLKOUT.
2. RCIO – External Resistor-Capacitor (RC) with I/O on OSC2/CLKOUT.
3. INTOSC – Internal oscillator with FOSC/4 output on OSC2 and I/O on OSC1/CLKIN.
4. INTOSCIO – Internal oscillator with I/O on OSC1/CLKIN and OSC2/CLKOUT.
5. EC – External clock with I/O on OSC2/CLKOUT.
6. HS – High Gain Crystal or Ceramic Resonator mode.
7. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode.
8. LP – Low-Power Crystal mode.

FIGURE 7-1: SIMPLIFIED PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



REGISTER 9-2: ADCON1: A/D CONTROL REGISTER 1

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
—	ADCS2	ADCS1	ADCS0	—	—	ADREF1	ADREF0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **ADCS<2:0>:** A/D Conversion Clock Select bits
000 = FOSC/2
001 = FOSC/8
010 = FOSC/32
011 = FRC (clock supplied from a dedicated RC oscillator)
100 = FOSC/4
101 = FOSC/16
110 = FOSC/64
111 = FRC (clock supplied from a dedicated RC oscillator)

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1-0 **ADREF<1:0>:** Voltage Reference Configuration bits
0x = VREF is connected to VDD
10 = VREF is connected to external VREF (RA3/AN3)
11 = VREF is connected to internal Fixed Voltage Reference

REGISTER 9-3: ADRES: ADC RESULT REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
ADRES7	ADRES6	ADRES5	ADRES4	ADRES3	ADRES2	ADRES1	ADRES0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **ADRES<7:0>**: ADC Result Register bits
8-bit conversion result.

15.2 Compare Mode

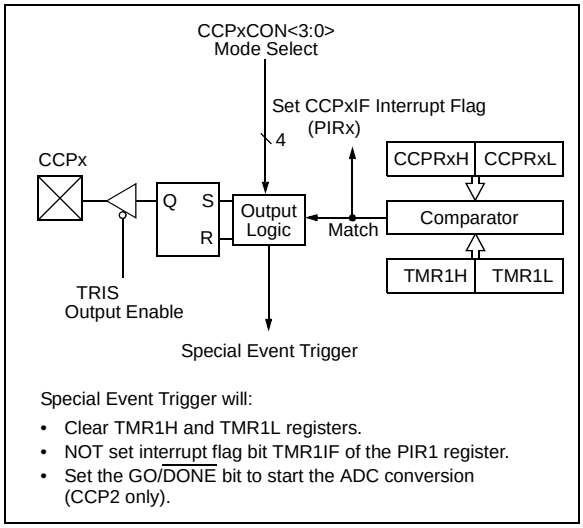
In Compare mode, the 16-bit CCPRx register value is constantly compared against the TMR1 register pair value. When a match occurs, the CCPx module may:

- Toggle the CCPx output
- Set the CCPx output
- Clear the CCPx output
- Generate a Special Event Trigger
- Generate a Software Interrupt

The action on the pin is based on the value of the CCPxM<3:0> control bits of the CCPxCON register.

All Compare modes can generate an interrupt.

FIGURE 15-2: COMPARE MODE OPERATION BLOCK DIAGRAM



15.2.1 CCPx PIN CONFIGURATION

The user must configure the CCPx pin as an output by clearing the associated TRIS bit.

Either RC1 or RB3 can be selected as the CCP2 pin. Refer to **Section 6.1 "Alternate Pin Function"** for more information.

Note:	Clearing the CCPxCON register will force the CCPx compare output latch to the default low level. This is not the PORT I/O data latch.

15.2.2 TIMER1 MODE SELECTION

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

Note:	Clocking Timer1 from the system clock (FOSC) should not be used in Compare mode. For the Compare operation of the TMR1 register to the CCPRx register to occur, Timer1 must be clocked from the Instruction Clock (FOSC/4) or from an external clock source.

15.2.3 SOFTWARE INTERRUPT MODE

When Software Interrupt mode is chosen (CCPxM<3:0> = 1010), the CCPxIF bit in the PIRx register is set and the CCPx module does not assert control of the CCPx pin (refer to the CCPxCON register).

15.2.4 SPECIAL EVENT TRIGGER

When Special Event Trigger mode is chosen (CCPxM<3:0> = 1011), the CCPx module does the following:

- Resets Timer1
- Starts an ADC conversion if ADC is enabled (CCP2 only)

The CCPx module does not assert control of the CCPx pin in this mode (refer to the CCPxCON register).

The Special Event Trigger output of the CCP occurs immediately upon a match between the TMR1H, TMR1L register pair and the CCPRxH, CCPRxL register pair. The TMR1H, TMR1L register pair is not reset until the next rising edge of the Timer1 clock. This allows the CCPRxH, CCPRxL register pair to effectively provide a 16-bit programmable period register for Timer1.

Note 1:	The Special Event Trigger from the CCP module does not set interrupt flag bit TMR1IF of the PIR1 register.
2:	Removing the match condition by changing the contents of the CCPRxH and CCPRxL register pair, between the clock edge that generates the Special Event Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring.

15.2.5 COMPARE DURING SLEEP

The Compare Mode is dependent upon the system clock (FOSC) for proper operation. Since FOSC is shut down during Sleep mode, the Compare mode will not function properly during Sleep.

16.0 ADDRESSABLE UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (AUSART)

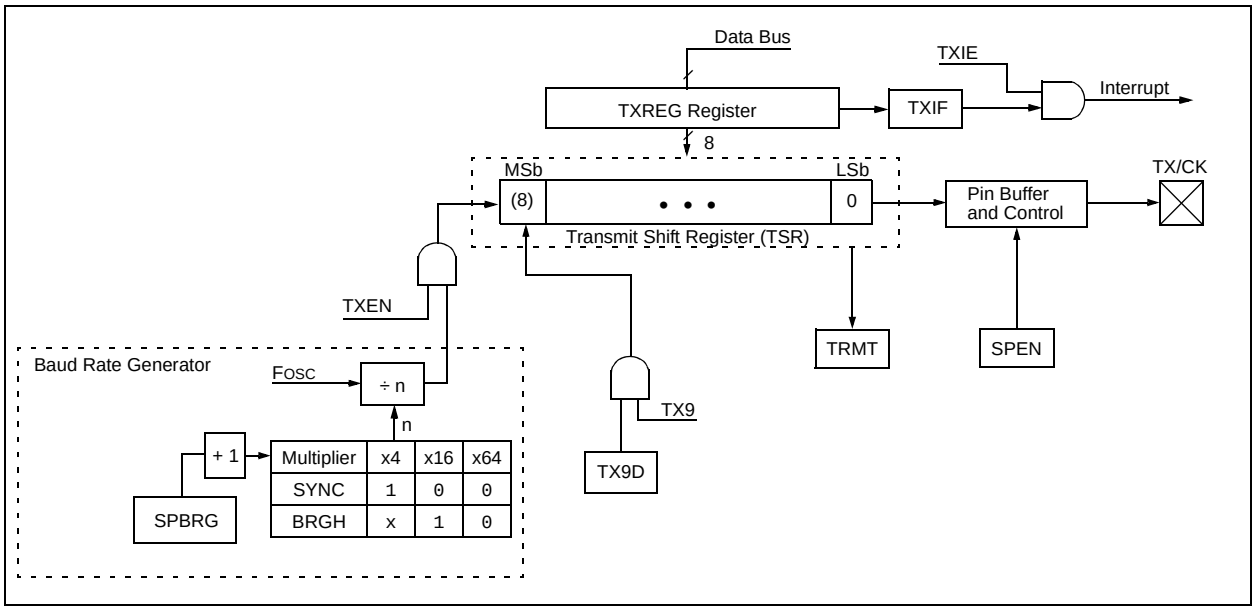
The Addressable Universal Synchronous Asynchronous Receiver Transmitter (AUSART) module is a serial I/O communications peripheral. It contains all the clock generators, shift registers and data buffers necessary to perform an input or output serial data transfer independent of device program execution. The AUSART, also known as a Serial Communications Interface (SCI), can be configured as a full-duplex asynchronous system or half-duplex synchronous system. Full-Duplex mode is useful for communications with peripheral systems, such as CRT terminals and personal computers. Half-Duplex Synchronous mode is intended for communications with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs or other microcontrollers. These devices typically do not have internal clocks for baud rate generation and require the external clock signal provided by a master synchronous device.

The AUSART module includes the following capabilities:

- Full-duplex asynchronous transmit and receive
- Two-character input buffer
- One-character output buffer
- Programmable 8-bit or 9-bit character length
- Address detection in 9-bit mode
- Input buffer overrun error detection
- Received character framing error detection
- Half-duplex synchronous master
- Half-duplex synchronous slave
- Sleep operation

Block diagrams of the AUSART transmitter and receiver are shown in Figure 16-1 and Figure 16-2.

FIGURE 16-1: AUSART TRANSMIT BLOCK DIAGRAM



16.3.2.3 AUSART Synchronous Slave Reception

The operation of the Synchronous Master and Slave modes is identical (**Section 16.3.1.4 "Synchronous Master Reception"**), with the following exceptions:

- Sleep
- CREN bit is always set, therefore the receiver is never Idle
- SREN bit, which is a "don't care" in Slave mode

A character may be received while in Sleep mode by setting the CREN bit prior to entering Sleep. Once the word is received, the RSR register will transfer the data to the RCREG register. If the RCIE interrupt enable bit of the PIE1 register is set, the interrupt generated will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will branch to the interrupt vector.

16.3.2.4 Synchronous Slave Reception Setup:

1. Set the SYNC and SPEN bits and clear the CSRC bit.
2. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
3. If 9-bit reception is desired, set the RX9 bit.
4. Verify address detection is disabled by clearing the ADDEN bit of the RCSTA register.
5. Set the CREN bit to enable reception.
6. The RCIF bit of the PIR1 register will be set when reception is complete. An interrupt will be generated if the RCIE bit of the PIE1 register was set.
7. If 9-bit mode is enabled, retrieve the Most Significant bit from the RX9D bit of the RCSTA register.
8. Retrieve the eight Least Significant bits from the receive FIFO by reading the RCREG register.
9. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register.

TABLE 16-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
RCREG	AUSART Receive Data Register								0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000X	0000 000X
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Synchronous Slave Reception.

FIGURE 17-4: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 0)

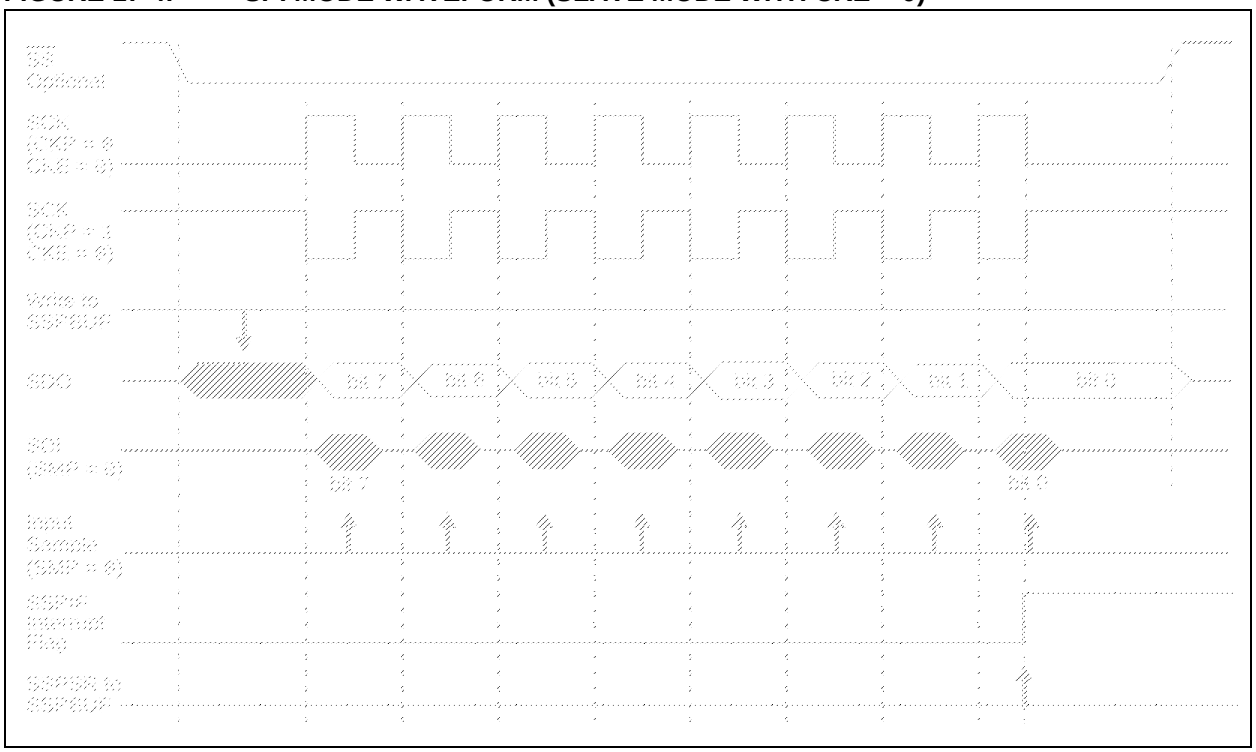
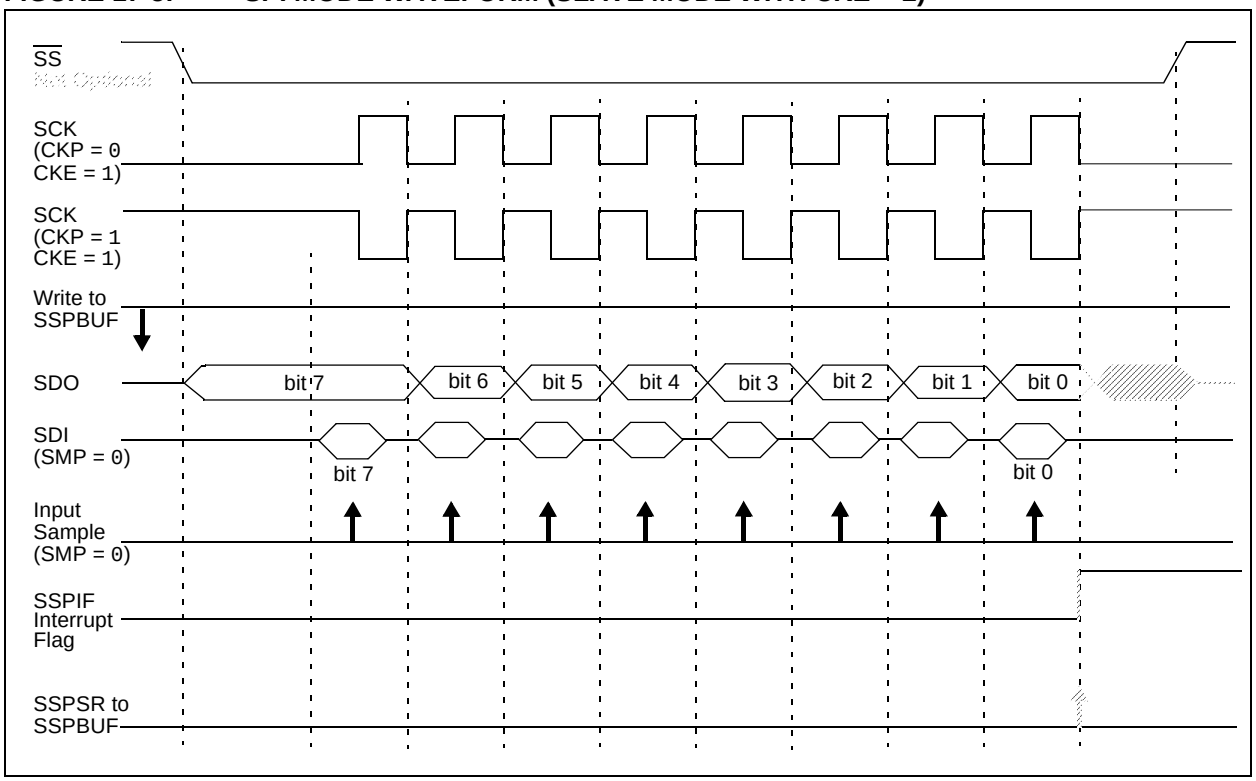


FIGURE 17-5: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)



REGISTER 17-3: SSPCON: SYNCHRONOUS SERIAL PORT CONTROL REGISTER (I²C MODE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **WCOL**: Write Collision Detect bit
- 1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)
- 0 = No collision

bit 6 **SSPOV**: Receive Overflow Indicator bit
- 1 = A byte is received while the SSPBUF register is still holding the previous byte. SSPOV is a "don't care" in Transmit mode. SSPOV must be cleared in software in either mode.
- 0 = No overflow

bit 5 **SSPEN**: Synchronous Serial Port Enable bit
- 1 = Enables the serial port and configures the SDA and SCL pins as serial port pins **(2)**
- 0 = Disables serial port and configures these pins as I/O port pins

bit 4 **CKP**: Clock Polarity Select bit
- 1 = Release control of SCL
- 0 = Holds clock low (clock stretch). (Used to ensure data setup time.)

bit 3-0 **SSPM<3:0>**: Synchronous Serial Port Mode Select bits
- 0110 = I²C Slave mode, 7-bit address
- 0111 = I²C Slave mode, 10-bit address
- 1000 = Reserved
- 1001 = Load SSPMSK register at SSPADD SFR Address **(1)**
- 1010 = Reserved
- 1011 = I²C Firmware Controlled Master mode (Slave Idle)
- 1100 = Reserved
- 1101 = Reserved
- 1110 = I²C Slave mode, 7-bit address with Start and Stop bit interrupts enabled
- 1111 = I²C Slave mode, 10-bit address with Start and Stop bit interrupts enabled

Note 1: When this mode is selected, any reads or writes to the SSPADD SFR address accesses the SSPMSK register.

2: When enabled, these pins must be properly configured as input or output using the associated TRIS bit.

22.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

22.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

TABLE 23-3: CLKOUT AND I/O TIMING PARAMETERS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
OS11	TosH2ckL	Fosc↑ to CLKOUT↓ (1)	—	—	70	ns	VDD = 3.3-5.0V
OS12	TosH2ckH	Fosc↑ to CLKOUT↑ (1)	—	—	72	ns	VDD = 3.3-5.0V
OS13	TckL2ioV	CLKOUT↓ to Port out valid(1)	—	—	20	ns	
OS14	TioV2ckH	Port input valid before CLKOUT↑(1)	TOSC + 200 ns	—	—	ns	
OS15	TosH2ioV	Fosc↑ (Q1 cycle) to Port out valid	—	50	70*	ns	VDD = 3.3-5.0V
OS16	TosH2ioI	Fosc↑ (Q2 cycle) to Port input invalid (I/O in hold time)	50	—	—	ns	VDD = 3.3-5.0V
OS17	TioV2osH	Port input valid to Fosc↑ (Q2 cycle) (I/O in setup time)	20	—	—	ns	
OS18	TioR	Port output rise time(2)	— —	40 15	72 32	ns	VDD = 2.0V VDD = 3.3-5.0V
OS19	TioF	Port output fall time(2)	— —	28 15	55 30	ns	VDD = 2.0V VDD = 3.3-5.0V
OS20*	Tinp	INT pin input high or low time	25	—	—	ns	
OS21*	Trbp	PORTB interrupt-on-change new input level time	TCY	—	—	ns	

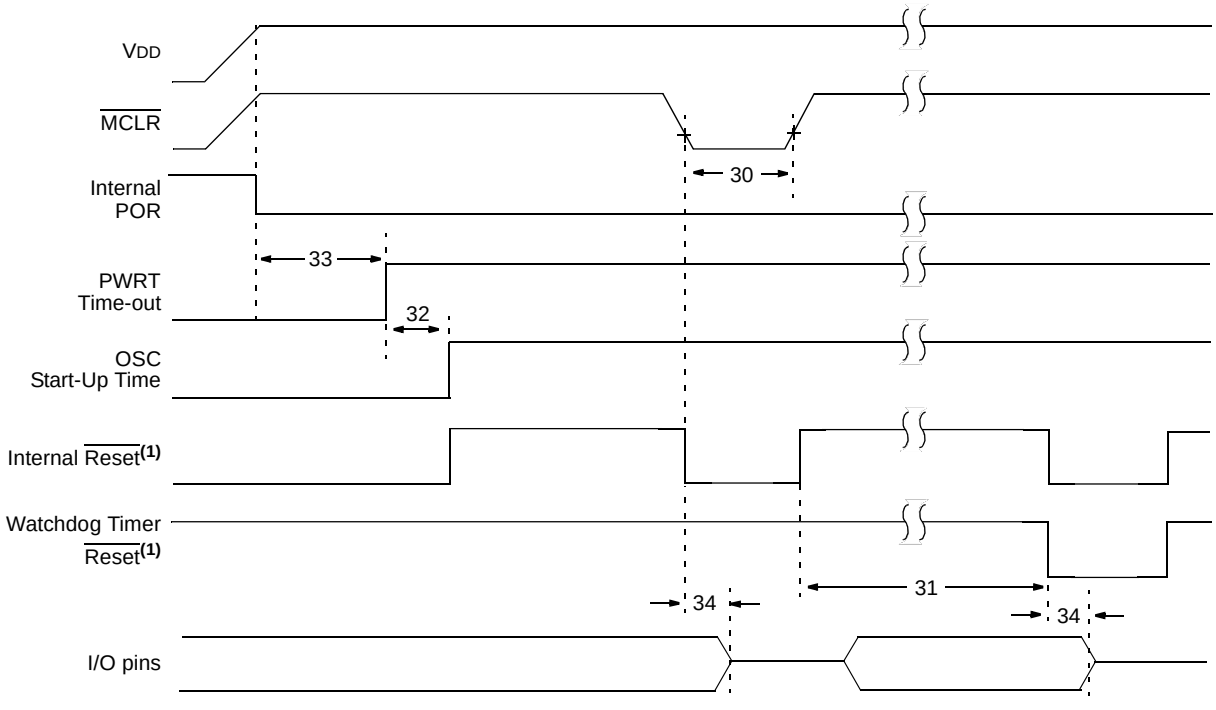
* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated.

Note 1: Measurements are taken in RC mode where CLKOUT output is 4 x TOSC.

2: Includes OSC2 in CLKOUT mode.

FIGURE 23-8: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note 1: Asserted low.

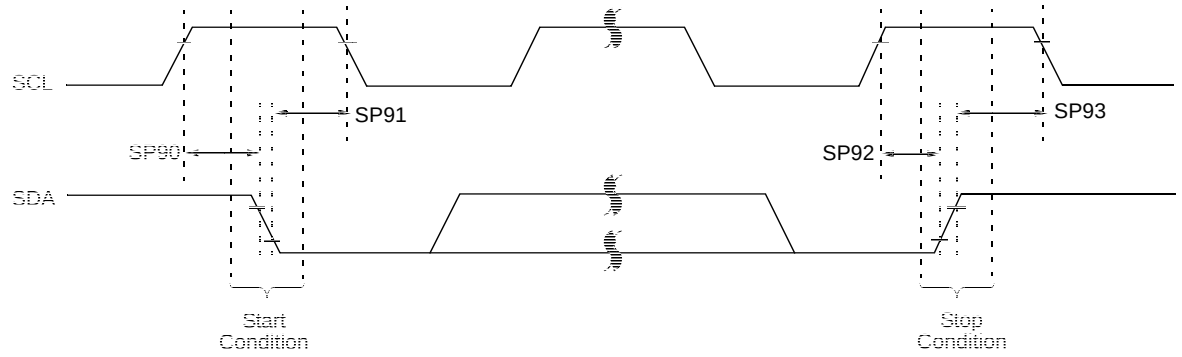
TABLE 23-11: SPI MODE REQUIREMENTS

Param No.	Symbol	Characteristic		Min.	Typ†	Max.	Units	Conditions
SP70*	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK↓ or SCK↑ input		Tcy	—	—	ns	
SP71*	TscH	SCK input high time (Slave mode)		Tcy + 20	—	—	ns	
SP72*	TscL	SCK input low time (Slave mode)		Tcy + 20	—	—	ns	
SP73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		100	—	—	ns	
SP74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	—	—	ns	
SP75*	TdoR	SDO data output rise time	3.0-5.5V	—	10	25	ns	
			1.8-5.5V	—	25	50	ns	
SP76*	TdoF	SDO data output fall time		—	10	25	ns	
SP77*	TssH2doZ	$\overline{SS}\uparrow$ to SDO output high-impedance		10	—	50	ns	
SP78*	TscR	SCK output rise time (Master mode)	3.0-5.5V	—	10	25	ns	
			1.8-5.5V	—	25	50	ns	
SP79*	TscF	SCK output fall time (Master mode)		—	10	25	ns	
SP80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	3.0-5.5V	—	—	50	ns	
			1.8-5.5V	—	—	145	ns	
SP81*	TdoV2scH, TdoV2scL	SDO data output setup to SCK edge		Tcy	—	—	ns	
SP82*	TssL2doV	SDO data output valid after $\overline{SS}\downarrow$ edge		—	—	50	ns	
SP83*	TscH2ssH, TscL2ssH	$\overline{SS}\uparrow$ after SCK edge		1.5Tcy + 40	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 23-20: I^2C BUS START/STOP BITS TIMING



Note: Refer to Figure 23-2 for load conditions.

TABLE 23-13: I^2C BUS DATA REQUIREMENTS

Param. No.	Symbol	Characteristic		Min.	Max.	Units	Conditions
SP100*	THIGH	Clock high time	100 kHz mode	4.0	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	Device must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
SP101*	TLOW	Clock low time	100 kHz mode	4.7	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	Device must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
SP102*	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1CB	300	ns	CB is specified to be from 10-400 pF
SP103*	TF	SDA and SCL fall time	100 kHz mode	—	250	ns	
			400 kHz mode	20 + 0.1CB	250	ns	CB is specified to be from 10-400 pF
SP106*	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
SP107*	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	**(Note 2)**
			400 kHz mode	100	—	ns	
SP109*	TAA	Output valid from clock	100 kHz mode	—	3500	ns	**(Note 1)**
			400 kHz mode	—	—	ns	
SP110*	TBUF	Bus free time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
SP111	CB	Bus capacitive loading		—	400	pF	

* These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

2: A Fast mode (400 kHz) I^2C bus device can be used in a Standard mode (100 kHz) I^2C bus system, but the requirement $T_{SU:DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line T_R max. + $T_{SU:DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification), before the SCL line is released.

TABLE 23-14: CAP SENSE OSCILLATOR SPECIFICATIONS

Param. No.	Symbol	Characteristic		Min.	Typ†	Max.	Units	Conditions
CS01	ISRC	Current Source	High	—	-5.8	-6	µA	-40, -85°C
			Medium	—	-1.1	-3.2	µA	
			Low	—	-0.2	-0.9	µA	
CS02	ISNK	Current Sink	High	—	6.6	6	µA	-40, -85°C
			Medium	—	1.3	3.2	µA	
			Low	—	0.24	0.9	µA	
CS03	VCHYST	Cap Hysteresis	High	—	525	—	mV	VCTH-VCTL
			Medium	—	375	—	mV	
			Low	—	280	—	mV	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 23-22: CAP SENSE OSCILLATOR

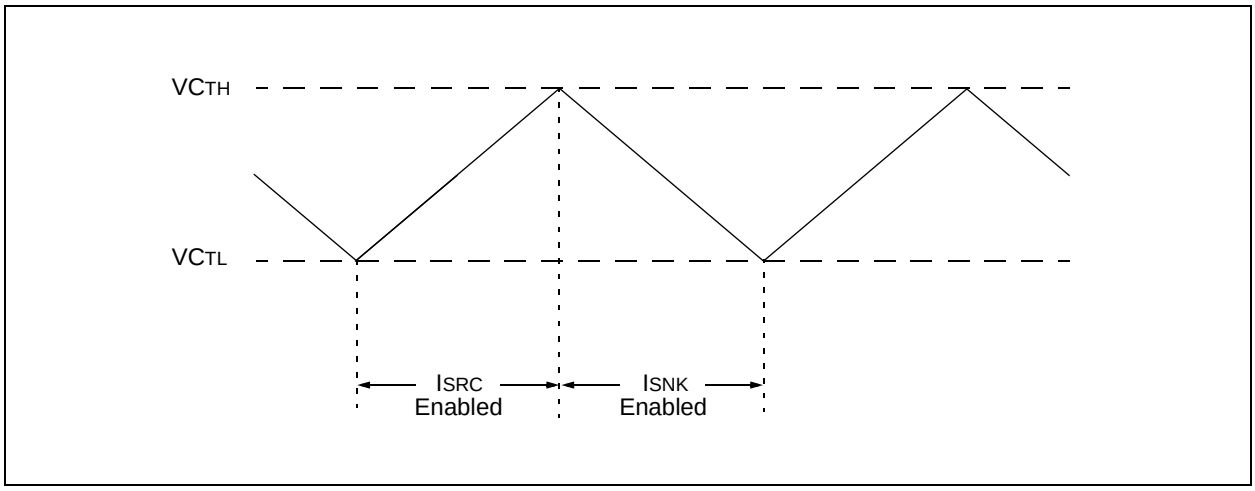


FIGURE 24-9: PIC16F722/3/4/6/7 MAXIMUM IDD vs. FOSC OVER VDD, HS MODE, VCAP = 0.1 µF

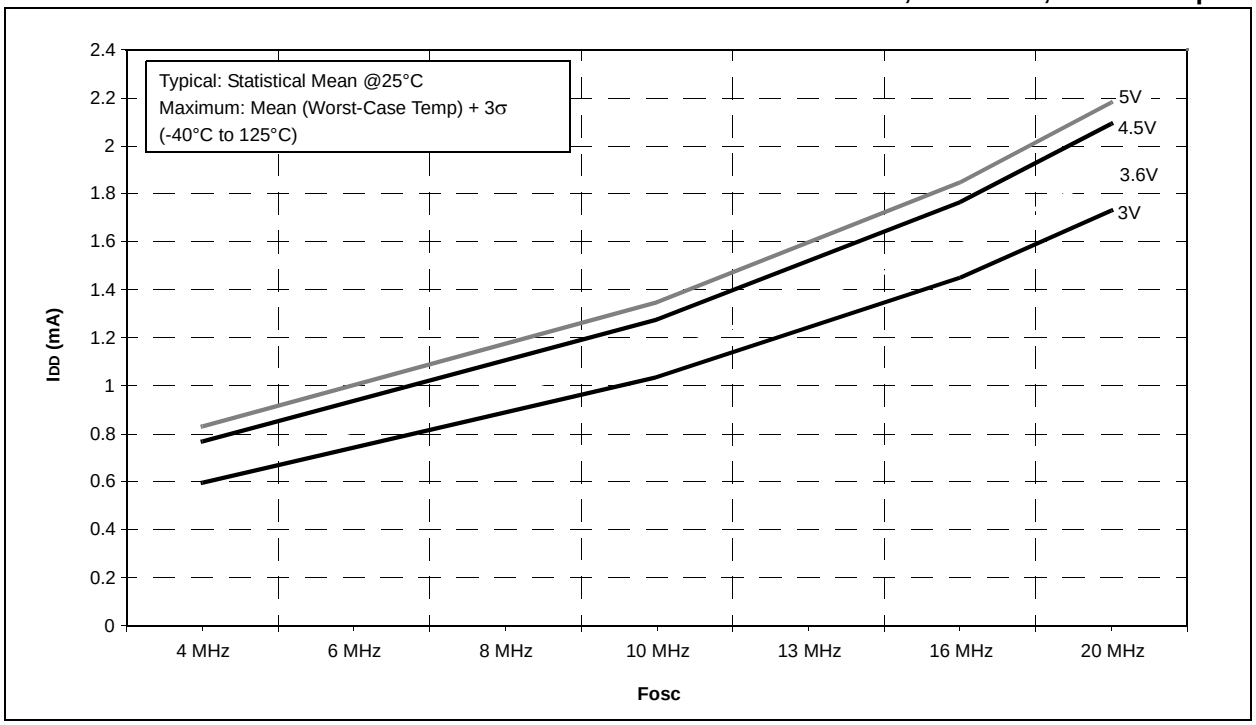


FIGURE 24-10: PIC16LF722/3/4/6/7 MAXIMUM IDD vs. FOSC OVER VDD, HS MODE

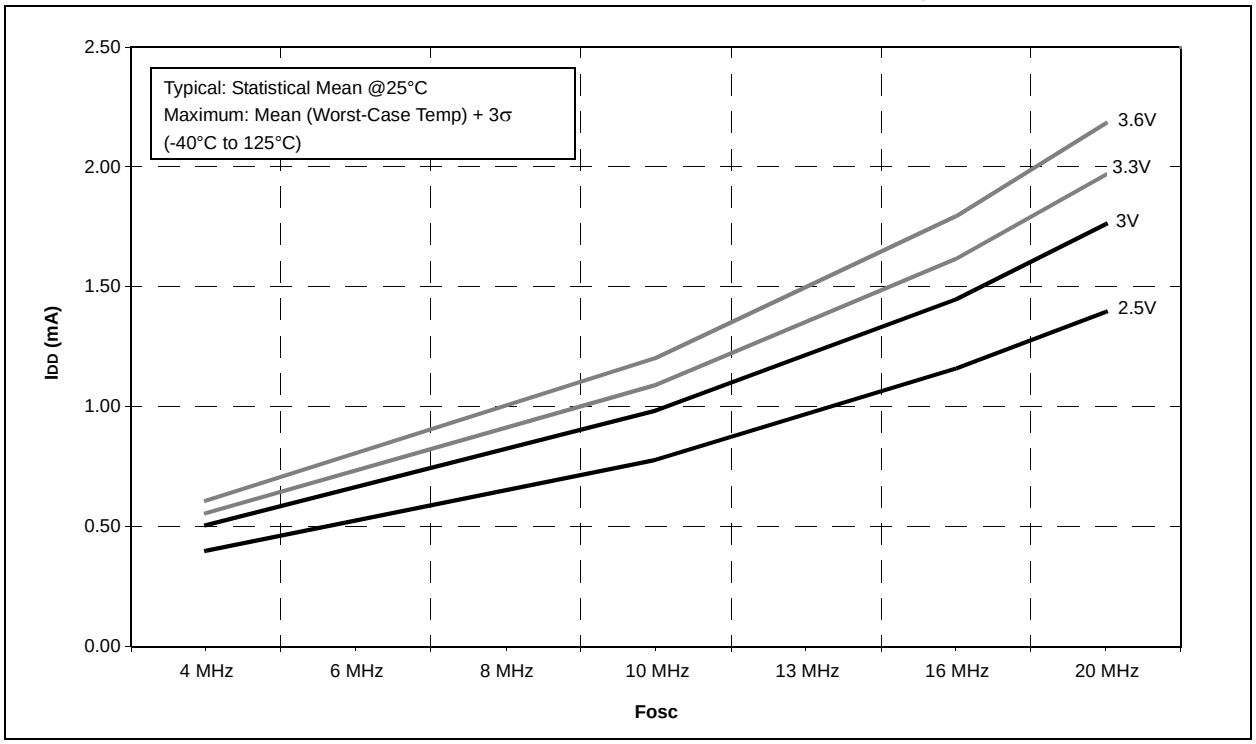


FIGURE 24-19: PIC16F722/3/4/6/7 MAXIMUM IDD vs. FOSC OVER VDD, INTOSC MODE, VCAP = 0.1 µF

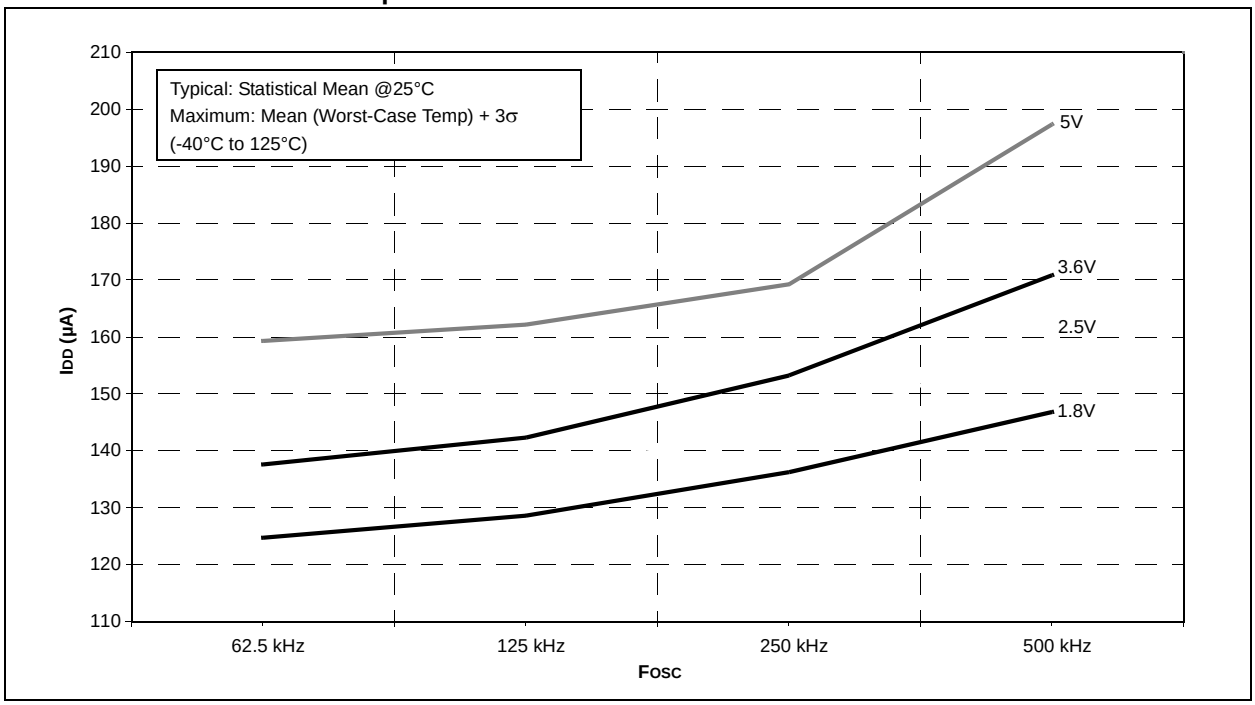


FIGURE 24-20: PIC16LF722/3/4/6/7 MAXIMUM IDD vs. FOSC OVER VDD, INTOSC MODE

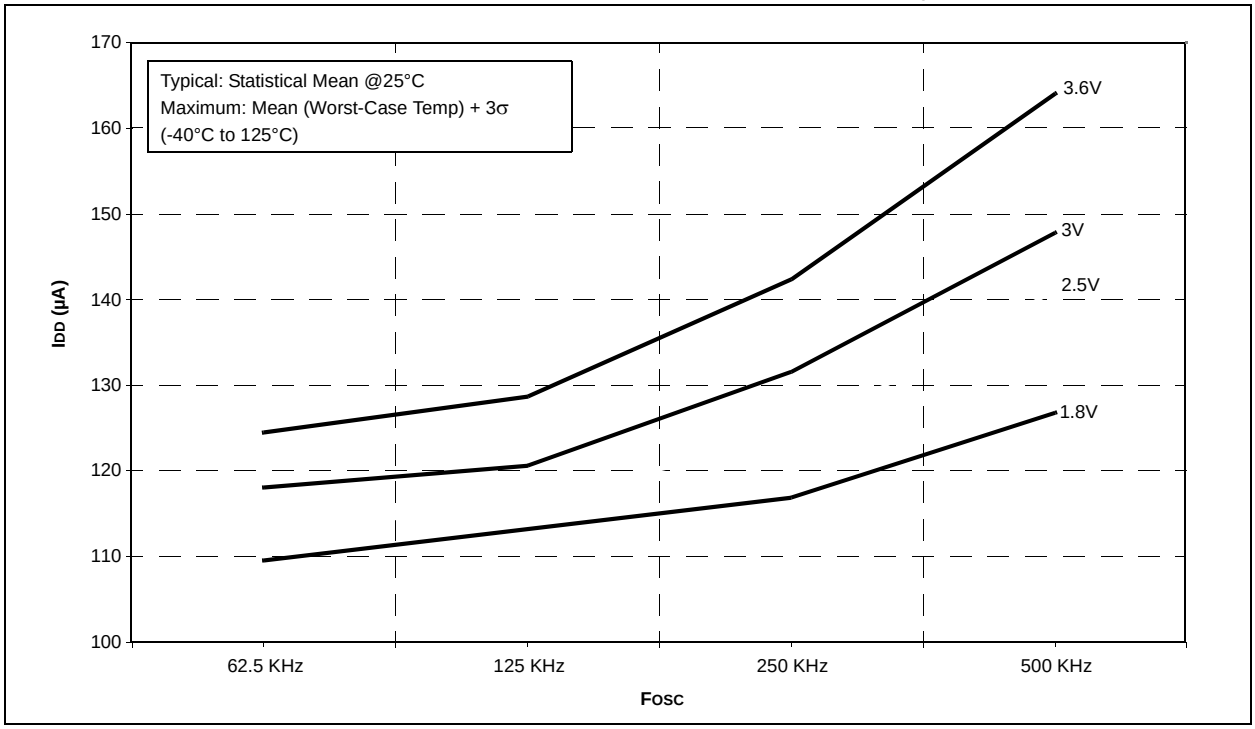


FIGURE 24-57: V_{OL} vs. I_{OL} OVER TEMPERATURE, V_{DD} = 1.8V

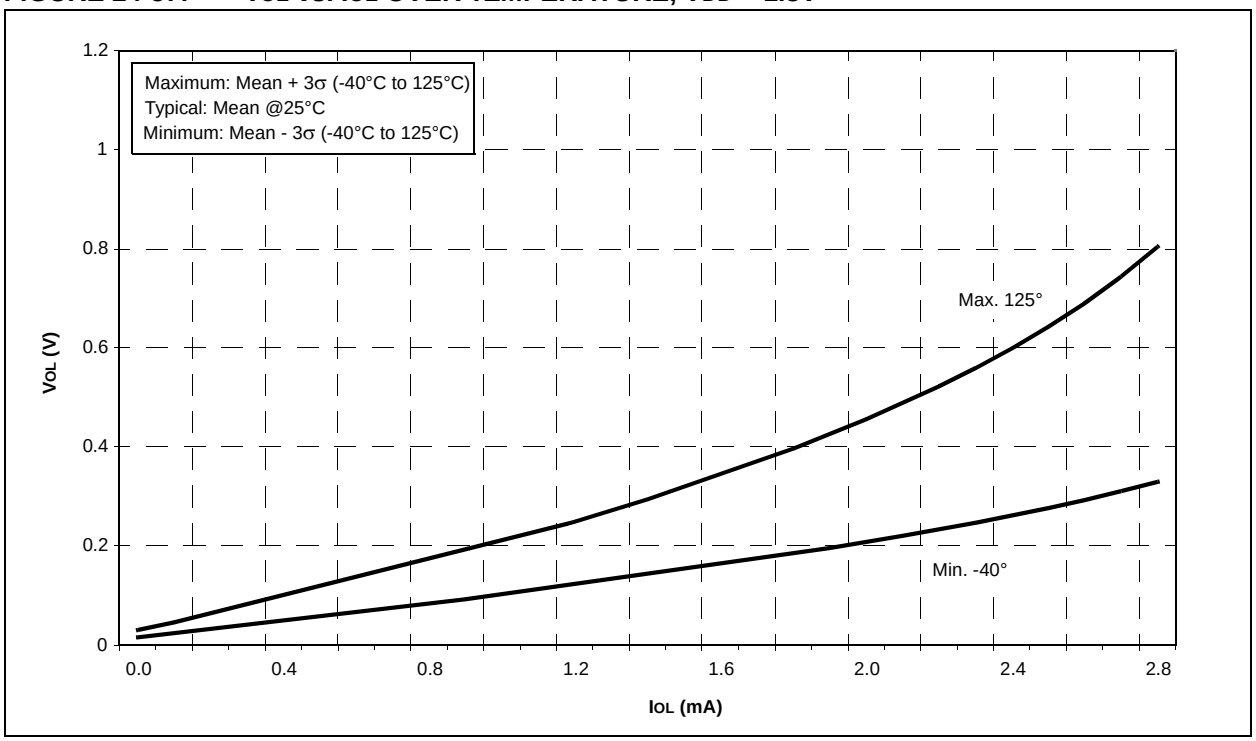
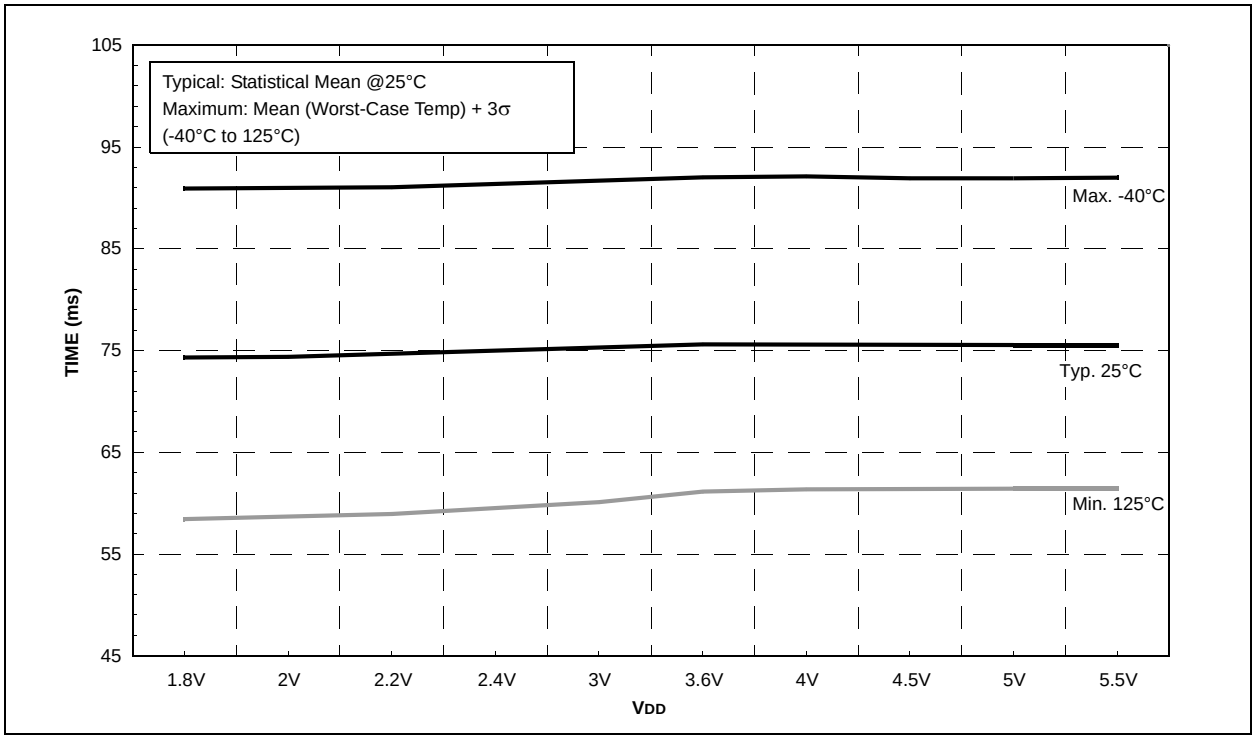
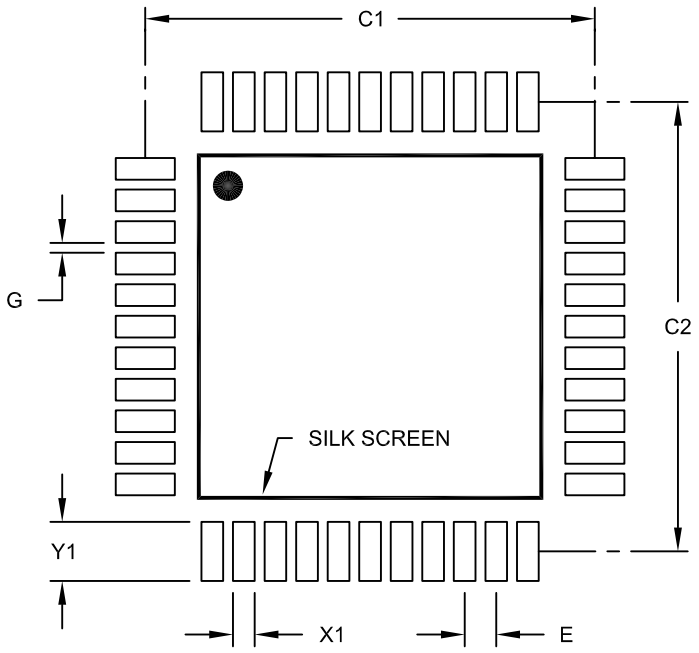


FIGURE 24-58: PIC16F722/3/4/6/7 PWRT PERIOD



44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076A