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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf724-e-ml

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# 1.0 DEVICE OVERVIEW

The PIC16(L)F722/3/4/6/7 devices are covered by this data sheet. They are available in 28/40/44-pin packages. Figure 1-1 shows a block diagram of the PIC16F722/723/726/PIC16LF722/723/726 devices and Figure 1-2 shows a block diagram of the PIC16F724/727/PIC16LF724/727 devices. Table 1-1 shows the pinout descriptions.

POR	BOR	то	PD	Condition			
0	x	1	1	Power-on Reset or LDO Reset			
0	x	0	x	Illegal, TO is set on POR			
0	x	x	0	Illegal, PD is set on POR			
1	0	1	1	Brown-out Reset			
1	1	0	1	WDT Reset			
1	1	0	0	WDT Wake-up			
1	1	u	u	MCLR Reset during normal operation			
1	1	1	0	MCLR Reset during Sleep or interrupt wake-up from Sleep			

#### TABLE 3-1: STATUS BITS AND THEIR SIGNIFICANCE

# TABLE 3-2: RESET CONDITION FOR SPECIAL REGISTERS<sup>(2)</sup>

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	0000h	0001 1xxx	0x
MCLR Reset during normal operation	0000h	000u uuuu	uu
MCLR Reset during Sleep	0000h	0001 Ouuu	uu
WDT Reset	0000h	0000 luuu	uu
WDT Wake-up	PC + 1	uuu0 0uuu	uu
Brown-out Reset	0000h	0001 luuu	u0
Interrupt Wake-up from Sleep	PC + 1 <sup>(1)</sup>	uuul Ouuu	uu

**Legend:** u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

**Note 1:** When the wake-up is due to an interrupt and Global Enable bit (GIE) is set, the return address is pushed on the stack and PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

**2:** If a Status bit is not implemented, that bit will be read as '0'.

# PIC16(L)F722/3/4/6/7

#### 4.5.3 PIE2 REGISTER

Γ.

bit 0

The PIE2 register contains the interrupt enable bits, as shown in Register 4-3.

# Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

#### REGISTER 4-3: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	CCP2IE
bit 7							bit 0

Legena:			
R = Readable bit W	= Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR '1'	= Bit is set	0' = Bit is cleared	x = Bit is unknown

#### bit 7-1 Unimplemented: Read as '0'

CCP2IE: CCP2 Interrupt Enable bit

1 = Enables the CCP2 interrupt

0 = Disables the CCP2 interrupt

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	00 0000	00 0000
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	11 1111	11 1111
APFCON	—	—	—	—	—	_	SSSEL	CCP2SEL	00	00
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000
CPSCON0	CPSON	—	—	—	CPSRNG1	CPSRNG0	CPSOUT	TOXCS	0 0000	0 0000
CPSCON1	—	—	—	—	CPSCH3	CPSCH2	CPSCH1	CPSCH0	0000	0000
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
IOCB	IOCB7	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0	0000 0000	0000 0000
OPTION_REG	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	XXXX XXXX	XXXX XXXX
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T <u>1GGO</u> / DONE	T1GVAL	T1GSS1	T1GSS0	0000 0x00	uuuu uxuu
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
WPUB	WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0	1111 1111	1111 1111

TABLE 6-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTB.

## 7.6 External Clock Modes

#### 7.6.1 OSCILLATOR START-UP TIMER (OST)

If the oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations on the OSC1 pin before the device is released from Reset. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the oscillator module.

#### 7.6.2 EC MODE

The External Clock (EC) mode allows an externally generated logic level as the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input and the OSC2 is available for general purpose I/O. Figure 7-2 shows the pin connections for EC mode.

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC<sup>®</sup> MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

#### FIGURE 7-2: EXTERNAL CLOCK (EC) MODE OPERATION



#### 7.6.3 LP, XT, HS MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 7-3). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is best suited to drive resonators with a low drive level specification, for example, tuning fork type crystals.

**XT** Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

**HS** Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 7-3 and Figure 7-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

#### FIGURE 7-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)



Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

- **2:** Always verify oscillator performance over the VDD and temperature range that is expected for the application.
- **3:** For oscillator design assistance, reference the following Microchip Applications Notes:
  - AN826, Crystal Oscillator Basics and Crystal Selection for rfPIC<sup>®</sup> and PIC<sup>®</sup> Devices (DS00826)
  - AN849, Basic PIC<sup>®</sup> Oscillator Design (DS00849)
  - AN943, Practical PIC<sup>®</sup> Oscillator Analysis and Design (DS00943)
  - AN949, Making Your Oscillator Work (DS00949).

# 8.2 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using  $ICSP^{TM}$  for verification purposes.

Note:	The entire Flash program memory will be							
	erased when the code protection is turned							
	off. See the "PIC16(L)F72X Memory							
	Programming Specification" (DS41332)							
	for more information.							

# 8.3 User ID

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify mode. Only the Least Significant seven bits of the ID locations are reported when using MPLAB IDE. See the "*PIC16(L)F72X Memory Programming Specification*" (DS41332) for more information.

# 9.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 8-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 8-bit binary result via successive approximation and stores the conversion result into the ADC result register (ADRES). Figure 9-1 shows the block diagram of the ADC.

The ADC voltage reference is software selectable to be either internally generated or externally supplied.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.



#### FIGURE 9-1: ADC BLOCK DIAGRAM

# 12.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module is a 16-bit timer/counter with the following features:

- 16-bit timer/counter register pair (TMR1H:TMR1L)
- Programmable internal or external clock source
- 3-bit prescaler
- Dedicated LP oscillator circuit
- Synchronous or asynchronous operation
- Multiple Timer1 gate (count enable) sources
- Interrupt on overflow
- Wake-up on overflow (external clock, Asynchronous mode only)
- Time base for the Capture/Compare function
- Special Event Trigger (with CCP)

- Gate Single-pulse mode
  - Gate Value StatusGate Event Interrupt

· Gate Toggle mode

Selectable Gate Source Polarity

Figure 12-1 is a block diagram of the Timer1 module.

#### FIGURE 12-1: TIMER1 BLOCK DIAGRAM



## 14.5 Software Control

The software portion of the capacitive sensing module is required to determine the change in frequency of the capacitive sensing oscillator. This is accomplished by the following:

- Setting a fixed time base to acquire counts on Timer0 or Timer1
- Establishing the nominal frequency for the capacitive sensing oscillator
- Establishing the reduced frequency for the capacitive sensing oscillator due to an additional capacitive load
- Set the frequency threshold

#### 14.5.1 NOMINAL FREQUENCY (NO CAPACITIVE LOAD)

To determine the nominal frequency of the capacitive sensing oscillator:

- Remove any extra capacitive load on the selected CPSx pin
- At the start of the fixed time base, clear the timer resource
- At the end of the fixed time base save the value in the timer resource

The value of the timer resource is the number of oscillations of the capacitive sensing oscillator for the given time base. The frequency of the capacitive sensing oscillator is equal to the number of counts on in the timer divided by the period of the fixed time base.

#### 14.5.2 REDUCED FREQUENCY (ADDITIONAL CAPACITIVE LOAD)

The extra capacitive load will cause the frequency of the capacitive sensing oscillator to decrease. To determine the reduced frequency of the capacitive sensing oscillator:

- Add a typical capacitive load on the selected CPSx pin
- Use the same fixed-time base as the nominal frequency measurement
- At the start of the fixed-time base, clear the timer resource
- At the end of the fixed-time base save the value in the timer resource

The value of the timer resource is the number of oscillations of the capacitive sensing oscillator with an additional capacitive load. The frequency of the capacitive sensing oscillator is equal to the number of counts on in the timer divided by the period of the fixed time base. This frequency should be less than the value obtained during the nominal frequency measurement.

### 14.5.3 FREQUENCY THRESHOLD

The frequency threshold should be placed midway between the value of nominal frequency and the reduced frequency of the capacitive sensing oscillator. Refer to Application Note AN1103, *Software Handling for Capacitive Sensing* (DS01103) for more detailed information the software required for capacitive sensing module.

Note:	For more		inform	ation	O	n general
	Capacitive Notes:		Sensing	refer	to	Application

- AN1101, Introduction to Capacitive Sensing (DS01101)
- AN1102, Layout and Physical Design Guidelines for Capacitive Sensing (DS01102).

# 15.0 CAPTURE/COMPARE/PWM (CCP) MODULE

The Capture/Compare/PWM module is a peripheral which allows the user to time and control different events. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate a pulse-width modulated signal of varying frequency and duty cycle.

The timer resources used by the module are shown in Table 15-1.

Additional information on CCP modules is available in the Application Note AN594, *Using the CCP Modules* (DS00594).

#### TABLE 15-1: CCP MODE – TIMER RESOURCES REQUIRED

CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

CCP1 Mode	CCP2 Mode	Interaction
Capture	Capture	Same TMR1 time base
Capture	Compare	Same TMR1 time base <sup>(1, 2)</sup>
Compare	Compare	Same TMR1 time base <sup>(1, 2)</sup>
PWM	PWM	The PWMs will have the same frequency and update rate (TMR2 interrupt). The rising edges will be aligned.
PWM	Capture	None
PWM	Compare	None

# TABLE 15-2: INTERACTION OF TWO CCP MODULES

**Note 1:** If CCP2 is configured as a Special Event Trigger, CCP1 will clear Timer1, affecting the value captured on the CCP2 pin.

**2:** If CCP1 is in Capture mode and CCP2 is configured as a Special Event Trigger, CCP2 will clear Timer1, affecting the value captured on the CCP1 pin.

Note:	CCPRx	and	CCPx	throughout	this				
	document refer to CCPR1 or CCPR2 and								
	CCP1 or CCP2, respectively								

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
RCREG	AUSART Receive Data Register								0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SPBRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	0000 0000	0000 0000
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	0000 -010

#### TABLE 16-2: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Asynchronous Reception.

# 16.3.2.3 AUSART Synchronous Slave Reception

The operation of the Synchronous Master and Slave modes is identical (Section 16.3.1.4 "Synchronous Master Reception"), with the following exceptions:

- Sleep
- CREN bit is always set, therefore the receiver is never Idle
- SREN bit, which is a "don't care" in Slave mode

A character may be received while in Sleep mode by setting the CREN bit prior to entering Sleep. Once the word is received, the RSR register will transfer the data to the RCREG register. If the RCIE interrupt enable bit of the PIE1 register is set, the interrupt generated will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will branch to the interrupt vector.

- 16.3.2.4 Synchronous Slave Reception Setup:
- 1. Set the SYNC and SPEN bits and clear the CSRC bit.
- 2. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 3. If 9-bit reception is desired, set the RX9 bit.
- 4. Verify address detection is disabled by clearing the ADDEN bit of the RCSTA register.
- 5. Set the CREN bit to enable reception.
- The RCIF bit of the PIR1 register will be set when reception is complete. An interrupt will be generated if the RCIE bit of the PIE1 register was set.
- 7. If 9-bit mode is enabled, retrieve the Most Significant bit from the RX9D bit of the RCSTA register.
- 8. Retrieve the eight Least Significant bits from the receive FIFO by reading the RCREG register.
- 9. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
RCREG	AUSART R	eceive Data	a Register						0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000X	0000 000X
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	0000 -010

#### TABLE 16-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Synchronous Slave Reception.

PIC16(L)F722/3/4/6/7



# 18.0 PROGRAM MEMORY READ

The Flash program memory is readable during normal operation over the full VDD range of the device. To read data from Program Memory, five Special Function Registers (SFRs) are used:

- PMCON1
- PMDATL
- PMDATH
- PMADRL
- PMADRH

The value written to the PMADRH:PMADRL register pair determines which program memory location is read. The read operation will be initiated by setting the RD bit of the PMCON1 register. The program memory flash controller takes two instructions to complete the read, causing the second instruction after the setting the RD bit will be ignored. To avoid conflict with program execution, it is recommended that the two instructions following the setting of the RD bit are NOP. When the read completes, the result is placed in the PMDATLH:PMDATL register pair. Refer to Example 18-1 for sample code.

Note: Code-protect does not effect the CPU from performing a read operation on the program memory. For more information, refer to Section 8.2 "Code Protection".

	BANKSEL MOVF MOVWF MOVF	PMADRL MS_PROG_ADDR, PMADRH LS_PROG_ADDR,	; W; ;MS Byte of Program Address to read W;
	MOVWF	PMADRL	;LS Byte of Program Address to read
ed	BANKSEL	PMCON1	i
	BSF	PMCON1, RD	;Initiate Read
uer	NOP		
Seq	NOP		;Any instructions here are ignored as program
<u> </u>			;memory is read in second cycle after BSF
	BANKSEL	PMDATL	;
	MOVF	PMDATL, W	;W = LS Byte of Program Memory Read
	MOVWF	LOWPMBYTE	;
	MOVF	PMDATH, W	;W = MS Byte of Program Memory Read
	MOVWF	HIGHPMBYTE	;
	MOVWF	HIGHPMBYTE	;

#### EXAMPLE 18-1: PROGRAM MEMORY READ

# 23.6 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

Т							
F	Frequency	Т	Time				
Lowerc	ase letters (pp) and their meanings:						
рр							
сс	CCP1	OSC	OSC1				
ck	CLKOUT	rd	RD				
CS	CS	rw	RD or WR				
di	SDI	SC	SCK				
do	SDO	SS	SS				
dt	Data in	tO	TOCKI				
io	I/O PORT	t1	T1CKI				
mc	MCLR	wr	WR				
Upperc	Uppercase letters and their meanings:						
S							
F	Fall	Р	Period				
Н	High	R	Rise				
I	Invalid (High-impedance)	V	Valid				
L	Low	Z	High-impedance				

#### FIGURE 23-2: LOAD CONDITIONS











Note 1: If the A/D clock source is selected as RC, a time of TcY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.





#### TABLE 23-9: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$								
Param. No.	Symbol	Characteristic	Characteristic		Max.	Units	Conditions	
US120	ТскH2dtV	SYNC XMIT (Master and Slave)	3.0-5.5V	—	80	ns		
		Clock high to data-out valid	1.8-5.5V	—	100	ns		
US121 TCKRF	Clock out rise time and fall time	3.0-5.5V	—	45	ns			
		(Master mode)	1.8-5.5V	—	50	ns		
US122	TDTRF	Data-out rise time and fall time	3.0-5.5V	_	45	ns		
			1.8-5.5V	_	50	ns		

#### FIGURE 23-15: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



10

15

ns

ns

#### TABLE 23-10: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Data-hold before  $CK \downarrow (DT hold time)$ 

Data-hold after  $CK \downarrow (DT hold time)$ 

# Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C Param. Symbol Characteristic Min. Max. Units Conditions US125 TDTV2CKL SYNC RCV (Master and Slave) Image: Condition state s

US126

TCKL2DTL



#### FIGURE 24-33: PIC16F722/3/4/6/7 BOR IPD vs. VDD, VCAP = 0.1 µF













# 44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			6.80
Optional Center Pad Length	T2			6.80
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.80
Distance Between Pads	G	0.25		

#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A