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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf724-i-ml

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PIC16(L)F722/3/4/6/7





FIGURE 2-6:

PIC16F726/LF726 AND PIC16F727/LF727 SPECIAL FUNCTION REGISTERS

	٦		1		٦		т Т
ndirect addr. ^(*)	00h	Indirect addr. ^(*)	80h	Indirect addr. ^(*)	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION	81h	TMR0	101h	OPTION	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h	ANSELA	185h
PORTB	06h	TRISB	86h		106h	ANSELB	186h
PORTC	07h	TRISC	87h		107h		187h
PORTD ⁽¹⁾	08h	TRISD ⁽¹⁾	88h	CPSCON0	108h	ANSELD ⁽¹⁾	188h
PORTE	09h	TRISE	89h	CPSCON1	109h	ANSELE ⁽¹⁾	189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	PMDATL	10Ch	PMCON1	18Ch
PIR2	0Dh	PIE2	8Dh	PMADRL	10Dh	Reserved	18Dh
TMR1L	0Eh	PCON	8Eh	PMDATH	10Eh	Reserved	18Eh
TMR1H	0Fh	T1GCON	8Fh	PMADRH	10Fh	Reserved	18Fh
T1CON	10h	OSCCON	90h		110h		190h
TMR2	11h	OSCTUNE	91h		111h		191h
T2CON	12h	PR2	92h		112h		192h
SSPBUF	13h	SSPADD/SSPMSK	93h		113h		193h
SSPCON	14h	SSPSTAT	94h		114h		194h
CCPR1L	15h	WPUB	95h		115h		195h
CCPR1H	16h	IOCB	96h	General	116h	General	196h
CCP1CON	17h		97h	Purpose	117h	Purpose	197h
RCSTA	18h	TXSTA	98h	Register	118h	Register	198h
TXREG	19h	SPBRG	99h	16 Bytes	119h	16 Bytes	199h
RCREG	1Ah		9Ah		11Ah		19Ah
CCPR2L	1Bh		9Bh		11Bh		19Bh
CCPR2H	1Ch	APFCON	9Ch		11Ch		19Ch
CCP2CON	1Dh	FVRCON	9Dh		11Dh		19Dh
ADRES	1Eh		9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
	20h		A0h		120h		1A0h
General Purpose Register		General Purpose Register 80 Bytes		General Purpose Register 80 Bytes		General Purpose Register 80 Bytes	
96 Bytes			EFh		16Fh		1EFh
		Accesses 70h-7Fh	F0h	Accesses 70h-7Fh	170h	Accesses 70h-7Fh	1F0h
	7Fh		FFh		17Fh		1FFh
Bank 0	_	Bank 1	J	Bank 2	_	Bank 3	1
I: = Unimple * = Not a ph	mented o	data memory locations, gister	read as	'0',			

2.2.2.3 PCON Register

The Power Control (PCON) register contains flag bits (refer to Table 3-2) to differentiate between a:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- Watchdog Timer Reset (WDT)
- External MCLR Reset

The PCON register also controls the software enable of the BOR.

The PCON register bits are shown in Register 2-3.

REGISTER 2-3: PCON: POWER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-q	R/W-q
—	—	_	—	—	—	POR	BOR
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
q = Value depends on cor	ndition		

bit 7-2	Unimplemented: Read as '0'
bit 1	POR: Power-on Reset Status bit
	1 = No Power-on Reset occurred
	0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)
bit 0	BOR: Brown-out Reset Status bit
	 1 = No Brown-out Reset occurred 0 = A Brown-out Reset occurred (must be set in software after a Power-on Reset or Brown-out Reset occurs)

Note 1: Set BOREN<1:0> = 01 in the Configuration Word register for this bit to control the $\overline{\text{BOR}}$.

Register	Address	Power-on Reset/ Brown-out Reset ⁽¹⁾	MCLR Reset/ WDT Reset	Wake-up from Sleep through Interrupt/Time out
PCON	8Eh	dd	(1,5)	uu
T1GCON	8Fh	0000 0x00	uuuu uxuu	uuuu uxuu
OSCCON	90h	10 qq	10 qq	uu qq
OSCTUNE	91h	00 0000	uu uuuu	uu uuuu
PR2	92h	1111 1111	1111 1111	uuuu uuuu
SSPADD	93h	0000 0000	0000 0000	uuuu uuuu
SSPMSK	93h	1111 1111	1111 1111	uuuu uuuu
SSPSTAT	94h	0000 0000	0000 0000	uuuu uuuu
WPUB	95h	1111 1111	1111 1111	uuuu uuuu
IOCB	96h	0000 0000	0000 0000	uuuu uuuu
TXSTA	98h	0000 -010	0000 -010	uuuu -uuu
SPBRG	99h	0000 0000	0000 0000	uuuu uuuu
APFCON	9Ch	00	00	uu
FVRCON	9Dh	q00000	q00000	uuuuuu
ADCON1	9Fh	-00000	-00000	-uuuuu
CPSCON0	108h	0 0000	0 0000	u uuuu
CPSCON1	109h	0000	0000	uuuu
PMDATL	10Ch	xxxx xxxx	xxxx xxxx	uuuu uuuu
PMADRL	10Dh	xxxx xxxx	xxxx xxxx	uuuu uuuu
PMDATH	10Eh	xx xxxx	xx xxxx	uu uuuu
PMADRH	10Fh	x xxxx	x xxxx	u uuuu
ANSELA	185h	11 1111	11 1111	uu uuuu
ANSELB	186h	11 1111	11 1111	uu uuuu
ANSELD ⁽⁶⁾	188h	1111 1111	1111 1111	uuuu uuuu
ANSELE	189h	111	111	uuu
PMCON1	18Ch	10	10	u u

TABLE 3-4: INITIALIZATION CONDITION FOR REGISTERS (CONTINUED)

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 and PIR2 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 3-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

6: PIC16F724/727/PIC16LF724/727 only.

Note

TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ADCON0	-	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	0000 0000	0000 0000
ADCON1		ADCS2	ADCS1	ADCS0	—	—	ADREF1	ADREF0	-00000	-00000
ANSELA	-	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	11 1111	11 1111
APFCON	_	_	_	_	_	_	SSSEL	CCP2SEL	00	00
CPSCON0	CPSON	_	_	_	CPSRNG1	CPSRNG0	CPSOUT	TOXCS	0 0000	0 0000
CPSCON1	_	_	_	_	CPSCH3	CPSCH2	CPSCH1	CPSCH0	0000	0000
CONFIG2 ⁽¹⁾	_	_	VCAPEN1	VCAPEN0	—	_	_	-	-	—
OPTION_REG	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx xxxx	xxxx xxxx
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111	1111 1111

 $\label{eq:Legend: x = unknown, u = unchanged, - = unimplemented locations read as `0'. Shaded cells are not used by PORTA.$

Note 1: PIC16F72X only.

R/W-1	R/W-1	R/V	V-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU	INTEDG	Т0	cs	TOSE	PSA	PS2	PS1	PS0
bit 7								bit 0
Legend:								
R = Readable I	bit	W = W	ritable bit		U = Unimpler	mented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bi	t is set		'0' = Bit is cle	ared	x = Bit is unkı	nown
bit 7 RBPU: PORTB Pull-up Enable bit 1 = PORTB pull-ups are disabled 0 = PORTB pull-ups are enabled by individual port latch values								
bit 6	INTEDG: Interrupt Edge Select bit 1 = Interrupt on rising edge of INT pin 0 = Interrupt on falling edge of INT pin							
bit 5	TOCS: TMR0 1 = Transition 0 = Internal in	Clock S n on TOC nstruction	ource Sele KI pin or C n cycle cloo	ect bit PSOSC si ck (Fosc/4)	gnal)			
bit 4	TOSE: TMR0 1 = Incremen 0 = Incremen	Source t on high t on low	Edge Sele n-to-low tra -to-high tra	ct bit nsition on ⁻ nsition on ⁻	T0CKI pin T0CKI pin			
bit 3	PSA: Presca 1 = Prescaler 0 = Prescaler	ler Assig is assig is assig	Inment bit Ined to the Ined to the	WDT Timer0 mc	odule			
bit 2-0	PS<2:0>: Pre	escaler F	Rate Select	bits				
	BIT	VALUE	TMR0 RATE	WDT RATI	E			
	0 0 0 1 1 1 1	000 001 010 0111 000 01 10 11	1 : 2 1 : 4 1 : 8 1 : 16 1 : 32 1 : 64 1 : 128 1 : 256	1 : 1 1 : 2 1 : 4 1 : 8 1 : 16 1 : 32 1 : 64 1 : 128	_			
TABLE 11-1:	SUMMAR	Y OF R	EGISTER	S ASSOC		H TIMER0		

REGISTER 11-1: OPTION_REG: OPTION REGISTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CPSCON0	CPSON	_	_		CPSRNG1	CPSRNG0	CPSOUT	T0XCS	0 0000	0 0000
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
OPTION_REG	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
TMR0	MR0 Timer0 Module Register								xxxx xxxx	uuuu uuuu
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111	1111 1111

Legend: -= Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.

12.11 Timer1 Control Register

The Timer1 Control register (T1CON), shown in Register 12-1, is used to control Timer1 and select the various features of the Timer1 module.

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	_	TMR1ON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6	TMR1CS<1:0>: Timer1 Clock Source Select bits
	11 = Timer1 clock source is Capacitive Sensing Oscillator (CAPOSC)
	10 = Timer1 clock source is pin or oscillator:
	$\underline{\text{If } \text{T1OSCEN} = 0}$
	External clock from T1CKI pin (on the rising edge)
	$\frac{\text{If } 110\text{SUEN} = 1}{\text{Crustel excillator on T10SUT10SO pine}}$
	01 – Timer1 clock source is system clock (FOSC)
	00 = Timer1 clock source is instruction clock (FOSC/4)
bit 5-4	T1CKPS<1:0>: Timer1 Input Clock Prescale Select bits
	11 = 1.8 Prescale value
	10 = 1:4 Prescale value
	01 = 1:2 Prescale value
	00 = 1:1 Prescale value
bit 3	T1OSCEN: LP Oscillator Enable Control bit
	1 = Dedicated Timer1 oscillator circuit enabled
	0 = Dedicated Timer1 oscillator circuit disabled
bit 2	T1SYNC: Timer1 External Clock Input Synchronization Control bit
	<u>TMR1CS<1:0> = $1X$</u>
	1 = Do not synchronize external clock input
	0 = Synchronize external clock input with system clock (FOSC)
	TMR1CS<1:0> = 0X
	This bit is ignored. Timer1 uses the internal clock when TMR1CS<1:0> = $1X$.
bit 1	Unimplemented: Read as '0'
bit 0	TMR10N: Timer1 On bit
	1 = Enables Timer1
	0 = Stops Timer1
	Clears Timer1 Gate flip-flop

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	11 1111	11 1111
CCP1CON	_	_	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
CCP2CON	_	_	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	xxxx xxxx
TMR1H	Holding Reg	gister for the	Most Signific	ant Byte of th	he 16-bit TMI	R1 Register			XXXX XXXX	uuuu uuuu
TMR1L	Holding Reg	gister for the	Least Signifi	cant Byte of	the 16-bit TM	IR1 Register			xxxx xxxx	uuuu uuuu
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	_	TMR10N	0000 00-0	uuuu uu-u
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T <u>1GGO</u> / DONE	T1GVAL	T1GSS1	T1GSS0	0000 0x00	uuuu uxuu

TABLE 12-6: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
—	—	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0		
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'			
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown		
bit 7-6	Unimplemen	ted: Read as '	0'						
bit 5-4	DCxB<1:0>:	PWM Duty Cyc	cle Least Signi	ficant bits					
	Capture mode	<u>e</u> :							
	Unused	-l							
	Compare mod	<u>de:</u>							
	Dhused								
	These bits are	e the two LSbs	of the PWM d	uty cycle. The	eight MSbs are	e found in CCP	RxL.		
bit 3-0	CCPxM<3:0>	CCP Mode S	elect bits						
	0000 = Captu	ure/Compare/F	WM off (resets	s CCP module)					
	0001 = Unus	ed (reserved)	ale output on i	match (CCPvIE	bit of the DIR	rogistor is sot)		
	0011 = Unus	ed (reserved)	gie output on i			register is set)		
	0100 = Capte	ure mode, evéi	y falling edge						
	0101 = Captu	ure mode, evei	y rising edge						
	0110 = Capti	ure mode, ever	y 4th rising ed	ge					
	1000 = Com	pare mode, ever	output on mat	tch (CCPxIF bit	t of the PIRx re	aister is set)			
	1001 = Com	pare mode, cle	ar output on m	atch (CCPxIF	bit of the PIRx	register is set)			
	1010 = Comp CCP	Compare mode, generate software interrupt on match (CCPxIF bit is set of the PIRx register, CCPx pin is unaffected)							
	1011 = Com	pare mode, trig	iger special ev	ent (CCPxIF b	it of the PIRx r	egister is set,	TMR1 is reset		
	and A	VD conversion	(1) is started if	the ADC modu	le is enabled.	CCPx pin is un	affected.)		
	11xx = PWM	1 mode.							

REGISTER 15-1: CCPxCON: CCPx CONTROL REGISTER



						SYNC = 0,	BRGH =	0				
BAUD	Foso	= 20.00	0 MHz	Fosc = 18.432 MHz			Fosc = 16.0000 MHz			Fosc	= 11.05	92 MHz
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	_		_	_		_			—		_	_
1200	1221	1.73	255	1200	0.00	239	1201	0.08	207	1200	0.00	143
2400	2404	0.16	129	2400	0.00	119	2403	0.16	103	2400	0.00	71
9600	9470	-1.36	32	9600	0.00	29	9615	0.16	25	9600	0.00	17
10417	10417	0.00	29	10286	-1.26	27	10416	-0.01	23	10165	-2.42	16
19.2k	19.53k	1.73	15	19.20k	0.00	14	19.23k	0.16	12	19.20k	0.00	8
57.6k	_	—	_	57.60k	0.00	7	—	—	—	57.60k	0.00	2
115.2k	—	—	—	—	—	—	—	—	—	—	—	—

TABLE 16-5: BAUD RATES FOR ASYNCHRONOUS MODES

						SYNC = 0,	BRGH = (D					
BAUD	Fos	c = 8.00	0 MHz	Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fos	Fosc = 1.000 MHz		
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	
300		_	_	300	0.16	207	300	0.00	191	300	0.16	51	
1200	1202	0.16	103	1202	0.16	51	1200	0.00	47	1202	0.16	12	
2400	2404	0.16	51	2404	0.16	25	2400	0.00	23	_	_	—	
9600	9615	0.16	12	—	_	_	9600	0.00	5	_	_	—	
10417	10417	0.00	11	10417	0.00	5	—	_	_	—	_	_	
19.2k		_	_	—	_	_	19.20k	0.00	2	—	_	_	
57.6k	—	—	—	—	—	_	57.60k	0.00	0	—	—	—	
115.2k	—	—	_	—	—	_	_	—	_	_	—	_	

						SYNC = 0,	BRGH = 2	1				
BAUD	Fosc	= 20.00	0 MHz	Fosc = 18.432 MHz			Fosc = 16.0000 MHz			Fosc	= 11.059	92 MHz
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	—	_	_	_		_		_	—	_	_	—
1200	—	—	—	—	—	—	—	—	—	—	—	—
2400	—	—	—	—	—	—	—	—	—	—	_	_
9600	9615	0.16	129	9600	0.00	119	9615	0.16	103	9600	0.00	71
10417	10417	0.00	119	10378	-0.37	110	10417	0.00	95	10473	0.53	65
19.2k	19.23k	0.16	64	19.20k	0.00	59	19.23k	0.16	51	19.20k	0.00	35
57.6k	56.82k	-1.36	21	57.60k	0.00	19	58.8k	2.12	16	57.60k	0.00	11
115.2k	113.64k	-1.36	10	115.2k	0.00	9	—	_	_	115.2k	0.00	5

16.3.1.4 Synchronous Master Reception

Data is received at the RX/DT pin. The RX/DT pin output driver is automatically disabled when the AUSART is configured for synchronous master receive operation.

In Synchronous mode, reception is enabled by setting either the Single Receive Enable bit (SREN of the RCSTA register) or the Continuous Receive Enable bit (CREN of the RCSTA register).

When SREN is set and CREN is clear, only as many clock cycles are generated as there are data bits in a single character. The SREN bit is automatically cleared at the completion of one character. When CREN is set, clocks are continuously generated until CREN is cleared. If CREN is cleared in the middle of a character the CK clock stops immediately and the partial character is discarded. If SREN and CREN are both set, then SREN is cleared at the completion of the first character and CREN takes precedence.

To initiate reception, set either SREN or CREN. Data is sampled at the RX/DT pin on the trailing edge of the TX/CK clock pin and is shifted into the Receive Shift Register (RSR). When a complete character is received into the RSR, the RCIF bit of the PIR1 register is set and the character is automatically transferred to the two character receive FIFO. The Least Significant eight bits of the top character in the receive FIFO are available in RCREG. The RCIF bit remains set as long as there are unread characters in the receive FIFO.

16.3.1.5 Slave Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a slave receives the clock on the TX/CK line. The TX/ CK pin output driver is automatically disabled when the device is configured for synchronous slave transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One data bit is transferred for each clock cycle. Only as many clock cycles should be received as there are data bits.

16.3.1.6 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before RCREG is read to access the FIFO. When this happens the OERR bit of the RCSTA register is set. Previous data in the FIFO will not be overwritten. The two characters in the FIFO buffer can be read, however, no additional characters will be received until the error is cleared. The OERR bit can only be cleared by clearing the overrun condition. If the overrun error occurred when the SREN bit is set and CREN is clear then the error is cleared by reading RCREG. If the overrun occurred when the CREN bit is set then the error condition is cleared by either clearing the CREN bit of the RCSTA register.

16.3.1.7 Receiving 9-bit Characters

The AUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set, the AUSART will shift 9-bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth, and Most Significant, data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREG.

Address detection in Synchronous modes is not supported, therefore, the ADDEN bit of the RCSTA register must be cleared.

16.3.1.8 Synchronous Master Reception Setup:

- 1. Initialize the SPBRG register for the appropriate baud rate. Set or clear the BRGH bit, as required, to achieve the desired baud rate.
- 2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
- 3. Ensure bits CREN and SREN are clear.
- 4. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 5. If 9-bit reception is desired, set bit RX9.
- 6. Verify address detection is disabled by clearing the ADDEN bit of the RCSTA register.
- 7. Start reception by setting the SREN bit or for continuous reception, set the CREN bit.
- Interrupt flag bit RCIF of the PIR1 register will be set when reception of a character is complete. An interrupt will be generated if the RCIE interrupt enable bit of the PIE1 register was set.
- 9. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- 10. Read the 8-bit received data by reading the RCREG register.
- 11. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit, which resets the AUSART.

16.3.2 SYNCHRONOUS SLAVE MODE

The following bits are used to configure the AUSART for Synchronous slave operation:

- SYNC = 1
- CSRC = 0
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXSTA register configures the device for synchronous operation. Clearing the CSRC bit of the TXSTA register configures the device as a slave. Clearing the SREN and CREN bits of the RCSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCSTA register enables the AUSART.

16.3.2.1 AUSART Synchronous Slave Transmit

The operation of the Synchronous Master and Slave modes are identical (refer to **Section 16.3.1.2 "Synchronous Master Transmission")**, except in the case of the Sleep mode. If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

- 1. The first character will immediately transfer to the TSR register and transmit.
- 2. The second word will remain in TXREG register.
- 3. The TXIF bit will not be set.
- After the first character has been shifted out of TSR, the TXREG register will transfer the second character to the TSR and the TXIF bit will now be set.
- If the PEIE and TXIE bits are set, the interrupt will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will call the Interrupt Service Routine.
- 16.3.2.2 Synchronous Slave Transmission Setup:
- 1. Set the SYNC and SPEN bits and clear the CSRC bit.
- 2. Clear the CREN and SREN bits.
- If using interrupts, ensure that the GIE and PEIE bits of the INTCON register are set and set the TXIE bit.
- 4. If 9-bit transmission is desired, set the TX9 bit.
- 5. Enable transmission by setting the TXEN bit.
- 6. Verify address detection is disabled by clearing the ADDEN bit of the RCSTA register.
- 7. If 9-bit transmission is selected, insert the Most Significant bit into the TX9D bit.
- 8. Start transmission by writing the Least Significant eight bits to the TXREG register.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000X	0000 000X
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
TXREG	AUSART T	ransmit Dat	ta Register						0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010

TABLE 16-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Synchronous Slave Transmission.

17.1.2 SLAVE MODE

For any SPI device acting as a slave, the data is transmitted and received as external clock pulses appear on SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

17.1.2.1 Slave Mode Operation

The SSP consists of a transmit/receive shift register (SSPSR) and a buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPBUF holds the data that was written to the SSPSR until the received data is ready.

The slave has no control as to when data will be clocked in or out of the device. All data that is to be transmitted, to a master or another slave, must be loaded into the SSPBUF register before the first clock pulse is received.

Once eight bits of data have been received:

- · Received byte is moved to the SSPBUF register
- BF bit of the SSPSTAT register is set
- SSPIF bit of the PIR1 register is set

Any write to the SSPBUF register during transmission/reception of data will be ignored and the Write Collision Detect bit, WCOL of the SSPCON register, will be set. User software must clear the WCOL bit so that it can be determined if the following write(s) to the SSPBUF register completed successfully.

The user's firmware must read SSPBUF, clearing the BF flag, or the SSPOV bit of the SSPCON register will be set with the reception of the next byte and communication will be disabled.

A SPI module transmits and receives at the same time, occasionally causing dummy data to be transmitted/received. It is up to the user to determine which data is to be used and what can be discarded.

17.1.2.2 Enabling Slave I/O

To enable the serial port, the SSPEN bit of the SSPCON register must be set. If a Slave mode of operation is selected in the SSPM bits of the SSPCON register, the SDI, SDO, SCK pins will be assigned as serial port pins.

For these pins to function as serial port pins, they must have their corresponding data direction bits set or cleared in the associated TRIS register as follows:

- · SDI configured as input
- · SDO configured as output
- · SCK configured as input

Optionally, a fourth pin, Slave Select (\overline{SS}) may be used in Slave mode. Slave Select may be configured to operate on one of the following pins via the SSSEL bit in the APFCON register.

- RA5/AN4/SS
- RA0/AN0/SS

Upon selection of a Slave Select pin, the appropriate bits must be set in the ANSELA and TRISA registers. Slave Select must be set as an input by setting the corresponding bit in TRISA, and digital I/O must be enabled on the SS pin by clearing the corresponding bit of the ANSELA register.

17.1.2.3 Slave Mode Setup

When initializing the SSP module to SPI Slave mode, compatibility must be ensured with the master device. This is done by programming the appropriate control bits of the SSPCON and SSPSTAT registers. These control bits allow the following to be specified:

- · SCK as clock input
- Idle state of SCK (CKP bit)
- Data input sample phase (SMP bit)
- Output data on rising/falling edge of SCK (CKE bit)

Figure 17-4 and Figure 17-5 show example waveforms of Slave mode operation.

17.2.5 RECEPTION

When the R/\overline{W} bit of the received address byte is clear, the master will write data to the slave. If an address match occurs, the received address is loaded into the SSPBUF register. An address byte overflow will occur if that loaded address is not read from the SSPBUF before the next complete byte is received.

An SSP interrupt is generated for each data transfer byte. The BF, R/\overline{W} and D/\overline{A} bits of the SSPSTAT register are used to determine the status of the last received byte.

FIGURE 17-10: I²C WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)

R/	$\overline{W} = 0$	
SDA 1 A7XA6XA5XA4XA3XA2XA1	ACK Receiving Data ACK Receiving Data //D7\D6\D5\D4\D3\D2\D1\D0_/D7\D6\D5\D4\D3\	
	3_91_2_3_4_5_6_7_8_9_1_2_3_4_5_	/6_/7_/8 _ _/9_/ [!] ₽ [!] I
SSPIF	Cleared in software	Bus Master sends Stop
BF	 SSPBUF register is read 	
SSPOV		
	Bit SSPOV is set because the SSPBUF register is	s still full. 🗕
		s not sent.

REGISTER 18-4: PMADRH: PROGRAM MEMORY ADDRESS HIGH REGISTER

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	— — PMA12		PMA11	PMA10	PMA9	PMA8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 Unimplemented: Read as '0'

bit 4-0 PMA<12:8>: Program Memory Read Address bits

REGISTER 18-5: PMADRL: PROGRAM MEMORY ADDRESS LOW REGISTER

| R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PMA7 | PMA6 | PMA5 | PMA4 | PMA3 | PMA2 | PMA1 | PMA0 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PMA<7:0>:** Program Memory Read Address bits

TABLE 18-1: SUMMARY OF REGISTERS ASSOCIATED WITH PROGRAM MEMORY READ

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
PMCON1	Reserved	-	—	—	—	—	—	RD	1 0	10
PMADRH	—	_	_	Program I	Memory Re	ead Addres	x xxxx	x xxxx		
PMADRL	Program N	lemory Re	ad Address	s Register I	Low Byte				XXXX XXXX	XXXX XXXX
PMDATH	—	_	Program	rogram Memory Read Data Register High Byte					xx xxxx	xx xxxx
PMDATL	Program N	lemory Re	ad Data Re	egister Low	v Byte				xxxx xxxx	xxxx xxxx

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Program Memory Read.

23.6 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

Т			
F	Frequency	Т	Time
Lowercase letters (pp) and their meanings:			
рр			
сс	CCP1	OSC	OSC1
ck	CLKOUT	rd	RD
CS	CS	rw	RD or WR
di	SDI	SC	SCK
do	SDO	SS	SS
dt	Data in	tO	TOCKI
io	I/O PORT	t1	T1CKI
mc	MCLR	wr	WR
Uppercase letters and their meanings:			
S			
F	Fall	Р	Period
Н	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance

FIGURE 23-2: LOAD CONDITIONS



23.7 AC Characteristics: PIC16F72X-I/E



FIGURE 23-3: CLOCK TIMING





PIC16(L)F722/3/4/6/7



















FIGURE 24-65: PIC16F722/3/4/6/7 CAP SENSOR HYSTERESIS, POWER MODE = HIGH



