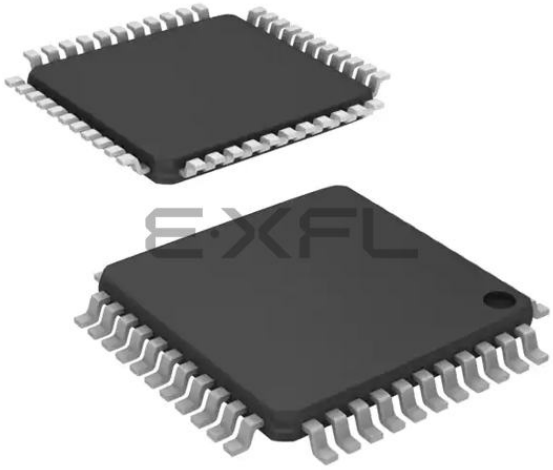

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf724-i-pt

TABLE 2: 40/44-PIN PDIP/TQFP/QFN SUMMARY (PIC16F724/727/PIC16LF724/727)

I/O	40-Pin PDIP	44-Pin TQFP	44-Pin QFN	A/D	Cap Sensor	Timers	CCP	AUSART	SSP	Interrupt	Pull-Up	Basic
RA0	2	19	19	AN0	—	—	—	—	$\overline{SS}$(3)	—	—	V_{CAP}(4)
RA1	3	20	20	AN1	—	—	—	—	—	—	—	—
RA2	4	21	21	AN2	—	—	—	—	—	—	—	—
RA3	5	22	22	AN3/V_{REF}	—	—	—	—	—	—	—	—
RA4	6	23	23	—	CPS6	T0CKI	—	—	—	—	—	—
RA5	7	24	24	AN4	CPS7	—	—	—	$\overline{SS}$(3)	—	—	V_{CAP}(4)
RA6	14	31	33	—	—	—	—	—	—	—	—	OSC2/CLKOUT/V_{CAP}(4)
RA7	13	30	32	—	—	—	—	—	—	—	—	OSC1/CLKIN
RB0	33	8	9	AN12	CPS0	—	—	—	—	IOC/INT	Y	—
RB1	34	9	10	AN10	CPS1	—	—	—	—	IOC	Y	—
RB2	35	10	11	AN8	CPS2	—	—	—	—	IOC	Y	—
RB3	36	11	12	AN9	CPS3	—	CCP2(2)	—	—	IOC	Y	—
RB4	37	14	14	AN11	CPS4	—	—	—	—	IOC	Y	—
RB5	38	15	15	AN13	CPS5	T1G	—	—	—	IOC	Y	—
RB6	39	16	16	—	—	—	—	—	—	IOC	Y	ICSPCLK/ICDCLK
RB7	40	17	17	—	—	—	—	—	—	IOC	Y	ICSPDAT/ICDDAT
RC0	15	32	34	—	—	T1OSO/ T1CKI	—	—	—	—	—	—
RC1	16	35	35	—	—	T1OSI	CCP2(2)	—	—	—	—	—
RC2	17	36	36	—	—	—	CCP1	—	—	—	—	—
RC3	18	37	37	—	—	—	—	—	SCK/SCL	—	—	—
RC4	23	42	42	—	—		—	—	SDI/SDA	—	—	—
RC5	24	43	43	—	—		—	—	SDO	—	—	—
RC6	25	44	44	—	—	—	—	TX/CK	—	—	—	—
RC7	26	1	1	—	—	—	—	RX/DT	—	—	—	—
RD0	19	38	38	—	CPS8	—	—	—	—	—	—	—
RD1	20	39	39	—	CPS9	—	—	—	—	—	—	—
RD2	21	40	40	—	CPS10	—	—	—	—	—	—	—
RD3	22	41	41	—	CPS11	—	—	—	—	—	—	—
RD4	27	2	2	—	CPS12	—	—	—	—	—	—	—
RD5	28	3	3	—	CPS13	—	—	—	—	—	—	—
RD6	29	4	4	—	CPS14	—	—	—	—	—	—	—
RD7	30	5	5	—	CPS15	—	—	—	—	—	—	—
RE0	8	25	25	AN5	—	—	—	—	—	—	—	—
RE1	9	26	26	AN6	—	—	—	—	—	—	—	—
RE2	10	27	27	AN7	—	—	—	—	—	—	—	—
RE3	1	18	18	—	—	—	—	—	—	—	Y(1)	$\overline{MCLR}$/V_{PP}
—	11,32	7,28	7,8,28	—	—	—	—	—	—	—	—	V_{DD}
—	12,13	6,29	6,30,31	—	—	—	—	—	—	—	—	V_{SS}

Note 1: Pull-up enabled only with external $\overline{MCLR}$ configuration.
2: RC1 is the default pin location for CCP2. RB3 may be selected by changing the CCP2SEL bit in the APFCON register.
3: RA5 is the default pin location for $\overline{SS}$. RA0 may be selected by changing the SSSEL bit in the APFCON register.
4: PIC16F722/3/4/6/7 devices only.

Note: The PIC16F722/3/4/6/7 devices have an internal low dropout voltage regulator. An external capacitor must be connected to one of the available V_{CAP} pins to stabilize the regulator. For more information, see **Section 5.0 "Low Dropout (LDO) Voltage Regulator"**. The PIC16LF722/3/4/6/7 devices do not have the voltage regulator and therefore no external capacitor is required.

TABLE 1-1: PIC16(L)F722/3/4/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB4/AN11/CPS4	RB4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN11	AN	—	A/D Channel 11 input.
	CPS4	AN	—	Capacitive sensing input 4.
RB5/AN13/CPS5/T1G	RB5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN13	AN	—	A/D Channel 13 input.
	CPS5	AN	—	Capacitive sensing input 5.
	T1G	ST	—	Timer1 Gate input.
RB6/ICSPCLK/ICDCLK	RB6	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	ICSPCLK	ST	—	Serial Programming Clock.
	ICDCLK	ST	—	In-Circuit Debug Clock.
RB7/ICSPDAT/ICDDAT	RB7	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
	ICDDAT	ST	—	In-Circuit Data I/O.
RC0/T1OSO/T1CKI	RC0	ST	CMOS	General purpose I/O.
	T1OSO	XTAL	XTAL	Timer1 oscillator connection.
	T1CKI	ST	—	Timer1 clock input.
RC1/T1OSI/CCP2	RC1	ST	CMOS	General purpose I/O.
	T1OSI	XTAL	XTAL	Timer1 oscillator connection.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
RC2/CCP1	RC2	ST	CMOS	General purpose I/O.
	CCP1	ST	CMOS	Capture/Compare/PWM1.
RC3/SCK/SCL	RC3	ST	CMOS	General purpose I/O.
	SCK	ST	CMOS	SPI clock.
	SCL	I^2C	OD	I^2C clock.
RC4/SDI/SDA	RC4	ST	CMOS	General purpose I/O.
	SDI	ST	—	SPI data input.
	SDA	I^2C	OD	I^2C data input/output.
RC5/SDO	RC5	ST	CMOS	General purpose I/O.
	SDO	—	CMOS	SPI data output.
RC6/TX/CK	RC6	ST	CMOS	General purpose I/O.
	TX	—	CMOS	USART asynchronous transmit.
	CK	ST	CMOS	USART synchronous clock.
RC7/RX/DT	RC7	ST	CMOS	General purpose I/O.
	RX	ST	—	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
RD0/CPS8	RD0	ST	CMOS	General purpose I/O.
	CPS8	AN	—	Capacitive sensing input 8.
RD1/CPS9	RD1	ST	CMOS	General purpose I/O.
	CPS9	AN	—	Capacitive sensing input 9.
RD2/CPS10	RD2	ST	CMOS	General purpose I/O.
	CPS10	AN	—	Capacitive sensing input 10.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

FIGURE 2-5: PIC16F723/LF723 AND PIC16F724/LF724 SPECIAL FUNCTION REGISTERS

	Bank 0		Bank 1		Bank 2		Bank 3	
File Address								
	Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
	TMR0	01h	OPTION	81h	TMR0	101h	OPTION	181h
	PCL	02h	PCL	82h	PCL	102h	PCL	182h
	STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
	FSR	04h	FSR	84h	FSR	104h	FSR	184h
	PORTA	05h	TRISA	85h		105h	ANSELA	185h
	PORTB	06h	TRISB	86h		106h	ANSELB	186h
	PORTC	07h	TRISC	87h		107h		187h
	PORTD(1)	08h	TRISD(1)	88h	CPSCON0	108h	ANSELD(1)	188h
	PORTE	09h	TRISE	89h	CPSCON1	109h	ANSELE(1)	189h
	PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
	INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
	PIR1	0Ch	PIE1	8Ch	PMDATL	10Ch	PMCON1	18Ch
	PIR2	0Dh	PIE2	8Dh	PMADRL	10Dh	Reserved	18Dh
	TMR1L	0Eh	PCON	8Eh	PMDATH	10Eh	Reserved	18Eh
	TMR1H	0Fh	T1GCON	8Fh	PMADRH	10Fh	Reserved	18Fh
	T1CON	10h	OSCCON	90h		110h		190h
	TMR2	11h	OSCTUNE	91h		111h		191h
	T2CON	12h	PR2	92h		112h		192h
	SSPBUF	13h	SSPADD/SSPMSK	93h		113h		193h
	SSPCON	14h	SSPSTAT	94h		114h		194h
	CCPR1L	15h	WPUB	95h		115h		195h
	CCPR1H	16h	IOCB	96h		116h		196h
	CCP1CON	17h		97h		117h		197h
	RCSTA	18h	TXSTA	98h		118h		198h
	TXREG	19h	SPBRG	99h		119h		199h
	RCREG	1Ah		9Ah		11Ah		19Ah
	CCPR2L	1Bh		9Bh		11Bh		19Bh
	CCPR2H	1Ch	APFCON	9Ch		11Ch		19Ch
	CCP2CON	1Dh	FVRCON	9Dh		11Dh		19Dh
	ADRES	1Eh		9Eh		11Eh		19Eh
	ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
	General Purpose Register 96 Bytes	20h – 7Fh	General Purpose Register 80 Bytes	A0h – EFh	General Purpose Register 16 Bytes	120h – 12Fh		1A0h – 1EFh
						130h – 16Fh		
			Accesses 70h-7Fh	F0h – FFh	Accesses 70h-7Fh	170h – 17Fh	Accesses 70h-7Fh	1F0h – 1FFh

Legend: = Unimplemented data memory locations, read as '0'.
* = Not a physical register.

Note 1: PORTD, TRISD, ANSELD and ANSELE are not implemented on the PIC16F723/LF723, read as '0'

6.0 I/O PORTS

There are as many as 35 general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

6.1 Alternate Pin Function

The Alternate Pin Function Control (APFCON) register is used to steer specific peripheral input and output functions between different pins. The APFCON register is shown in Register 6-1. For this device family, the following functions can be moved between different pins.

- $\overline{SS}$ (Slave Select)
- CCP2

REGISTER 6-1: APFCON: ALTERNATE PIN FUNCTION CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	SSSEL	CCP2SEL
bit 7							bit 0

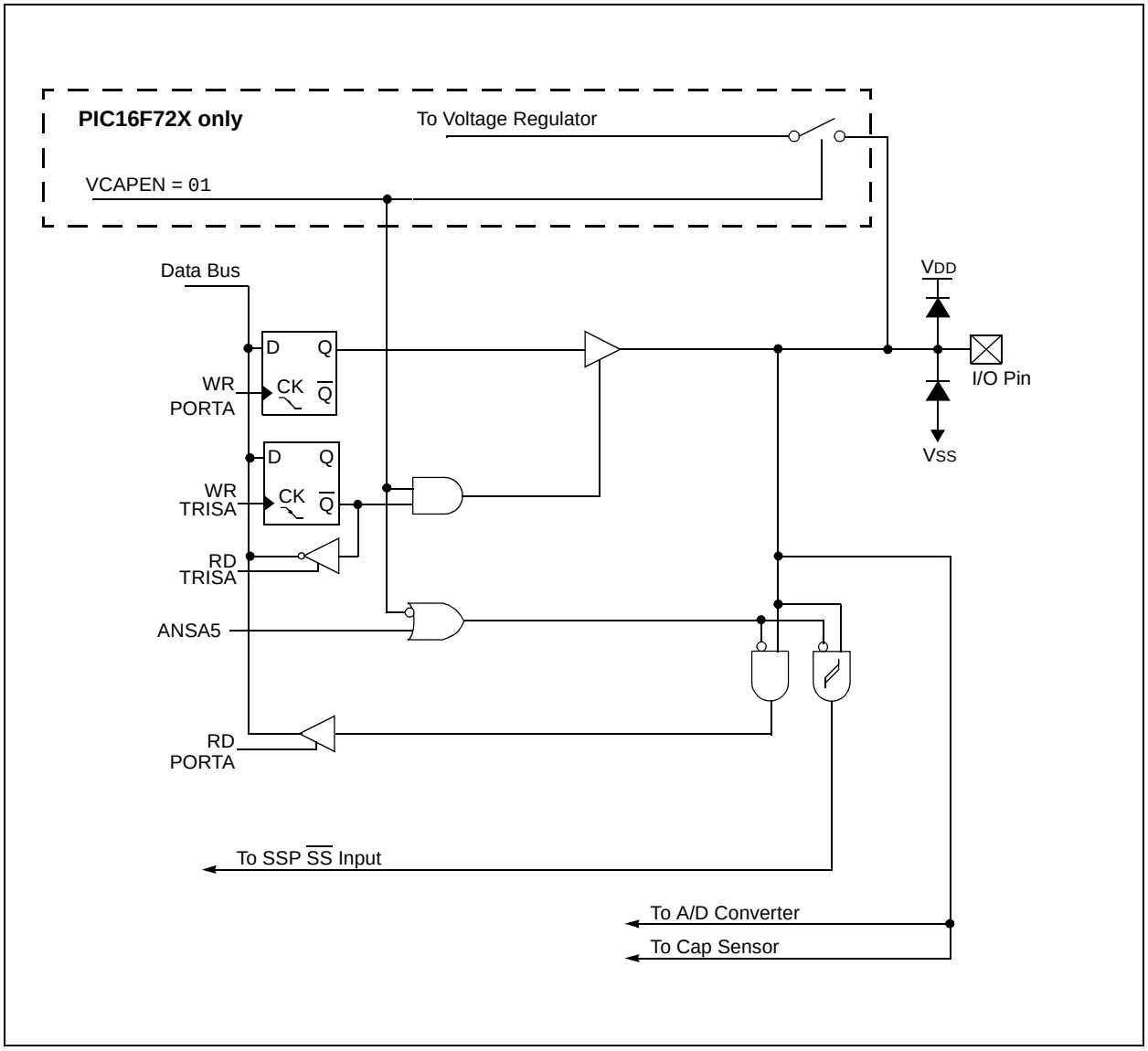
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as ‘0’.

bit 1 **SSSEL:** $\overline{SS}$ Input Pin Selection bit
0 = $\overline{SS}$ function is on RA5/AN4/CPS7/$\overline{SS}$/V_{CAP}
1 = $\overline{SS}$ function is on RA0/AN0/$\overline{SS}$/V_{CAP}

bit 0 **CCP2SEL:** CCP2 Input/Output Pin Selection bit
0 = CCP2 function is on RC1/T1OSI/CCP2
1 = CCP2 function is on RB3/CCP2

FIGURE 6-4: BLOCK DIAGRAM OF RA5



6.6 PORTE and TRISE Registers

PORTE is a 4-bit wide, bidirectional port. The corresponding data direction register is TRISE. Setting a TRISE bit (= 1) will make the corresponding PORTE pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISE bit (= 0) will make the corresponding PORTE pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). The exception is RE3, which is input only and its TRIS bit will always read as '1'. Example 6-5 shows how to initialize PORTE.

Reading the PORTE register (Register 6-15) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch. RE3 reads '0' when MCLRE = 1.

Note:	RE<2:0> and TRISE<2:0> are not implemented on the PIC16F722/723/726/ PIC16LF722/723/726. Read as '0'.

The TRISE register (Register 6-16) controls the PORTE pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISE register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

Note:	The ANSELE register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

EXAMPLE 6-5: INITIALIZING PORTE

```
BANKSEL PORTE        ;
CLRF    PORTE        ;Init PORTE
BANKSEL ANSELE       ;
CLRF    ANSELE       ;digital I/O
BANKSEL TRISE        ;
MOVLW   B'00001100'  ;Set RE<2> as an input
MOVWF   TRISE        ;and set RE<1:0>
                     ;as outputs
```

8.2 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using ICSP™ for verification purposes.

Note:	The entire Flash program memory will be erased when the code protection is turned off. See the "*PIC16(L)F72X Memory Programming Specification*" (DS41332) for more information.

8.3 User ID

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify mode. Only the Least Significant seven bits of the ID locations are reported when using MPLAB IDE. See the "*PIC16(L)F72X Memory Programming Specification*" (DS41332) for more information.

TABLE 9-1: ADC CLOCK PERIOD (T_{AD}) VS. DEVICE OPERATING FREQUENCIES

ADC Clock Period (T_{AD})		Device Frequency (F_{OSC})				
ADC Clock Source	**ADCS<2:0>**	**20 MHz**	**16 MHz**	**8 MHz**	**4 MHz**	**1 MHz**
Fosc/2	000	100 ns(2)	125 ns(2)	250 ns(2)	500 ns(2)	2.0 μs
Fosc/4	100	200 ns(2)	250 ns(2)	500 ns(2)	1.0 μs	4.0 μs
Fosc/8	001	400 ns(2)	0.5 μs(2)	1.0 μs	2.0 μs	8.0 μs(3)
Fosc/16	101	800 ns	1.0 μs	2.0 μs	4.0 μs	16.0 μs(3)
Fosc/32	010	1.6 μs	2.0 μs	4.0 μs	8.0 μs(3)	32.0 μs(3)
Fosc/64	110	3.2 μs	4.0 μs	8.0 μs(3)	16.0 μs(3)	64.0 μs(3)
FRC	x11	1.0-6.0 μs(1,4)	1.0-6.0 μs(1,4)	1.0-6.0 μs(1,4)	1.0-6.0 μs(1,4)	1.0-6.0 μs(1,4)

Legend: Shaded cells are outside of recommended range.

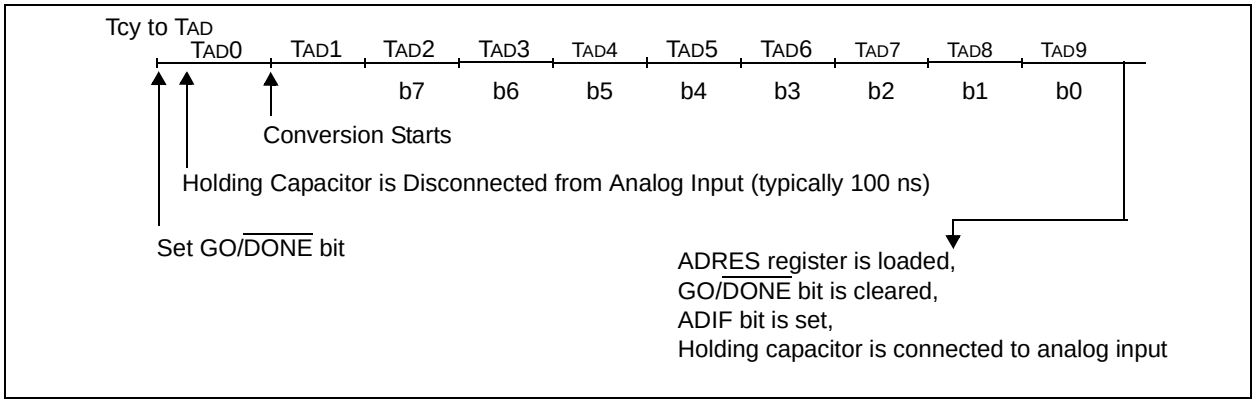
Note 1: The FRC source has a typical T_{AD} time of 1.6 μs for V_{DD}.

2: These values violate the minimum required T_{AD} time.

3: For faster conversion times, the selection of another clock source is recommended.

4: When the device frequency is greater than 1 MHz, the FRC clock source is only recommended if the conversion will be performed during Sleep.

FIGURE 9-2: ANALOG-TO-DIGITAL CONVERSION T_{AD} CYCLES



9.1.5 INTERRUPTS

The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital conversion. The ADC interrupt flag is the ADIF bit in the PIR1 register. The ADC interrupt enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

Note 1:	The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.
2:	The ADC operates during Sleep only when the FRC oscillator is selected.

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the GIE and PEIE bits of the INTCON register must be disabled. If the GIE and PEIE bits of the INTCON register are enabled, execution will switch to the Interrupt Service Routine.

Please refer to **Section 9.1.5 "Interrupts"** for more information.

9.2 ADC Operation

9.2.1 STARTING A CONVERSION

To enable the ADC module, the ADON bit of the ADCON0 register must be set to a '1'. Setting the GO/$\overline{\text{DONE}}$ bit of the ADCON0 register to a '1' will start the Analog-to-Digital conversion.

Note:	The GO/$\overline{\text{DONE}}$ bit should not be set in the same instruction that turns on the ADC. Refer to **Section 9.2.6 "A/D Conversion Procedure"**.

9.2.2 COMPLETION OF A CONVERSION

When the conversion is complete, the ADC module will:

- Clear the GO/$\overline{\text{DONE}}$ bit
- Set the ADIF Interrupt Flag bit
- Update the ADRES register with new conversion result

9.2.3 TERMINATING A CONVERSION

If a conversion must be terminated before completion, the GO/$\overline{\text{DONE}}$ bit can be cleared in software. The ADRES register will be updated with the partially complete Analog-to-Digital conversion sample. Incomplete bits will match the last bit converted.

Note:	A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.

9.2.4 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC clock source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than FRC, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.

9.2.5 SPECIAL EVENT TRIGGER

The Special Event Trigger of the CCP module allows periodic ADC measurements without software intervention. When this trigger occurs, the GO/$\overline{\text{DONE}}$ bit is set by hardware and the Timer1 counter resets to zero.

Using the Special Event Trigger does not assure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met.

Refer to **Section 15.0 "Capture/Compare/PWM (CCP) Module"** for more information.

REGISTER 9-2: ADCON1: A/D CONTROL REGISTER 1

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
—	ADCS2	ADCS1	ADCS0	—	—	ADREF1	ADREF0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **ADCS<2:0>:** A/D Conversion Clock Select bits
000 = FOSC/2
001 = FOSC/8
010 = FOSC/32
011 = FRC (clock supplied from a dedicated RC oscillator)
100 = FOSC/4
101 = FOSC/16
110 = FOSC/64
111 = FRC (clock supplied from a dedicated RC oscillator)

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1-0 **ADREF<1:0>:** Voltage Reference Configuration bits
0x = VREF is connected to VDD
10 = VREF is connected to external VREF (RA3/AN3)
11 = VREF is connected to internal Fixed Voltage Reference

REGISTER 9-3: ADRES: ADC RESULT REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
ADRES7	ADRES6	ADRES5	ADRES4	ADRES3	ADRES2	ADRES1	ADRES0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **ADRES<7:0>**: ADC Result Register bits
8-bit conversion result.

TABLE 12-6: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	--11 1111	--11 1111
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	xxxx xxxx
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	—	TMR1ON	0000 00-0	uuuu uu-u
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1$\overline{\text{GGO}}$/$\overline{\text{DONE}}$	T1GVAL	T1GSS1	T1GSS0	0000 0x00	uuuu uxuu

Legend: x = unknown, u = unchanged, – = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

15.3.4 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is ten bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 15-4.

EQUATION 15-4: PWM RESOLUTION

$$Resolution = \frac{log[4(PR2 + 1)]}{log(2)} \ bits$$

Note: If the pulse-width value is greater than the period, the assigned PWM pin(s) will remain unchanged.

TABLE 15-5: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 15-6: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

15.3.5 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCPx pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

15.3.6 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency (FOSC). Any changes in the system clock frequency will result in changes to the PWM frequency. Refer to **Section 7.0 "Oscillator Module"** for additional details.

15.3.7 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

15.3.8 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Disable the PWM pin (CCPx) output driver(s) by setting the associated TRIS bit(s).
2. Load the PR2 register with the PWM period value.
3. Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.
4. Load the CCPRxL register and the DCxBx bits of the CCPxCON register, with the PWM duty cycle value.
5. Configure and start Timer2:
   - Clear the TMR2IF interrupt flag bit of the PIR1 register. See Note below.
   - Configure the T2CKPS bits of the T2CON register with the Timer2 prescale value.
   - Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output pin:
   - Wait until Timer2 overflows, TMR2IF bit of the PIR1 register is set. See Note below.
   - Enable the PWM pin (CCPx) output driver(s) by clearing the associated TRIS bit(s).

Note: In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

16.1.2 AUSART ASYNCHRONOUS RECEIVER

The Asynchronous mode is typically used in RS-232 systems. The receiver block diagram is shown in Figure 16-2. The data is received on the RX/DT pin and drives the data recovery block. The data recovery block is actually a high-speed shifter operating at 16 times the baud rate, whereas the serial Receive Shift Register (RSR) operates at the bit rate. When all eight or nine bits of the character have been shifted in, they are immediately transferred to a two character First-In First-Out (FIFO) memory. The FIFO buffering allows reception of two complete characters and the start of a third character before software must start servicing the AUSART receiver. The FIFO and RSR registers are not directly accessible by software. Access to the received data is via the RCREG register.

16.1.2.1 Enabling the Receiver

The AUSART receiver is enabled for asynchronous operation by configuring the following three control bits:

- CREN = 1
- SYNC = 0
- SPEN = 1

All other AUSART control bits are assumed to be in their default state.

Setting the CREN bit of the RCSTA register enables the receiver circuitry of the AUSART. Clearing the SYNC bit of the TXSTA register configures the AUSART for asynchronous operation. Setting the SPEN bit of the RCSTA register enables the AUSART and automatically configures the RX/DT I/O pin as an input.

Note:	When the SPEN bit is set the TX/CK I/O pin is automatically configured as an output, regardless of the state of the corresponding TRIS bit and whether or not the AUSART transmitter is enabled. The PORT latch is disconnected from the output driver so it is not possible to use the TX/CK pin as a general purpose output.

16.1.2.2 Receiving Data

The receiver data recovery circuit initiates character reception on the falling edge of the first bit. The first bit, also known as the Start bit, is always a zero. The data recovery circuit counts one-half bit time to the center of the Start bit and verifies that the bit is still a zero. If it is not a zero then the data recovery circuit aborts character reception, without generating an error, and resumes looking for the falling edge of the Start bit. If the Start bit zero verification succeeds then the data recovery circuit counts a full bit time to the center of the next bit. The bit is then sampled by a majority detect circuit and the resulting '0' or '1' is shifted into the RSR. This repeats until all data bits have been sampled and shifted into the RSR. One final bit time is measured and the level sampled. This is the Stop bit, which is always a '1'. If the data recovery circuit samples a '0' in the Stop bit position then a framing error is set for this character, otherwise the framing error is cleared for this character. Refer to **Section 16.1.2.4 "Receive Framing Error"** for more information on framing errors.

Immediately after all data bits and the Stop bit have been received, the character in the RSR is transferred to the AUSART receive FIFO and the RCIF interrupt flag bit of the PIR1 register is set. The top character in the FIFO is transferred out of the FIFO by reading the RCREG register.

Note:	If the receive FIFO is overrun, no additional characters will be received until the overrun condition is cleared. Refer to **Section 16.1.2.5 "Receive Overrun Error"** for more information on overrun errors.

16.1.2.3 Receive Interrupts

The RCIF interrupt flag bit of the PIR1 register is set whenever the AUSART receiver is enabled and there is an unread character in the receive FIFO. The RCIF interrupt flag bit is read-only, it cannot be set or cleared by software.

RCIF interrupts are enabled by setting all of the following bits:

- RCIE interrupt enable bit of the PIE1 register
- PEIE peripheral interrupt enable bit of the INTCON register
- GIE global interrupt enable bit of the INTCON register

The RCIF interrupt flag bit of the PIR1 register will be set when there is an unread character in the FIFO, regardless of the state of interrupt enable bits.

17.1.2.4 Slave Select Operation

The $\overline{SS}$ pin allows Synchronous Slave mode operation. The SPI must be in Slave mode with $\overline{SS}$ pin control enabled (SSPM<3:0> = 0100). The associated TRIS bit for the $\overline{SS}$ pin must be set, making $\overline{SS}$ an input.

In Slave Select mode, when:

- $\overline{SS}$ = 0, The device operates as specified in **Section 17.1.2 "Slave Mode"**.
- $\overline{SS}$ = 1, The SPI module is held in Reset and the SDO pin will be tri-stated.

Note 1:	When the SPI is in Slave mode with $\overline{SS}$ pin control enabled (SSPM<3:0> = 0100), the SPI module will reset if the $\overline{SS}$ pin is driven high.
2:	If the SPI is used in Slave mode with CKE set, the $\overline{SS}$ pin control must be enabled.

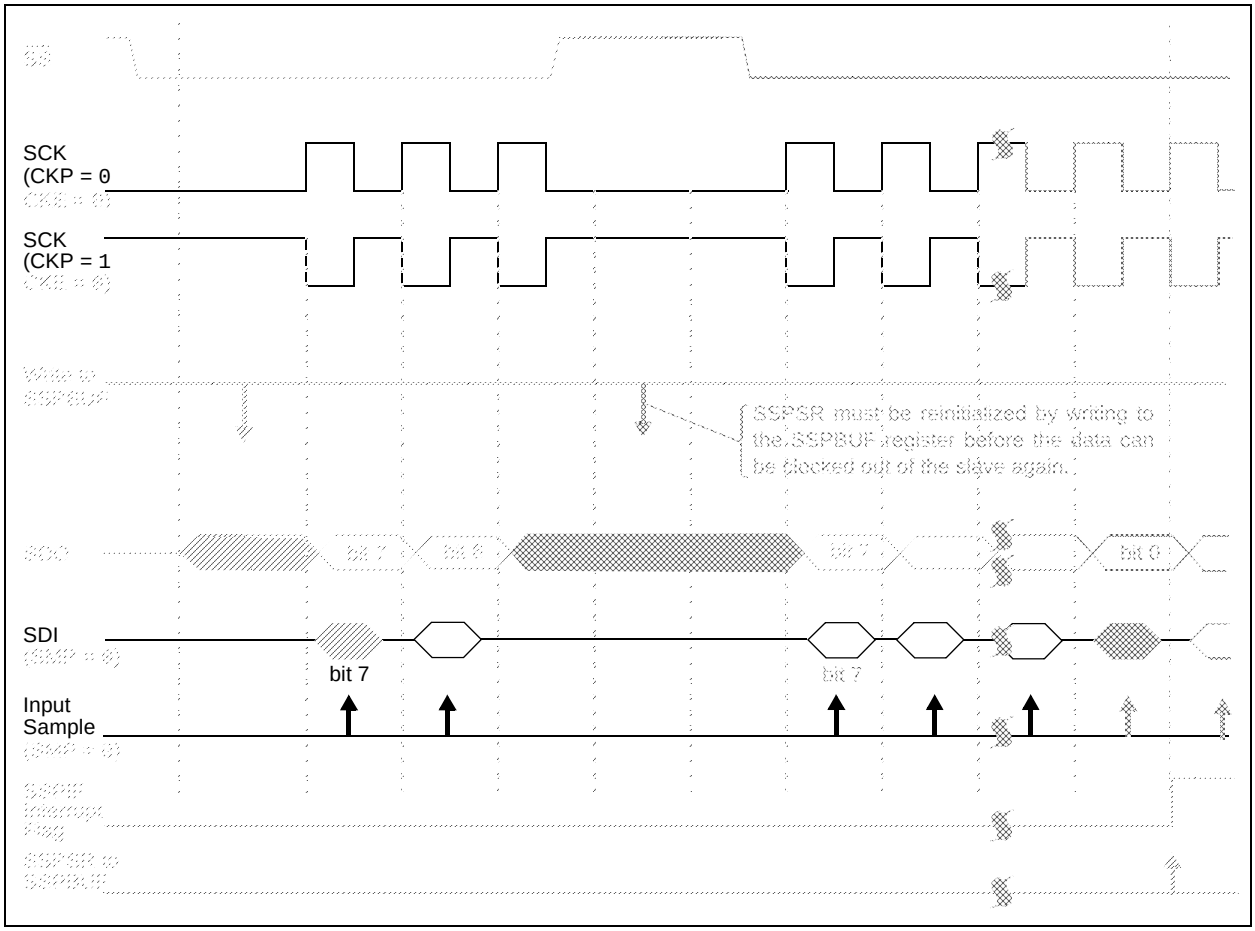
When the SPI module resets, the bit counter is cleared to '0'. This can be done by either forcing the $\overline{SS}$ pin to a high level or clearing the SSPEN bit. Figure 17-6 shows the timing waveform for such a synchronization event.

Note:	SSPSR must be reinitialized by writing to the SSPBUF register before the data can be clocked out of the slave again.

17.1.2.5 Sleep in Slave Mode

While in Sleep mode, the slave can transmit/receive data. The SPI Transmit/Receive Shift register operates asynchronously to the device on the externally supplied clock source. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all eight bits have been received, the SSP Interrupt Flag bit will be set and if enabled, will wake the device from Sleep.

FIGURE 17-6: SLAVE SELECT SYNCHRONIZATION WAVEFORM



23.1 DC Characteristics: PIC16(L)F722/3/4/6/7-I/E (Industrial, Extended)

PIC16LF722/3/4/6/7			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
PIC16F722/3/4/6/7			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**					
		PIC16LF722/3/4/6/7	1.8 1.8 2.3 2.5	— — — —	3.6 3.6 3.6 3.6	V V V V	FOSC ≤ 16 MHz: HFINTOSC, EC FOSC ≤ 4 MHz FOSC ≤ 20 MHz, EC FOSC ≤ 20 MHz, HS
D001		**PIC16F722/3/4/6/7**	1.8 1.8 2.3 2.5	— — — —	5.5 5.5 5.5 5.5	V V V V	FOSC ≤ 16 MHz: HFINTOSC, EC FOSC ≤ 4 MHz FOSC ≤ 20 MHz, EC FOSC ≤ 20 MHz, HS
D002*	VDR	**RAM Data Retention Voltage(1)**					
		PIC16LF722/3/4/6/7	1.5	—	—	V	Device in Sleep mode
D002*		**PIC16F722/3/4/6/7**	1.7	—	—	V	Device in Sleep mode
	VPOR*	**Power-on Reset Release Voltage**	—	1.6	—	V	
	VPORR*	**Power-on Reset Rearm Voltage**					
		PIC16LF722/3/4/6/7	—	0.8	—	V	Device in Sleep mode
		PIC16F722/3/4/6/7	—	1.7	—	V	Device in Sleep mode
D003	VFVR	**Fixed Voltage Reference Voltage, Initial Accuracy**	-8 -8 -8	— — —	6 6 6	% % %	VFVR = 1.024V, VDD ≥ 2.5V VFVR = 2.048V, VDD ≥ 2.5V VFVR = 4.096V, VDD ≥ 4.75V; -40 ≤ TA ≤ 85°C
			-8 -8 -8	— — —	6 6 6	% % %	VFVR = 1.024V, VDD ≥ 2.5V VFVR = 2.048V, VDD ≥ 2.5V VFVR = 4.096V, VDD ≥ 4.75V; -40 ≤ TA ≤ 125°C
D004*	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See **Section 3.2 "Power-on Reset (POR)"** for details.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

23.6 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

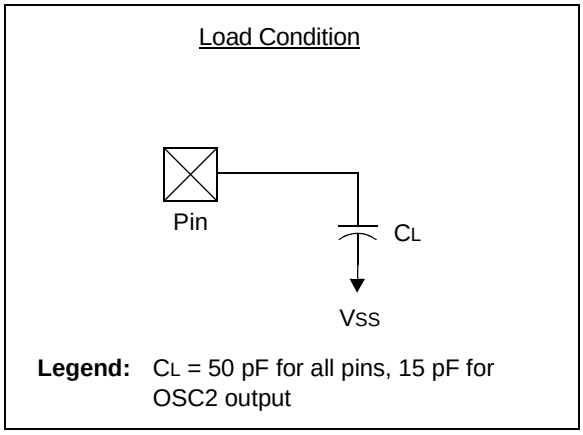
Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O PORT	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance

FIGURE 23-2: LOAD CONDITIONS



Legend: C_L = 50 pF for all pins, 15 pF for OSC2 output

FIGURE 24-7: PIC16F722/3/4/6/7 TYPICAL IDD vs. VDD OVER FOSC, EXTRC MODE, VCAP = 0.1 µF

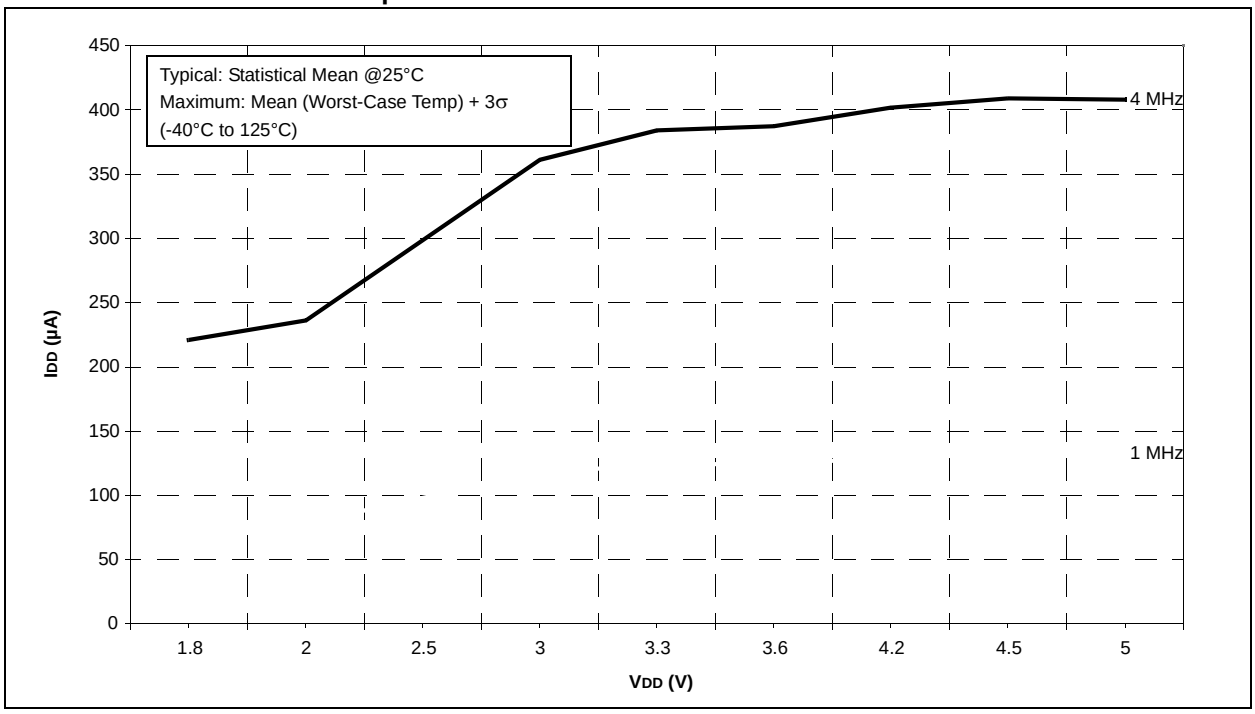


FIGURE 24-8: PIC16LF722/3/4/6/7 TYPICAL IDD vs. VDD OVER FOSC, EXTRC MODE

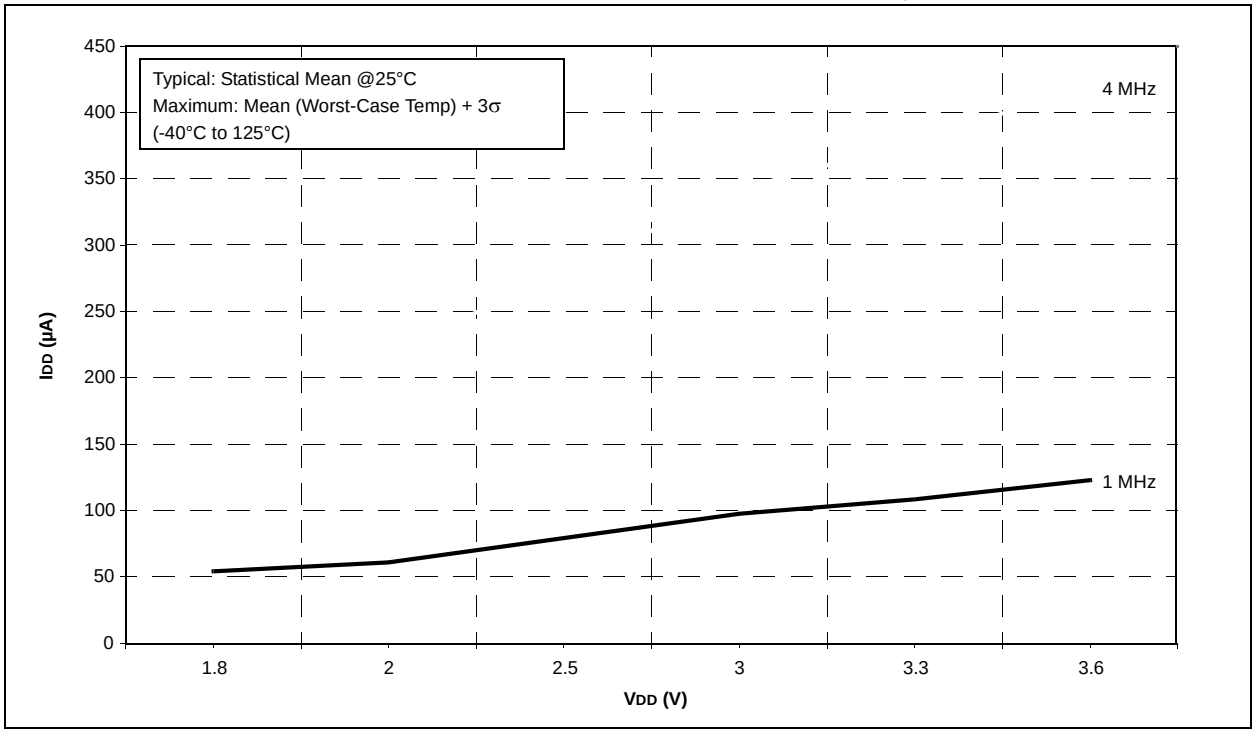


FIGURE 24-9: PIC16F722/3/4/6/7 MAXIMUM IDD vs. FOSC OVER VDD, HS MODE, VCAP = 0.1 µF

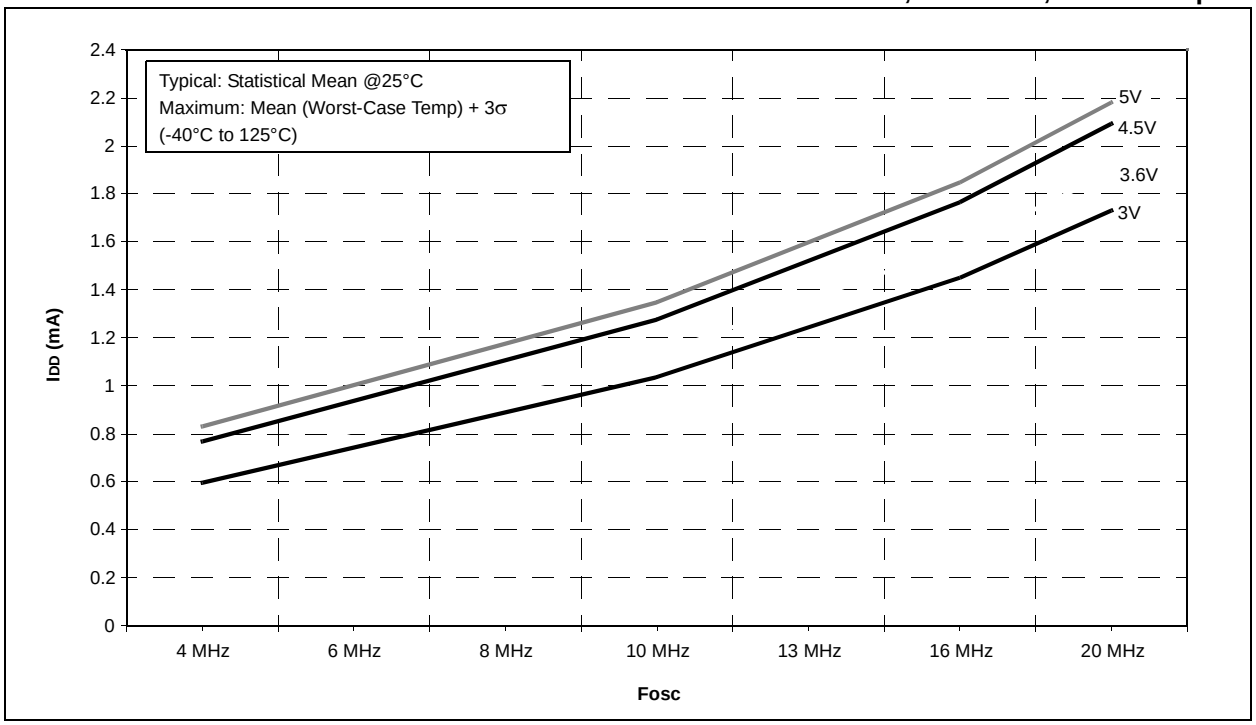


FIGURE 24-10: PIC16LF722/3/4/6/7 MAXIMUM IDD vs. FOSC OVER VDD, HS MODE

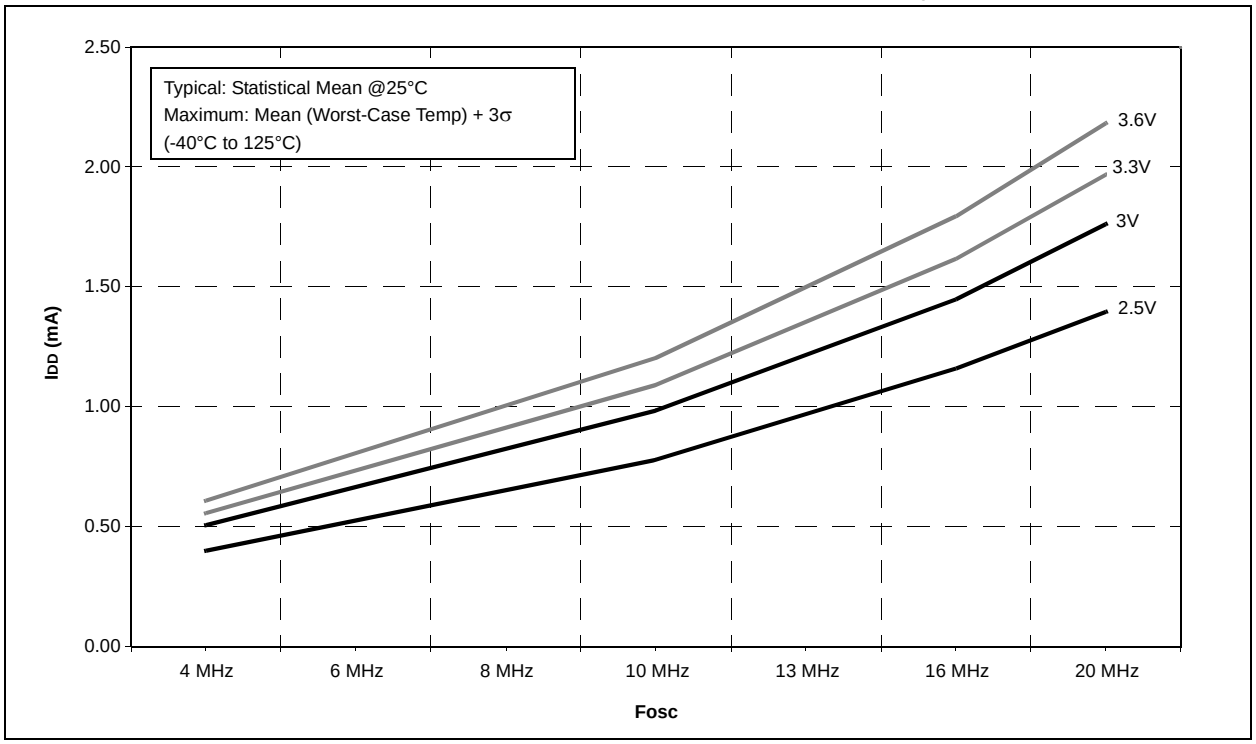


FIGURE 24-33: PIC16F722/3/4/6/7 BOR IPD vs. VDD, VCAP = 0.1 µF

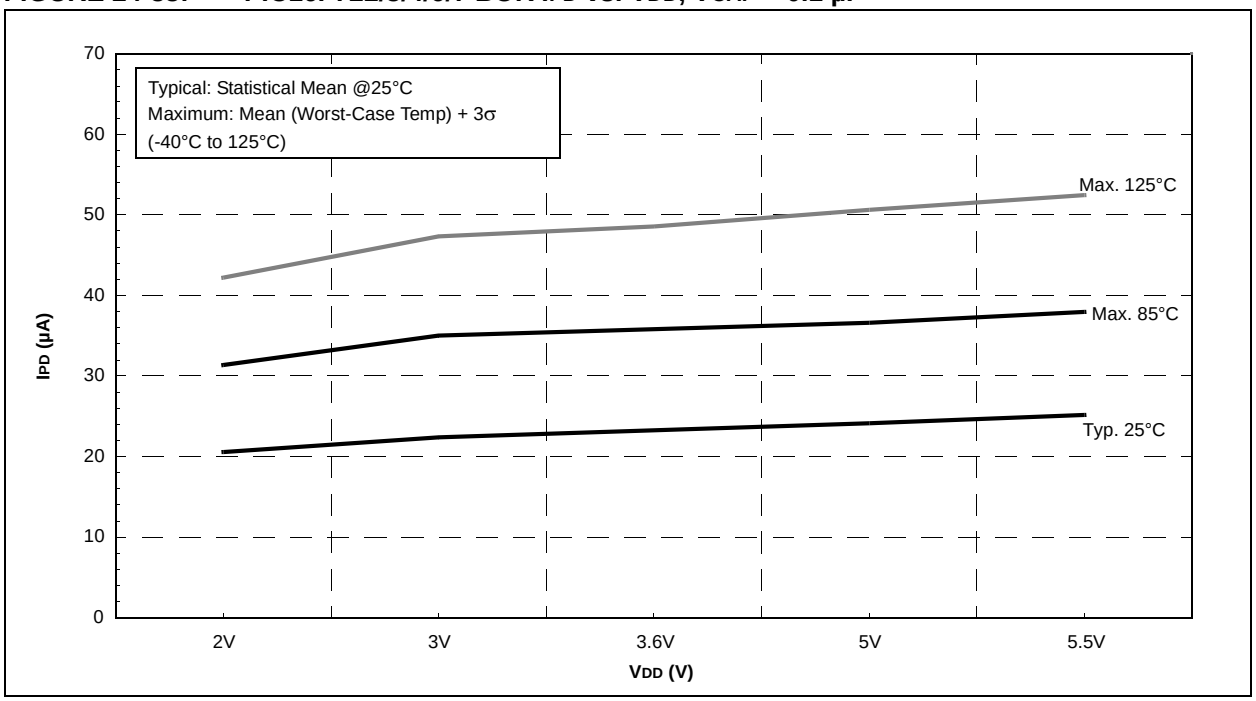


FIGURE 24-34: PIC16LF722/3/4/6/7 BOR IPD vs. VDD

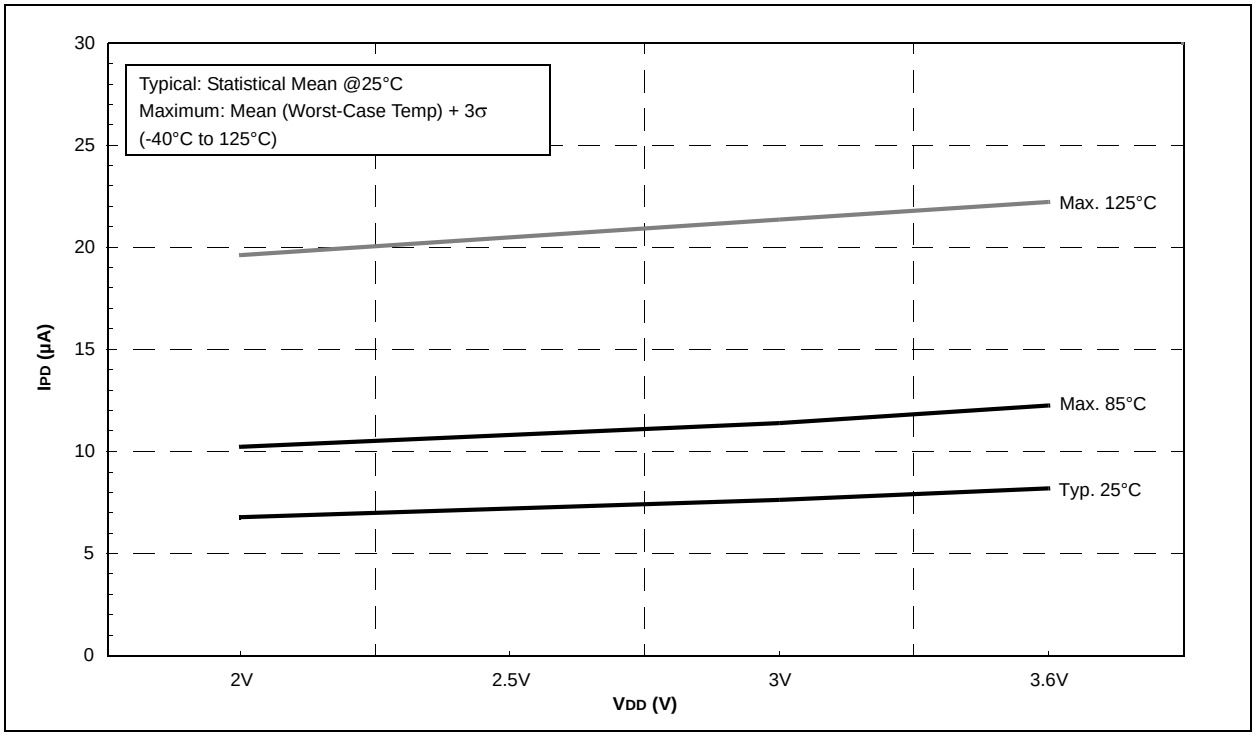


FIGURE 24-65: PIC16F722/3/4/6/7 CAP SENSOR HYSTERESIS, POWER MODE = HIGH

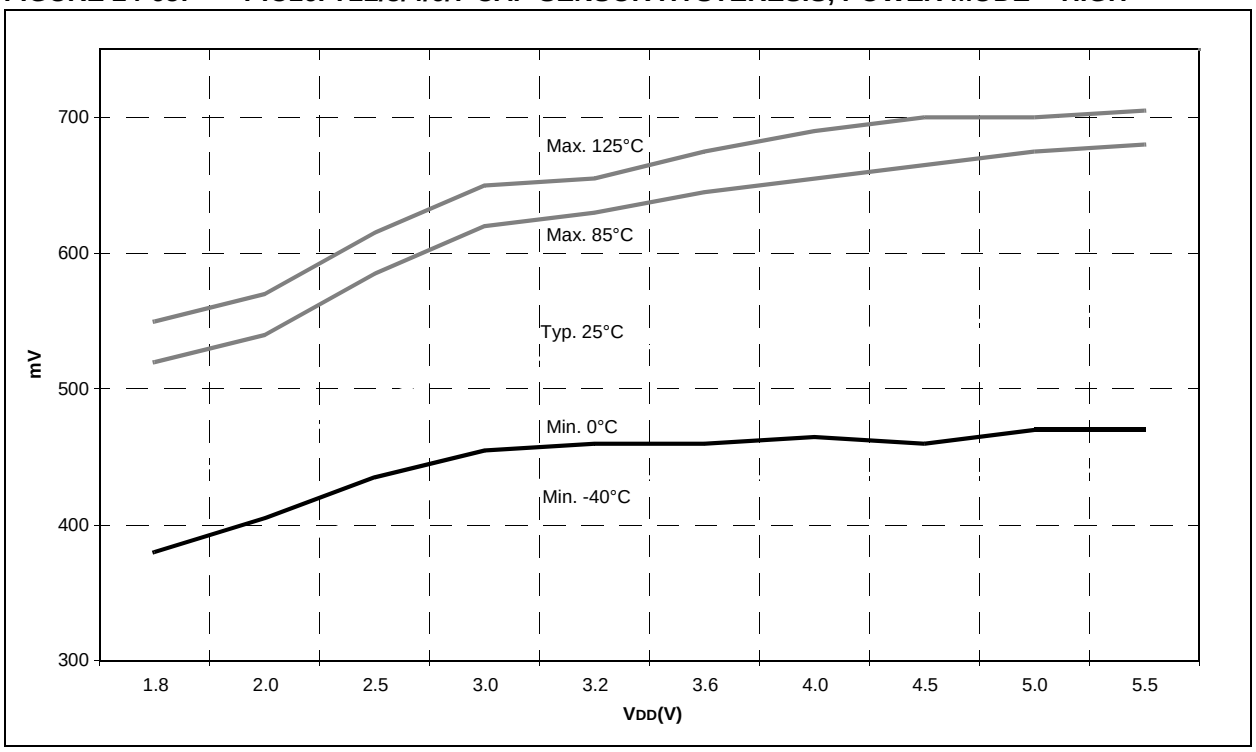


FIGURE 24-66: PIC16F722/3/4/6/7 CAP SENSOR HYSTERESIS, POWER MODE = MEDIUM