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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf724t-i-ml

PIC16(L)F722/3/4/6/7

FIGURE 2-6: PIC16F726/LF726 AND PIC16F727/LF727 SPECIAL FUNCTION REGISTERS

PIC16F726/PIC16LF726				PIC16F727/PIC16LF727				PIC16F728/PIC16LF728				PIC16F729/PIC16LF729				File Address			
Indirect addr. ^(*)		00h		Indirect addr. ^(*)		80h		Indirect addr. ^(*)		100h		Indirect addr. ^(*)		180h					
TMR0		01h		OPTION		81h		TMR0		101h		OPTION		181h					
PCL		02h		PCL		82h		PCL		102h		PCL		182h					
STATUS		03h		STATUS		83h		STATUS		103h		STATUS		183h					
FSR		04h		FSR		84h		FSR		104h		FSR		184h					
PORTA		05h		TRISA		85h				105h		ANSELA		185h					
PORTB		06h		TRISB		86h				106h		ANSELB		186h					
PORTC		07h		TRISC		87h				107h				187h					
PORTD ⁽¹⁾		08h		TRISD ⁽¹⁾		88h		CPSCON0		108h		ANSEL ⁽¹⁾		188h					
PORTE		09h		TRISE		89h		CPSCON1		109h		ANSELE ⁽¹⁾		189h					
PCLATH		0Ah		PCLATH		8Ah		PCLATH		10Ah		PCLATH		18Ah					
INTCON		0Bh		INTCON		8Bh		INTCON		10Bh		INTCON		18Bh					
PIR1		0Ch		PIE1		8Ch		PMDATL		10Ch		PMCON1		18Ch					
PIR2		0Dh		PIE2		8Dh		PMADRL		10Dh		Reserved		18Dh					
TMR1L		0Eh		PCON		8Eh		PMDATH		10Eh		Reserved		18Eh					
TMR1H		0Fh		T1GCON		8Fh		PMADRH		10Fh		Reserved		18Fh					
T1CON		10h		OSCCON		90h		General Purpose Register 16 Bytes		110h		General Purpose Register 16 Bytes		190h					
TMR2		11h		OSCTUNE		91h				111h				191h					
T2CON		12h		PR2		92h				112h				192h					
SSPBUF		13h		SSPAD ^D /SSPMSK		93h				113h				193h					
SSPCON		14h		SSPSTAT		94h				114h				194h					
CCPR1L		15h		WPUB		95h				115h				195h					
CCPR1H		16h		IOCB		96h				116h				196h					
CCP1CON		17h				97h				117h				197h					
RCSTA		18h		TXSTA		98h				118h				198h					
TXREG		19h		SPBRG		99h				119h				199h					
RCREG		1Ah				9Ah				11Ah				19Ah					
CCPR2L		1Bh				9Bh				11Bh				19Bh					
CCPR2H		1Ch		APFCON		9Ch				11Ch				19Ch					
CCP2CON		1Dh		FVRCON		9Dh				11Dh				19Dh					
ADRES		1Eh				9Eh				11Eh				19Eh					
ADCON0		1Fh		ADCON1		9Fh				11Fh				19Fh					
General Purpose Register 96 Bytes		20h		General Purpose Register 80 Bytes		A0h		General Purpose Register 80 Bytes		120h		General Purpose Register 80 Bytes		1A0h					
						EFh				16Fh				1EFh					
						F0h				170h				1F0h					
		7Fh				FFh				17Fh				1FFh					
Bank 0				Bank 1				Bank 2				Bank 3							

Legend: = Unimplemented data memory locations, read as '0',
* = Not a physical register

Note 1: PORTD, TRISD, ANSEL^D and ANSELE are not implemented on the PIC16F726/LF726, read as '0'

PIC16(L)F722/3/4/6/7

2.2.2.2 OPTION register

The OPTION register, shown in Register 2-2, is a readable and writable register, which contains various control bits to configure:

- Timer0/WDT prescaler
- External RB0/INT interrupt
- Timer0
- Weak pull-ups on PORTB

Note: To achieve a 1:1 prescaler assignment for Timer0, assign the prescaler to the WDT by setting the PSA bit of the OPTION_REG register to '1'. Refer to **Section 11.1.3 “Software Programmable Prescaler”**.

REGISTER 2-2: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBP}}\text{U}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **$\overline{\text{RBP}}\text{U}$:** PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual bits in the WPUB register
- bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin
- bit 5 **T0CS:** Timer0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (Fosc/4)
- bit 4 **T0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin
- bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module
- bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

PIC16(L)F722/3/4/6/7

REGISTER 4-1: INTCON: INTERRUPT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	TOIE	INTE	RBIE ⁽¹⁾	T0IF ⁽²⁾	INTF	RBIF
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7	GIE: Global Interrupt Enable bit 1 = Enables all unmasked interrupts 0 = Disables all interrupts
bit 6	PEIE: Peripheral Interrupt Enable bit 1 = Enables all unmasked peripheral interrupts 0 = Disables all peripheral interrupts
bit 5	TOIE: Timer0 Overflow Interrupt Enable bit 1 = Enables the Timer0 interrupt 0 = Disables the Timer0 interrupt
bit 4	INTE: RB0/INT External Interrupt Enable bit 1 = Enables the RB0/INT external interrupt 0 = Disables the RB0/INT external interrupt
bit 3	RBIE: PORTB Change Interrupt Enable bit ⁽¹⁾ 1 = Enables the PORTB change interrupt 0 = Disables the PORTB change interrupt
bit 2	T0IF: Timer0 Overflow Interrupt Flag bit ⁽²⁾ 1 = TMR0 register has overflowed (must be cleared in software) 0 = TMR0 register did not overflow
bit 1	INTF: RB0/INT External Interrupt Flag bit 1 = The RB0/INT external interrupt occurred (must be cleared in software) 0 = The RB0/INT external interrupt did not occur
bit 0	RBIF: PORTB Change Interrupt Flag bit 1 = When at least one of the PORTB general purpose I/O pins changed state (must be cleared in software) 0 = None of the PORTB general purpose I/O pins have changed state

Note 1: The appropriate bits in the IOCB register must also be set.

2: T0IF bit is set when Timer0 rolls over. Timer0 is unchanged on Reset and should be initialized before clearing T0IF bit.

PIC16(L)F722/3/4/6/7

4.5.3 PIE2 REGISTER

The PIE2 register contains the interrupt enable bits, as shown in Register 4-3.

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 4-3: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	CCP2IE
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-1

Unimplemented: Read as '0'

bit 0

CCP2IE: CCP2 Interrupt Enable bit

1 = Enables the CCP2 interrupt

0 = Disables the CCP2 interrupt

PIC16(L)F722/3/4/6/7

6.0 I/O PORTS

There are as many as 35 general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

6.1 Alternate Pin Function

The Alternate Pin Function Control (APFCON) register is used to steer specific peripheral input and output functions between different pins. The APFCON register is shown in Register 6-1. For this device family, the following functions can be moved between different pins.

- \overline{SS} (Slave Select)
- CCP2

REGISTER 6-1: APFCON: ALTERNATE PIN FUNCTION CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	SSSEL	CCP2SEL
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'.

bit 1 **SSSEL:** \overline{SS} Input Pin Selection bit

0 = \overline{SS} function is on RA5/AN4/CPS7/ \overline{SS} /VCAP

1 = \overline{SS} function is on RA0/AN0/ \overline{SS} /VCAP

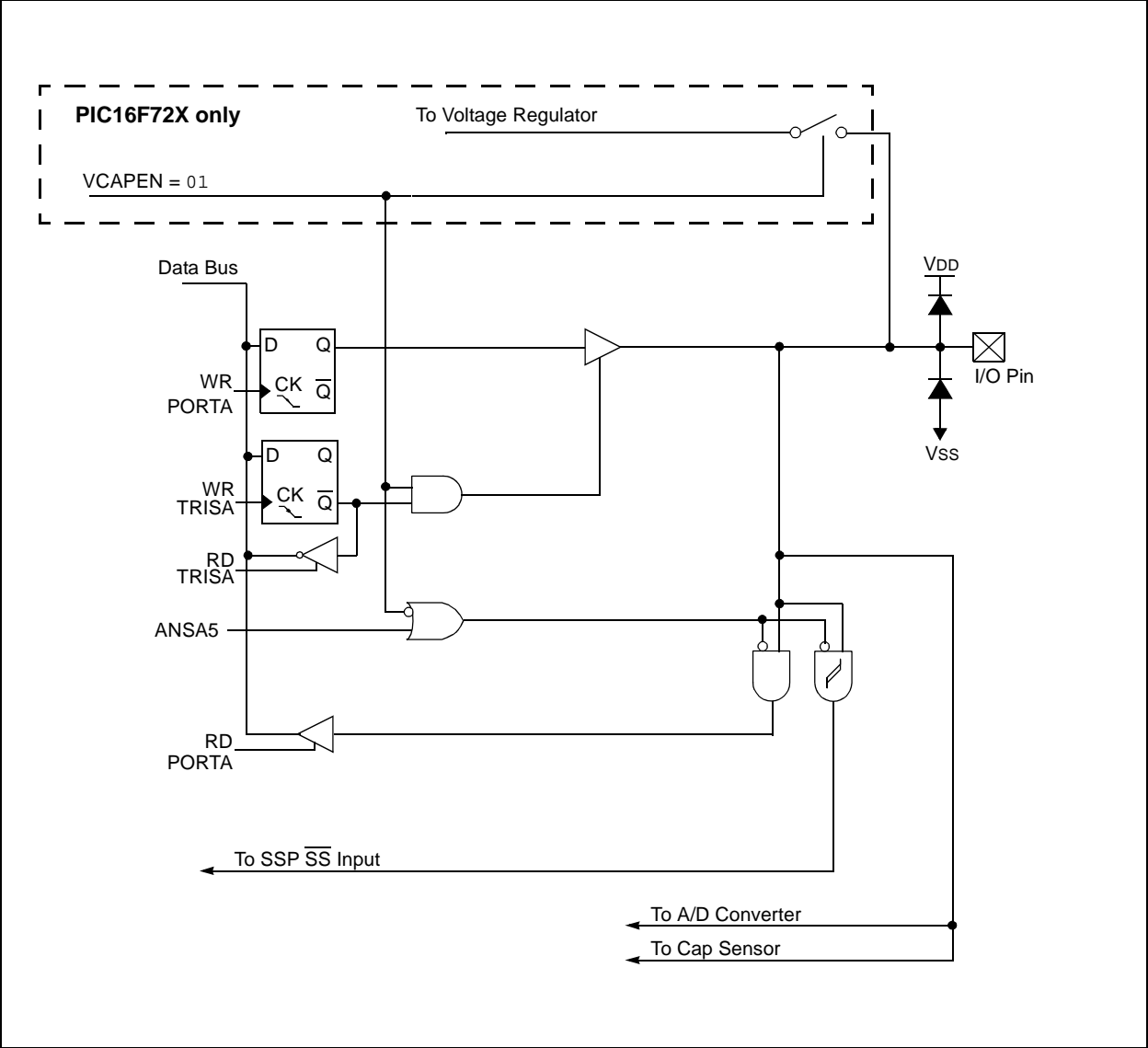
bit 0 **CCP2SEL:** CCP2 Input/Output Pin Selection bit

0 = CCP2 function is on RC1/T1OSI/CCP2

1 = CCP2 function is on RB3/CCP2

PIC16(L)F722/3/4/6/7

FIGURE 6-4: BLOCK DIAGRAM OF RA5



6.3 PORTB and TRISB Registers

PORTB is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISB (Register 6-6). Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 6-2 shows how to initialize PORTB.

Reading the PORTB register (Register 6-5) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch.

The TRISB register (Register 6-6) controls the PORTB pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISB register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'. Example 6-2 shows how to initialize PORTB.

EXAMPLE 6-2: INITIALIZING PORTB

```
BANKSEL PORTB      ;
CLRF  PORTB        ;Init PORTB
BANKSEL ANSELB
CLRF  ANSELB       ;Make RB<7:0> digital
BANKSEL TRISB      ;
MOVLW B'11110000' ;Set RB<7:4> as inputs
                     ;and RB<3:0> as outputs
MOVWF TRISB        ;
```

Note: The ANSELB register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

6.3.1 ANSELB REGISTER

The ANSELB register (Register 6-9) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELB bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELB bits has no effect on digital output functions. A pin with TRIS clear and ANSELB set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

6.3.2 WEAK PULL-UPS

Each of the PORTB pins has an individually configurable internal weak pull-up. Control bits WPUB<7:0> enable or disable each pull-up (see Register 6-7). Each weak pull-up is automatically turned off when the port pin is configured as an output. All pull-ups are disabled on a Power-on Reset by the RBPU bit of the OPTION register.

6.3.3 INTERRUPT-ON-CHANGE

All of the PORTB pins are individually configurable as an interrupt-on-change pin. Control bits IOCB<7:0> enable or disable the interrupt function for each pin. Refer to Register 6-8. The interrupt-on-change feature is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the present value is compared with the old value latched on the last read of PORTB to determine which bits have changed or mismatched the old value. The 'mismatch' outputs of the last read are OR'd together to set the PORTB Change Interrupt flag bit (RBIF) in the INTCON register.

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, clears the interrupt by:

- Any read or write of PORTB. This will end the mismatch condition.
- Clear the flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading or writing PORTB will end the mismatch condition and allow flag bit RBIF to be cleared. The latch holding the last read value is not affected by a MCLR nor Brown-out Reset. After these Resets, the RBIF flag will continue to be set if a mismatch is present.

Note: When a pin change occurs at the same time as a read operation on PORTB, the RBIF flag will always be set. If multiple PORTB pins are configured for the interrupt-on-change, the user may not be able to identify which pin changed state.

REGISTER 6-7: WPUB: WEAK PULL-UP PORTB REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **WPUB<7:0>**: Weak Pull-up Register bits

1 = Pull-up enabled

0 = Pull-up disabled

Note 1: Global RBPU bit of the OPTION register must be cleared for individual pull-ups to be enabled.

2: The weak pull-up device is automatically disabled if the pin is configured as an output.

REGISTER 6-8: IOCB: INTERRUPT-ON-CHANGE PORTB REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IOCB7	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **IOCB<7:0>**: Interrupt-on-Change PORTB Control bits

1 = Interrupt-on-change enabled

0 = Interrupt-on-change disabled

REGISTER 6-9: ANSELB: PORTB ANALOG SELECT REGISTER

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **ANSB<5:0>**: Analog Select between Analog or Digital Function on Pins RB<5:0>, respectively

0 = Digital I/O. Pin is assigned to port or Digital special function.

1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital Input buffer disabled.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 11-1: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBP}}\text{U}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **$\overline{\text{RBP}}\text{U}$** : PORTB Pull-up Enable bit
 1 = PORTB pull-ups are disabled
 0 = PORTB pull-ups are enabled by individual port latch values
- bit 6 **INTEDG**: Interrupt Edge Select bit
 1 = Interrupt on rising edge of INT pin
 0 = Interrupt on falling edge of INT pin
- bit 5 **T0CS**: TMR0 Clock Source Select bit
 1 = Transition on T0CKI pin or CPSOSC signal
 0 = Internal instruction cycle clock (Fosc/4)
- bit 4 **T0SE**: TMR0 Source Edge Select bit
 1 = Increment on high-to-low transition on T0CKI pin
 0 = Increment on low-to-high transition on T0CKI pin
- bit 3 **PSA**: Prescaler Assignment bit
 1 = Prescaler is assigned to the WDT
 0 = Prescaler is assigned to the Timer0 module
- bit 2-0 **PS<2:0>**: Prescaler Rate Select bits

BIT VALUE	TMR0 RATE	WDT RATE
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

TABLE 11-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CPSCON0	CPSON	—	—	—	CPSRNG1	CPSRNG0	CPSOUT	T0XCS	0--- 0000	0--- 0000
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
OPTION_REG	$\overline{\text{RBP}}\text{U}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111	1111 1111

Legend: — = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.

PIC16(L)F722/3/4/6/7

13.0 TIMER2 MODULE

The Timer2 module is an 8-bit timer with the following features:

- 8-bit timer register (TMR2)
- 8-bit period register (PR2)
- Interrupt on TMR2 match with PR2
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16)

See Figure 13-1 for a block diagram of Timer2.

13.1 Timer2 Operation

The clock input to the Timer2 module is the system instruction clock ($F_{osc}/4$). The clock is fed into the Timer2 prescaler, which has prescale options of 1:1, 1:4 or 1:16. The output of the prescaler is then used to increment the TMR2 register.

The values of TMR2 and PR2 are constantly compared to determine when they match. TMR2 will increment from 00h until it matches the value in PR2. When a match occurs, two things happen:

- TMR2 is reset to 00h on the next increment cycle.
- The Timer2 postscaler is incremented.

The match output of the Timer2/PR2 comparator is then fed into the Timer2 postscaler. The postscaler has postscale options of 1:1 to 1:16 inclusive. The output of the Timer2 postscaler is used to set the TMR2IF interrupt flag bit in the PIR1 register.

The TMR2 and PR2 registers are both fully readable and writable. On any Reset, the TMR2 register is set to 00h and the PR2 register is set to FFh.

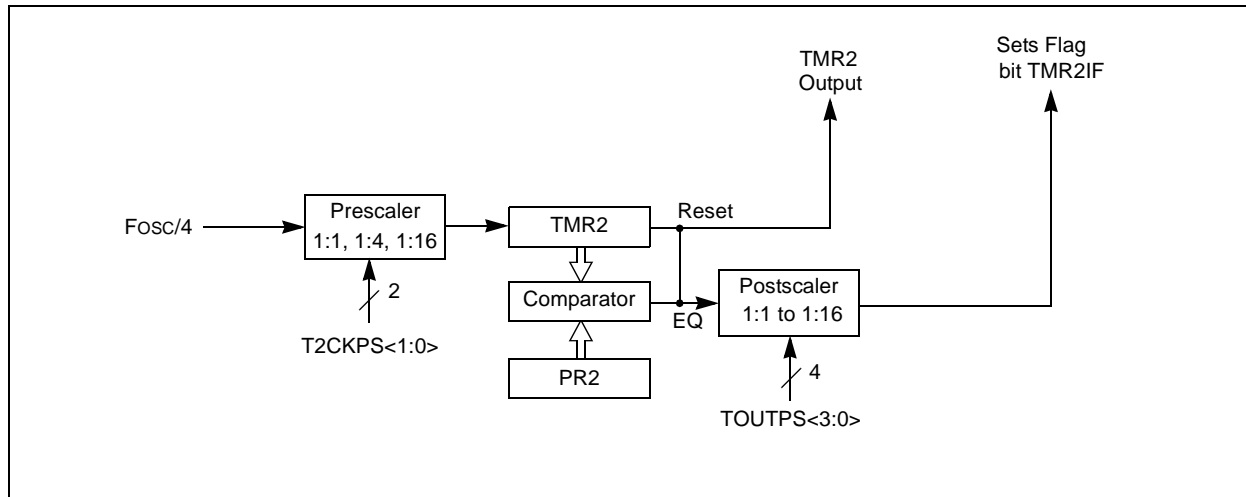
Timer2 is turned on by setting the TMR2ON bit in the T2CON register to a '1'. Timer2 is turned off by clearing the TMR2ON bit to a '0'.

The Timer2 prescaler is controlled by the T2CKPS bits in the T2CON register. The Timer2 postscaler is controlled by the TOUTPS bits in the T2CON register. The prescaler and postscaler counters are cleared when:

- A write to TMR2 occurs.
- A write to T2CON occurs.
- Any device Reset occurs (Power-on Reset, \overline{MCLR} Reset, Watchdog Timer Reset, or Brown-out Reset).

Note: TMR2 is not cleared when T2CON is written.

FIGURE 13-1: TIMER2 BLOCK DIAGRAM



15.3.2 PWM PERIOD

The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using the formula of Equation 15-1.

EQUATION 15-1: PWM PERIOD

$$PWM\ Period = [(PR2) + 1] \cdot 4 \cdot T_{OSC} \cdot (TMR2\ Prescale\ Value)$$

Note: $T_{OSC} = 1/F_{OSC}$

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCPx pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from CCPRxL into CCPRxH.

Note: The Timer2 postscaler (refer to **Section 13.1 “Timer2 Operation”**) is not used in the determination of the PWM frequency.

15.3.3 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to multiple registers: CCPRxL register and DCxB<1:0> bits of the CCPxCON register. The CCPRxL contains the eight MSbs and the DCxB<1:0> bits of the CCPxCON register contain the two LSbs. CCPRxL and DCxB<1:0> bits of the CCPxCON register can be written to at any time. The duty cycle value is not latched into CCPRxH until after the period completes (i.e., a match between PR2 and TMR2 registers occurs). While using the PWM, the CCPRxH register is read-only.

Equation 15-2 is used to calculate the PWM pulse width.

Equation 15-3 is used to calculate the PWM duty cycle ratio.

EQUATION 15-2: PULSE WIDTH

$$Pulse\ Width = (CCPRxL:CCPxCON<5:4>) \cdot T_{OSC} \cdot (TMR2\ Prescale\ Value)$$

Note: $T_{OSC} = 1/F_{OSC}$

EQUATION 15-3: DUTY CYCLE RATIO

$$Duty\ Cycle\ Ratio = \frac{(CCPRxL:CCPxCON<5:4>)}{4(PR2 + 1)}$$

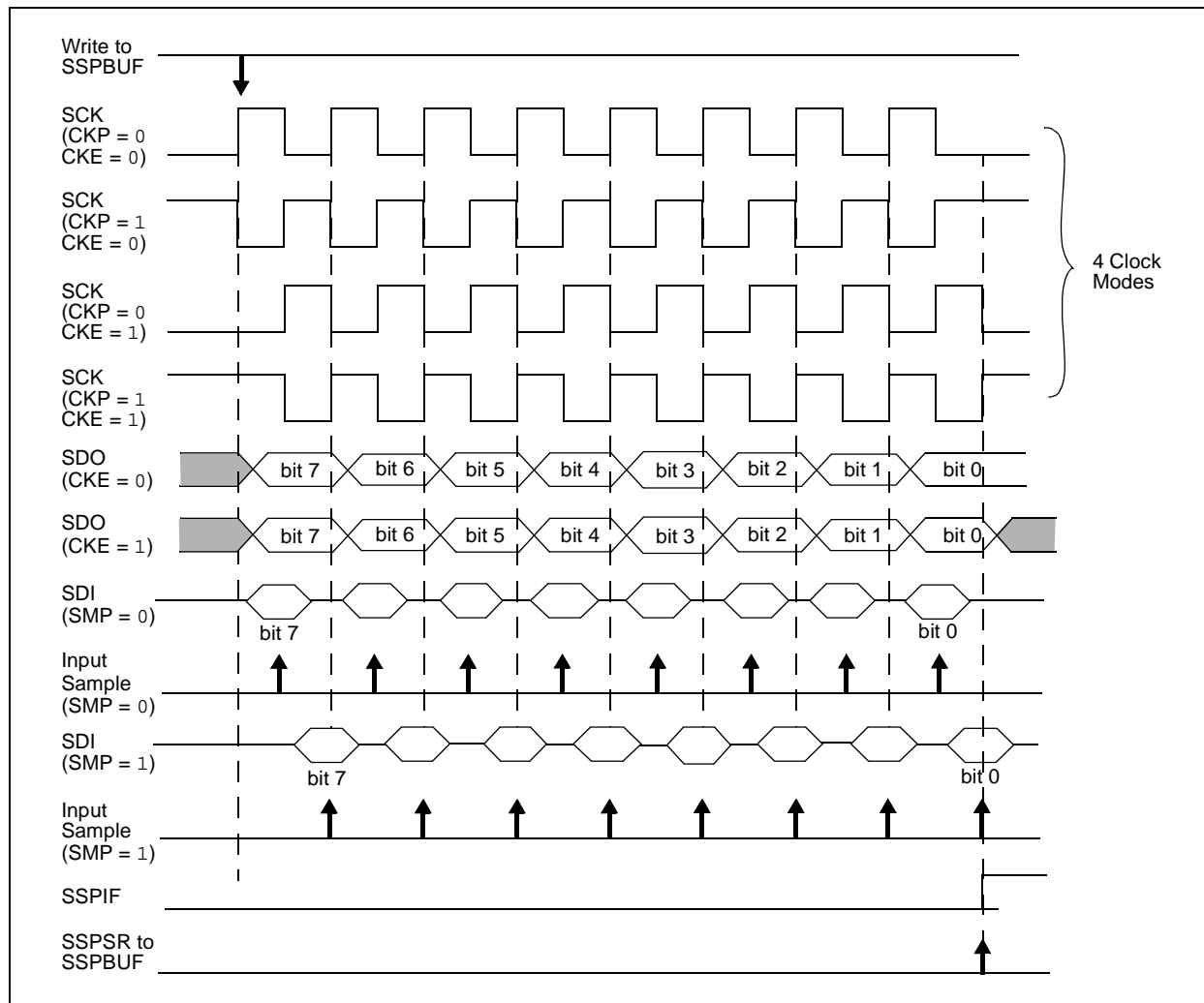
The CCPRxH register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (F_{OSC}), or two bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPRxH and 2-bit latch, then the CCPx pin is cleared (refer to Figure 15-3).

PIC16(L)F722/3/4/6/7

FIGURE 17-3: SPI MASTER MODE WAVEFORM



EXAMPLE 17-1: LOADING THE SSPBUF (SSPSR) REGISTER

```

BANKSEL    SSPSTAT    ;
LOOP      BTFSS      SSPSTAT, BF ;Has data been received(transmit complete)?
          GOTO        LOOP        ;No
BANKSEL    SSPBUF      ;
          MOVF        SSPBUF, W    ;WREG reg = contents of SSPBUF
          MOVWF       RXDATA       ;Save in user RAM, if data is meaningful
          MOVF        TXDATA, W    ;W reg = contents of TXDATA
          MOVWF       SSPBUF       ;New data to xmit
    
```

23.5 Thermal Considerations

Standard Operating Conditions (unless otherwise stated)					
Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$					
Param No.	Sym.	Characteristic	Typ.	Units	Conditions
TH01	θ_{JA}	Thermal Resistance Junction to Ambient	60	$^{\circ}\text{C/W}$	28-pin SPDIP package
			80	$^{\circ}\text{C/W}$	28-pin SOIC package
			90	$^{\circ}\text{C/W}$	28-pin SSOP package
			27.5	$^{\circ}\text{C/W}$	28-pin UQFN 4x4mm package
			27.5	$^{\circ}\text{C/W}$	28-pin QFN 6x6mm package
			47.2	$^{\circ}\text{C/W}$	40-pin PDIP package
			46	$^{\circ}\text{C/W}$	44-pin TQFP package
			24.4	$^{\circ}\text{C/W}$	44-pin QFN 8x8mm package
TH02	θ_{JC}	Thermal Resistance Junction to Case	31.4	$^{\circ}\text{C/W}$	28-pin SPDIP package
			24	$^{\circ}\text{C/W}$	28-pin SOIC package
			24	$^{\circ}\text{C/W}$	28-pin SSOP package
			24	$^{\circ}\text{C/W}$	28-pin UQFN 4x4mm package
			24	$^{\circ}\text{C/W}$	28-pin QFN 6x6mm package
			24.7	$^{\circ}\text{C/W}$	40-pin PDIP package
			14.5	$^{\circ}\text{C/W}$	44-pin TQFP package
			20	$^{\circ}\text{C/W}$	44-pin QFN 8x8mm package
TH03	T_{JMAX}	Maximum Junction Temperature	150	$^{\circ}\text{C}$	
TH04	PD	Power Dissipation	—	W	$PD = P_{INTERNAL} + P_{I/O}$
TH05	$P_{INTERNAL}$	Internal Power Dissipation	—	W	$P_{INTERNAL} = I_{DD} \times V_{DD}^{(1)}$
TH06	$P_{I/O}$	I/O Power Dissipation	—	W	$P_{I/O} = \sum (I_{OL} \times V_{OL}) + \sum (I_{OH} \times (V_{DD} - V_{OH}))$
TH07	P_{DER}	Derated Power	—	W	$P_{DER} = P_{DMAX} (T_J - T_A) / \theta_{JA}^{(2)}$

Note 1: I_{DD} is current to run the chip alone without driving any load on the output pins.

2: T_A = Ambient Temperature

3: T_J = Junction Temperature

PIC16(L)F722/3/4/6/7

FIGURE 24-25: PIC16F722/3/4/6/7 TYPICAL I_{DD} vs. F_{OSC} OVER V_{DD} , INTOSC MODE, $V_{CAP} = 0.1 \mu F$

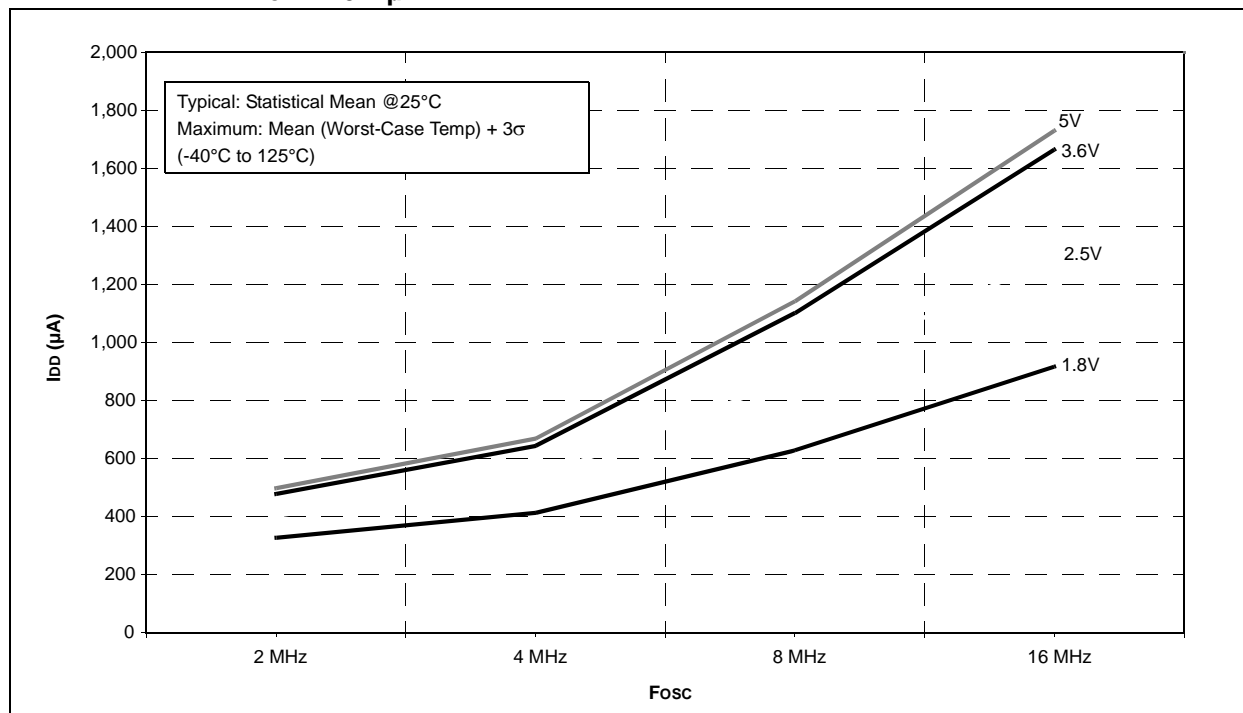
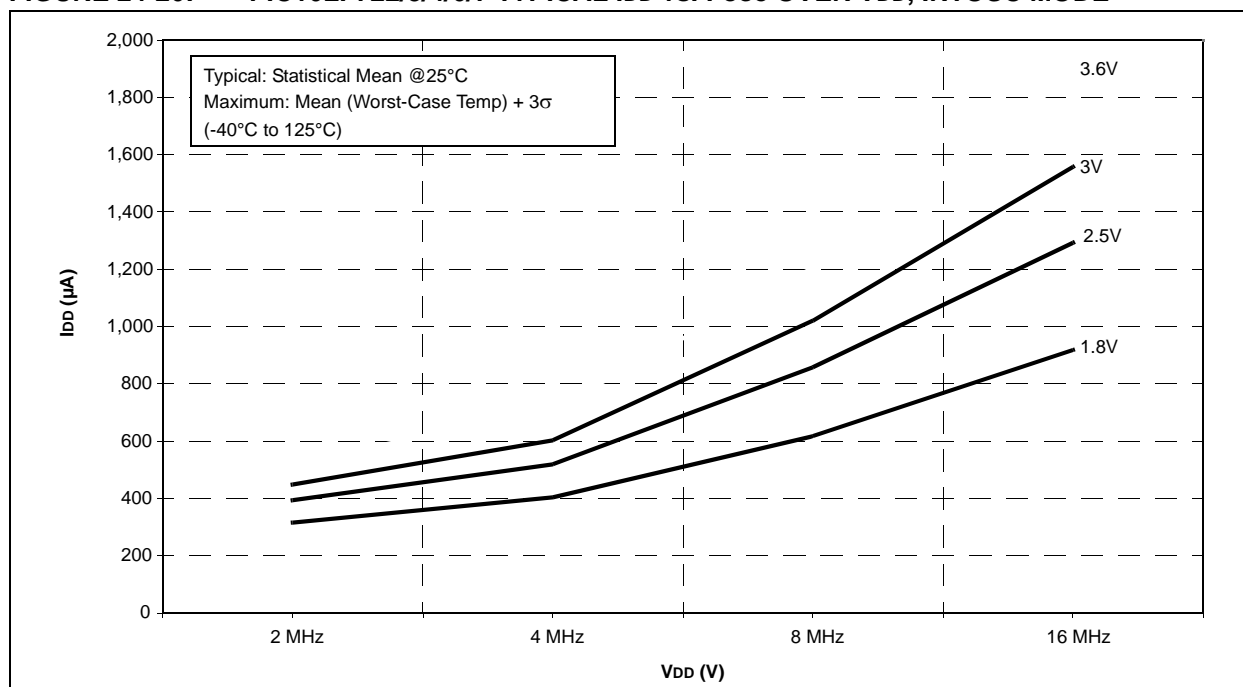


FIGURE 24-26: PIC16LF722/3/4/6/7 TYPICAL I_{DD} vs. F_{OSC} OVER V_{DD} , INTOSC MODE



PIC16(L)F722/3/4/6/7

FIGURE 24-49: TTL INPUT THRESHOLD V_{IN} vs. V_{DD} OVER TEMPERATURE

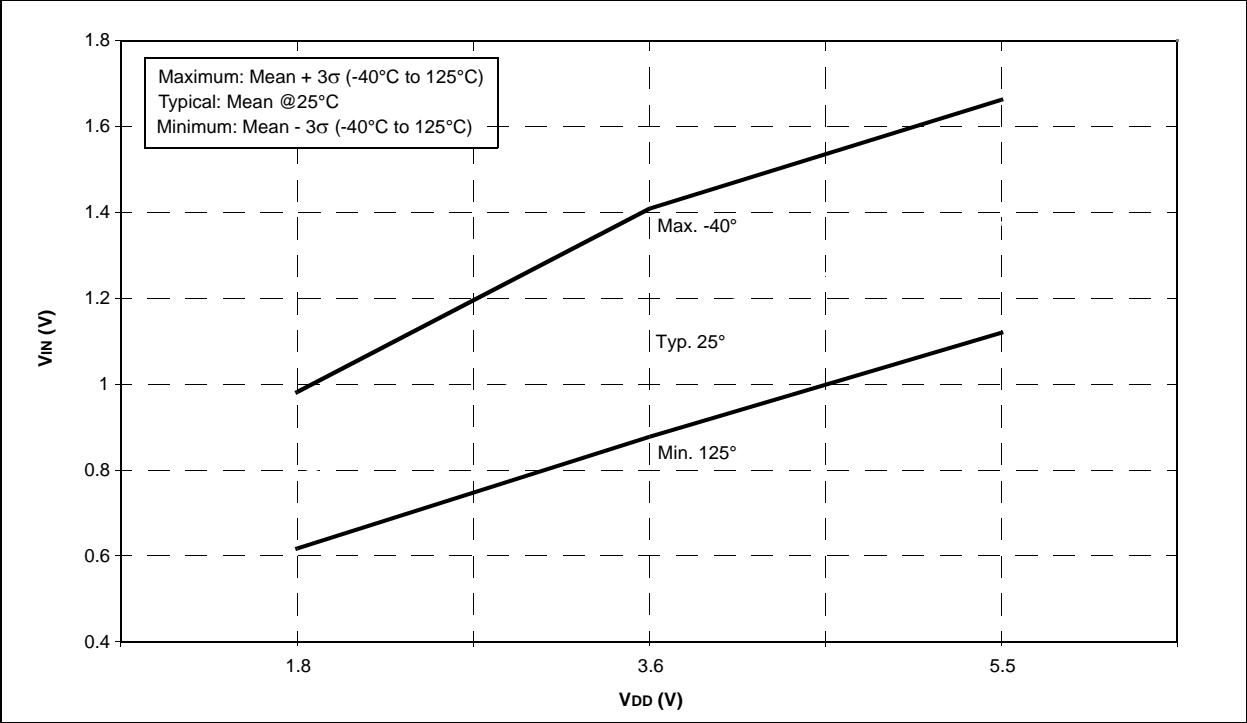


FIGURE 24-50: SCHMITT TRIGGER INPUT THRESHOLD V_{IN} vs. V_{DD} OVER TEMPERATURE

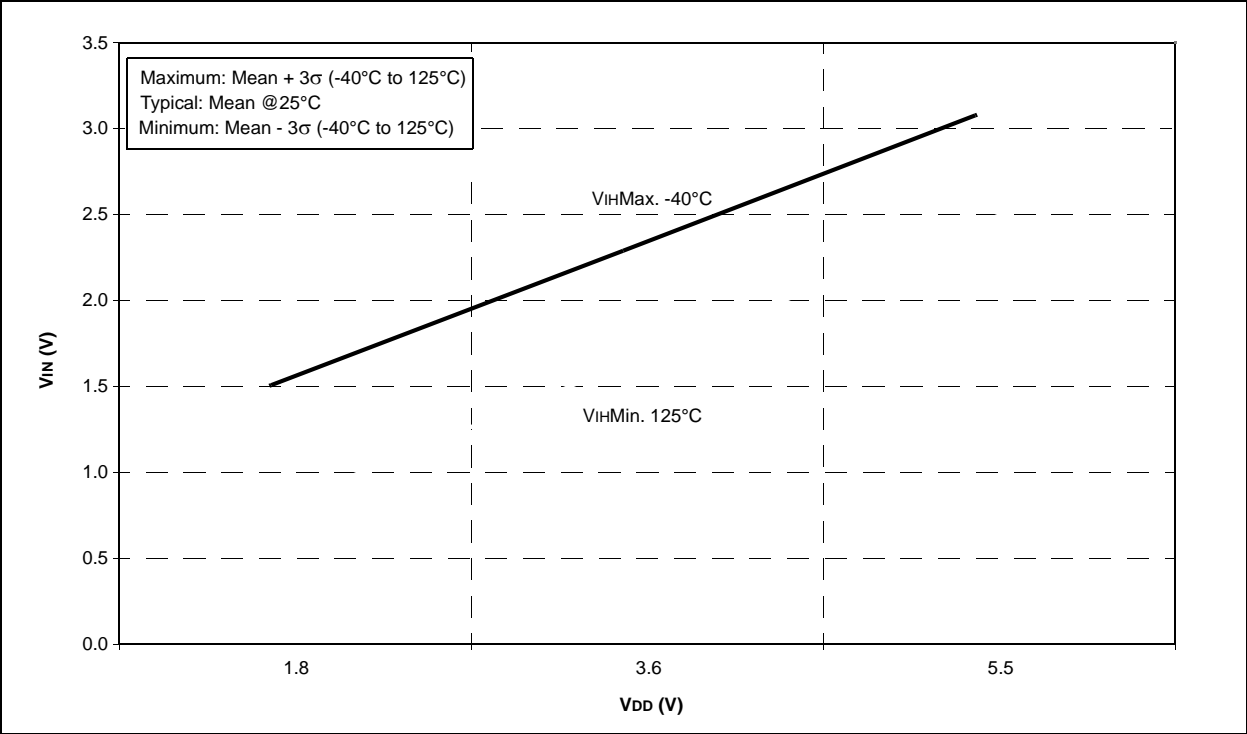


FIGURE 24-59: PIC16F722/3/4/6/7 WDT TIME-OUT PERIOD

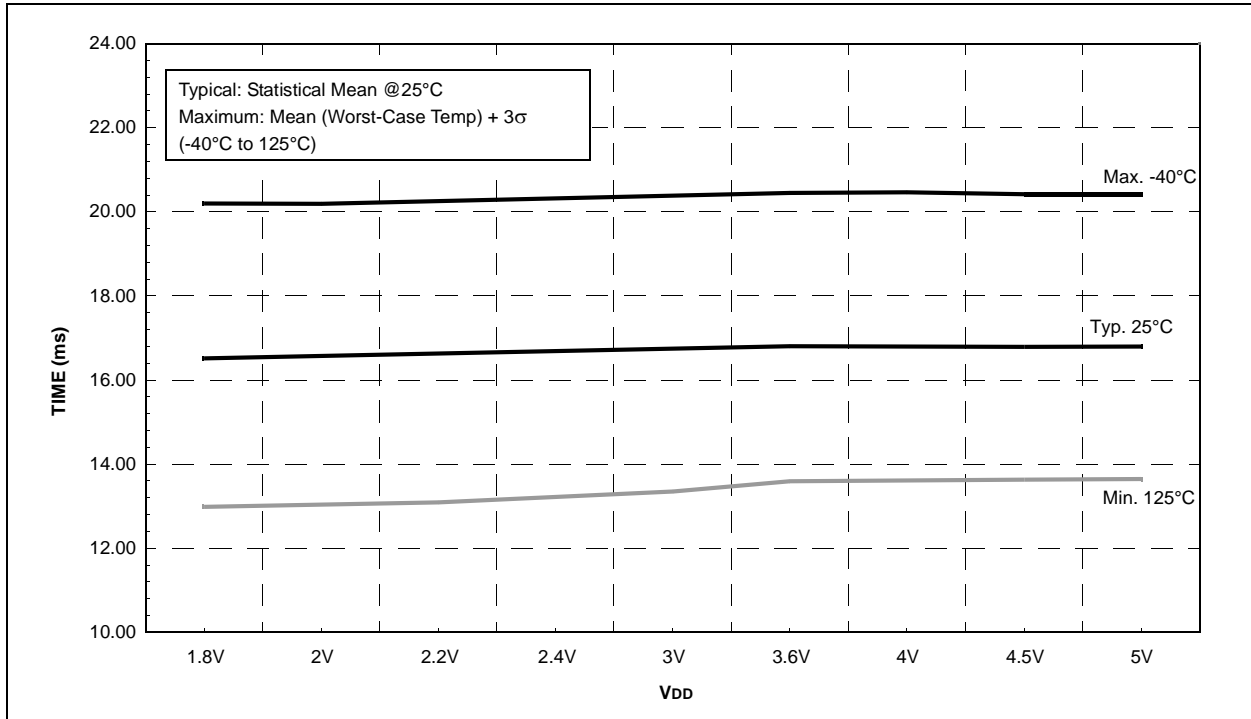
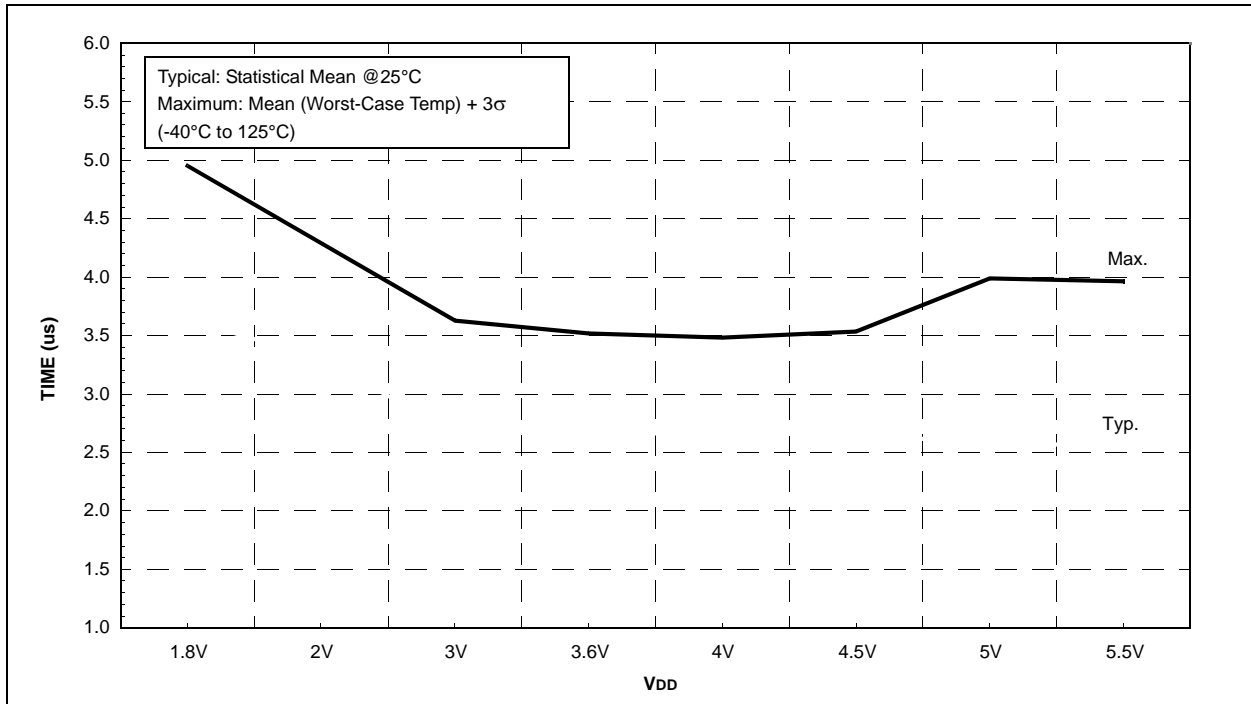
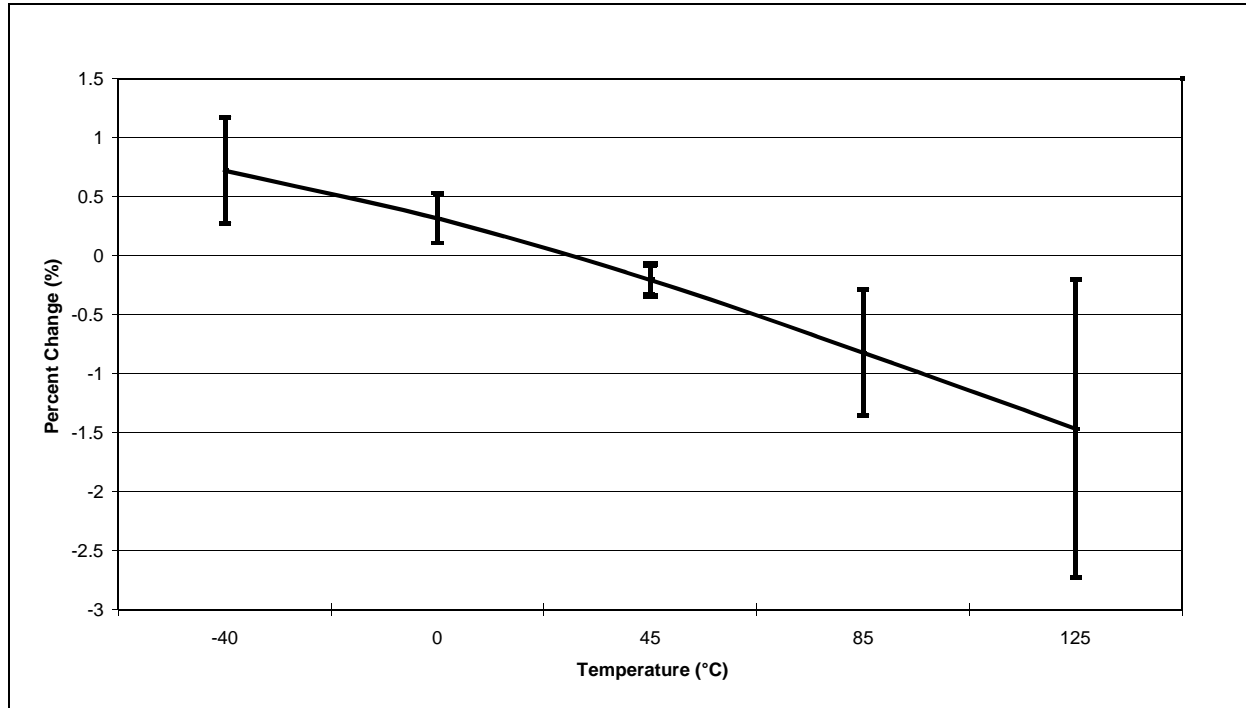


FIGURE 24-60: PIC16F722/3/4/6/7 HFINTOSC WAKE-UP FROM SLEEP START-UP TIME



PIC16(L)F722/3/4/6/7

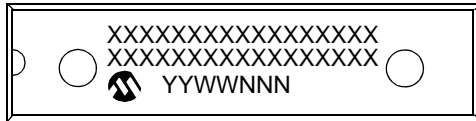
FIGURE 24-69: TYPICAL FVR CHANGE VS. TEMPERATURE NORMALIZED AT 25°C



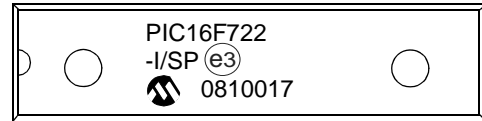
25.0 PACKAGING INFORMATION

25.1 Package Marking Information

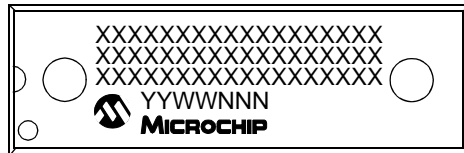
28-Lead SPDIP



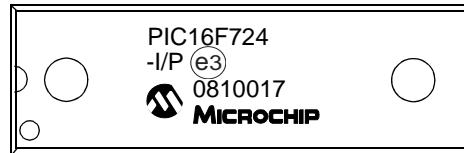
Example



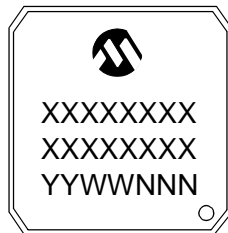
40-Lead PDIP



Example



28-Lead QFN/UQFN



Example



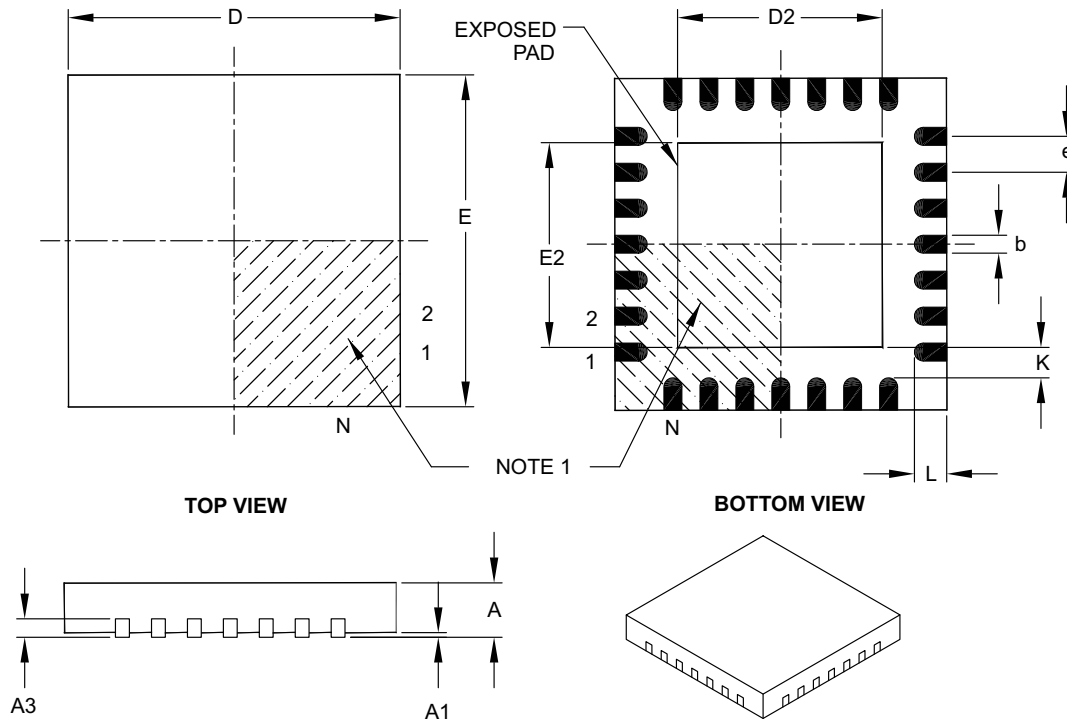
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC® designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

- * Standard PICmicro® device marking consists of Microchip part number, year code, week code and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	3.65	3.70	4.20
Contact Width	b	0.23	0.30	0.35
Contact Length	L	0.50	0.55	0.70
Contact-to-Exposed Pad	K	0.20	—	—

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B