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Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I ² C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 14KB (8K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 368 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 11x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 28-DIP (0.300", 7.62mm) |
| Supplier Device Package | 28-SPDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16lf726-i-sp |

The diagram illustrates the internal architecture and external connections of the PIC16F722/723/726 microcontroller. Key components include:

- Configuration:** A block at the top left for setting device-specific parameters.
- Program Memory:** Flash Program Memory connected to a Program Counter and an 8-Level Stack (13-bit).
- Instruction Path:** Program Bus (14) feeds into the Instruction Register, which then feeds into the Instruction Decode and Control block.
- Timing and Power:** Includes an Internal Oscillator Block, Timing Generation, and a Power-up Timer/Oscillator Start-up Timer/Power-on Reset/Watchdog Timer/Brown-out Reset/LDO(1) Regulator.
- Arithmetic and Logic:** Features an ALU, W Register, and a MUX (Multiplexer).
- Control and Status:** Includes a STATUS Register, FSR Register, and an Addr MUX (Address Multiplexer).
- Ports:** PORTA, PORTB, PORTC, and PORTE, each with multiple pins (RA0-RA7, RB0-RB7, RC0-RC7, RE3).
- Timers and Counters:** Timer0, Timer1 (32 kHz Oscillator), Timer2, CCP1, and CCP2.
- Communication:** AUSART (Asynchronous Universal Serial Transceiver) and a Synchronous Serial Port.
- Analog and Sensing:** Analog-To-Digital Converter (ADC) and a Capacitive Sensing Module.
- External Connections:** OSC1/CLKIN, OSC2/CLKOUT, VREF, MCLR, VDD, VSS, TX/CK, RX/DT, SDO, SDA, SCL, SS.

3.4.2 WDT CONTROL

The WDTE bit is located in the Configuration Word Register 1. When set, the WDT runs continuously.

The PSA and PS<2:0> bits of the OPTION register control the WDT period. See **Section 11.0 “Timer0 Module”** for more information.

FIGURE 3-1: WATCHDOG TIMER BLOCK DIAGRAM

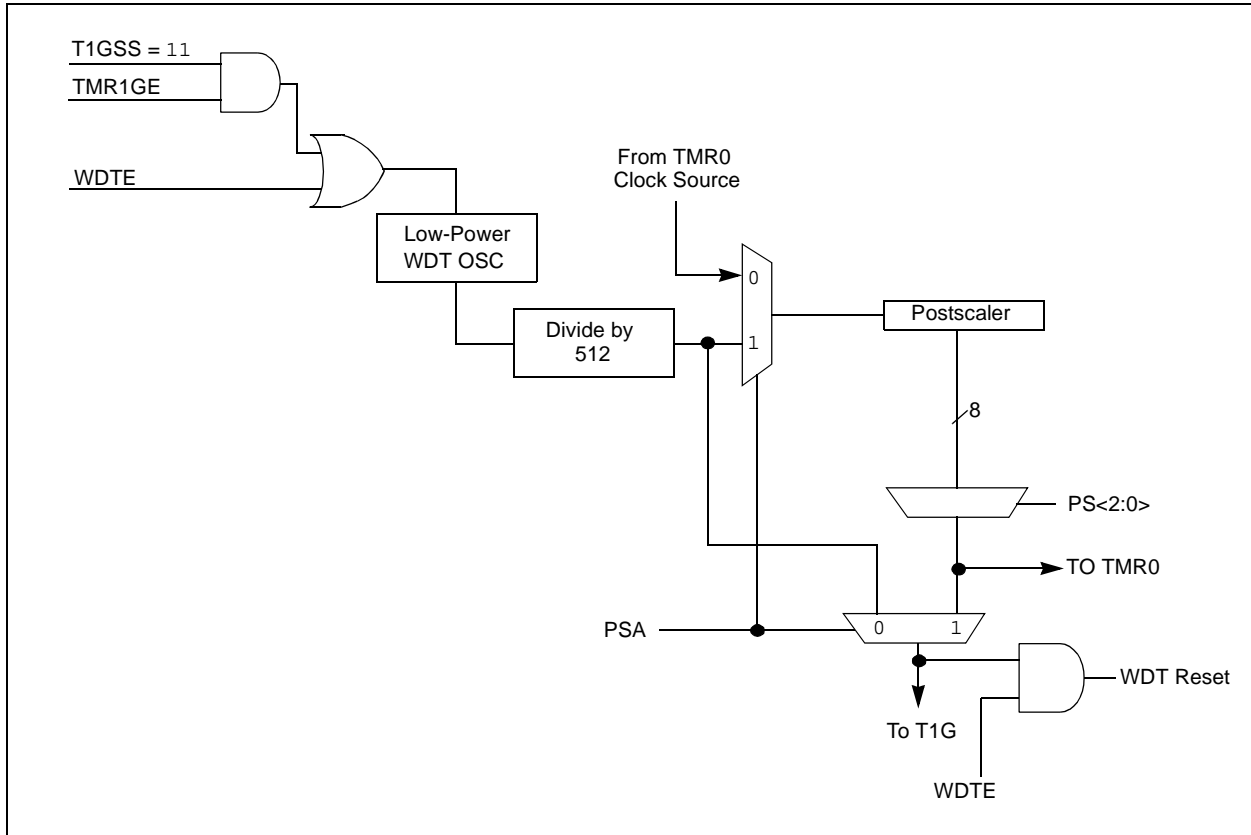


TABLE 3-1: WDT STATUS

| Conditions | WDT |
|--|------------------------------|
| WDTE = 0 | Cleared |
| CLRWDT Command | |
| Exit Sleep + System Clock = T1OSC, EXTRC, INTOSC, EXTCLK | |
| Exit Sleep + System Clock = XT, HS, LP | Cleared until the end of OST |

6.6.1 RE0/AN5⁽¹⁾

Figure 6-22 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC

Note 1: RE0/AN5 is available on PIC16F724/LF724 and PIC16F727/LF727 only.

6.6.2 RE1/AN6⁽¹⁾

Figure 6-22 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC

Note 1: RE0/AN5 is available on PIC16F724/LF724 and PIC16F727/LF727 only.

6.6.3 RE2/AN7⁽¹⁾

Figure 6-22 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC

Note 1: RE0/AN5 is available on PIC16F724/LF724 and PIC16F727/LF727 only.

6.6.4 RE3/MCLR/VPP

Figure 6-23 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose input
- as Master Clear Reset with weak pull-up
- a programming voltage reference input

9.2.7 ADC REGISTER DEFINITIONS

The following registers are used to control the operation of the ADC.

REGISTER 9-1: ADCON0: A/D CONTROL REGISTER 0

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-----|-------|-------|-------|-------|---------|-------|
| — | — | CHS3 | CHS2 | CHS1 | CHS0 | GO/DONE | ADON |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS<3:0>:** Analog Channel Select bits

0000 = AN0
 0001 = AN1
 0010 = AN2
 0011 = AN3
 0100 = AN4
 0101 = AN5
 0110 = AN6
 0111 = AN7
 1000 = AN8
 1001 = AN9
 1010 = AN10
 1011 = AN11
 1100 = AN12
 1101 = AN13
 1110 = Reserved
 1111 = Fixed Voltage Reference (FVREF)

bit 1 **GO/DONE:** A/D Conversion Status bit

1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
 This bit is automatically cleared by hardware when the A/D conversion has completed.
 0 = A/D conversion completed/not in progress

bit 0 **ADON:** ADC Enable bit

1 = ADC is enabled
 0 = ADC is disabled and consumes no operating current

12.1 Timer1 Operation

The Timer1 module is a 16-bit incrementing counter which is accessed through the TMR1H:TMR1L register pair. Writes to TMR1H or TMR1L directly update the counter.

When used with an internal clock source, the module is a timer and increments on every instruction cycle. When used with an external clock source, the module can be used as either a timer or counter and increments on every selected edge of the external source.

Timer1 is enabled by configuring the TMR1ON and TMR1GE bits in the T1CON and T1GCON registers, respectively. Table 12-1 displays the Timer1 enable selections.

TABLE 12-1: TIMER1 ENABLE SELECTIONS

| TMR1ON | TMR1GE | Timer1 Operation |
|--------|--------|------------------|
| 0 | 0 | Off |
| 0 | 1 | Off |
| 1 | 0 | Always On |
| 1 | 1 | Count Enabled |

12.2 Clock Source Selection

The TMR1CS<1:0> and T1OSCEN bits of the T1CON register are used to select the clock source for Timer1. Table 12-2 displays the clock source selections.

12.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected, the TMR1H:TMR1L register pair will increment on multiples of FOSC as determined by the Timer1 prescaler.

12.2.2 EXTERNAL CLOCK SOURCE

When the external clock source is selected, the Timer1 module may work as a timer or a counter.

When enabled to count, Timer1 is incremented on the rising edge of the external clock input T1CKI or the capacitive sensing oscillator signal. Either of these external clock sources can be synchronized to the microcontroller system clock or they can run asynchronously.

When used as a timer with a clock oscillator, an external 32.768 kHz crystal can be used in conjunction with the dedicated internal oscillator circuit.

Note: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge after any one or more of the following conditions:

- Timer1 enabled after POR reset
- Write to TMR1H or TMR1L
- Timer1 is disabled
- Timer1 is disabled (TMR1ON = 0) when T1CKI is high then Timer1 is enabled (TMR1ON = 1) when T1CKI is low.

TABLE 12-2: CLOCK SOURCE SELECTIONS

| TMR1CS1 | TMR1CS0 | T1OSCEN | Clock Source |
|---------|---------|---------|--|
| 0 | 1 | x | System Clock (FOSC) |
| 0 | 0 | x | Instruction Clock (FOSC/4) |
| 1 | 1 | x | Capacitive Sensing Oscillator |
| 1 | 0 | 0 | External Clocking on T1CKI Pin |
| 1 | 0 | 1 | Oscillator Circuit on T1OSI/T1OSO Pins |

12.6 Timer1 Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using Timer1 Gate circuitry. This is also referred to as Timer1 Gate Count Enable.

Timer1 Gate can also be driven by multiple selectable sources.

12.6.1 TIMER1 GATE COUNT ENABLE

The Timer1 Gate is enabled by setting the TMR1GE bit of the T1GCON register. The polarity of the Timer1 Gate is configured using the T1GPOL bit of the T1GCON register.

When Timer1 Gate (T1G) input is active, Timer1 will increment on the rising edge of the Timer1 clock source. When Timer1 Gate input is inactive, no incrementing will occur and Timer1 will hold the current count. See Figure 12-3 for timing details.

TABLE 12-3: TIMER1 GATE ENABLE SELECTIONS

| T1CLK | T1GPOL | T1G | Timer1 Operation |
|-------|--------|-----|------------------|
| ↑ | 0 | 0 | Counts |
| ↑ | 0 | 1 | Holds Count |
| ↑ | 1 | 0 | Holds Count |
| ↑ | 1 | 1 | Counts |

12.6.2 TIMER1 GATE SOURCE SELECTION

The Timer1 Gate source can be selected from one of four different sources. Source selection is controlled by the T1GSS bits of the T1GCON register. The polarity for each available source is also selectable. Polarity selection is controlled by the T1GPOL bit of the T1GCON register.

TABLE 12-4: TIMER1 GATE SOURCES

| T1GSS | Timer1 Gate Source |
|-------|---|
| 00 | Timer1 Gate Pin |
| 01 | Overflow of Timer0 (TMR0 increments from FFh to 00h) |
| 10 | Timer2 match PR2 (TMR2 increments to match PR2) |
| 11 | Count Enabled by WDT Overflow (Watchdog Time-out interval expired) |

12.6.2.1 T1G Pin Gate Operation

The T1G pin is one source for Timer1 Gate Control. It can be used to supply an external source to the Timer1 Gate circuitry.

12.6.2.2 Timer0 Overflow Gate Operation

When Timer0 increments from FFh to 00h, a low-to-high pulse will automatically be generated and internally supplied to the Timer1 Gate circuitry.

12.6.2.3 Timer2 Match Gate Operation

The TMR2 register will increment until it matches the value in the PR2 register. On the very next increment cycle, TMR2 will be reset to 00h. When this Reset occurs, a low-to-high pulse will automatically be generated and internally supplied to the Timer1 Gate circuitry.

12.6.2.4 Watchdog Overflow Gate Operation

The Watchdog Timer oscillator, prescaler and counter will be automatically turned on when TMR1GE = 1 and T1GSS selects the WDT as a gate source for Timer1 (T1GSS = 11). TMR1ON does not factor into the oscillator, prescaler and counter enable. See Table 12-5.

The PSA and PS bits of the OPTION register still control what time-out interval is selected. Changing the prescaler during operation may result in a spurious capture.

Enabling the Watchdog Timer oscillator does not automatically enable a Watchdog Reset or Wake-up from Sleep upon counter overflow.

Note: When using the WDT as a gate source for Timer1, operations that clear the Watchdog Timer (CLRWD, SLEEP instructions) will affect the time interval being measured for capacitive sensing. This includes waking from Sleep. All other interrupts that might wake the device from Sleep should be disabled to prevent them from disturbing the measurement period.

As the gate signal coming from the WDT counter will generate different pulse widths depending on if the WDT is enabled, when the CLRWD instruction is executed, and so on, Toggle mode must be used. A specific sequence is required to put the device into the correct state to capture the next WDT counter interval.

12.11 Timer1 Control Register

The Timer1 Control register (T1CON), shown in Register 12-1, is used to control Timer1 and select the various features of the Timer1 module.

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 |
|---------|---------|---------|---------|---------|--------|-----|--------|
| TMR1CS1 | TMR1CS0 | T1CKPS1 | T1CKPS0 | T1OSCEN | T1SYNC | — | TMR1ON |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6

TMR1CS<1:0>: Timer1 Clock Source Select bits

11 = Timer1 clock source is Capacitive Sensing Oscillator (CAPOSC)

10 = Timer1 clock source is pin or oscillator:

If T1OSCEN = 0:

External clock from T1CKI pin (on the rising edge)

If T1OSCEN = 1:

Crystal oscillator on T1OSI/T1OSO pins

01 = Timer1 clock source is system clock (Fosc)

00 = Timer1 clock source is instruction clock (Fosc/4)

bit 5-4

T1CKPS<1:0>: Timer1 Input Clock Prescale Select bits

11 = 1:8 Prescale value

10 = 1:4 Prescale value

01 = 1:2 Prescale value

00 = 1:1 Prescale value

bit 3

T1OSCEN: LP Oscillator Enable Control bit

1 = Dedicated Timer1 oscillator circuit enabled

0 = Dedicated Timer1 oscillator circuit disabled

bit 2

T1SYNC: Timer1 External Clock Input Synchronization Control bit

TMR1CS<1:0> = 1x

1 = Do not synchronize external clock input

0 = Synchronize external clock input with system clock (Fosc)

TMR1CS<1:0> = 0x

This bit is ignored. Timer1 uses the internal clock when TMR1CS<1:0> = 1x.

bit 1

Unimplemented: Read as '0'

bit 0

TMR1ON: Timer1 On bit

1 = Enables Timer1

0 = Stops Timer1

Clears Timer1 Gate flip-flop

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15.3.4 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is ten bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 15-4.

EQUATION 15-4: PWM RESOLUTION

$$Resolution = \frac{\log[4(PR2 + 1)]}{\log(2)} \text{ bits}$$

Note: If the pulse-width value is greater than the period, the assigned PWM pin(s) will remain unchanged.

TABLE 15-5: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 20 MHz)

| PWM Frequency | 1.22 kHz | 4.88 kHz | 19.53 kHz | 78.12 kHz | 156.3 kHz | 208.3 kHz |
|---------------------------|----------|----------|-----------|-----------|-----------|-----------|
| Timer Prescale (1, 4, 16) | 16 | 4 | 1 | 1 | 1 | 1 |
| PR2 Value | 0xFF | 0xFF | 0xFF | 0x3F | 0x1F | 0x17 |
| Maximum Resolution (bits) | 10 | 10 | 10 | 8 | 7 | 6.6 |

TABLE 15-6: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 8 MHz)

| PWM Frequency | 1.22 kHz | 4.90 kHz | 19.61 kHz | 76.92 kHz | 153.85 kHz | 200.0 kHz |
|---------------------------|----------|----------|-----------|-----------|------------|-----------|
| Timer Prescale (1, 4, 16) | 16 | 4 | 1 | 1 | 1 | 1 |
| PR2 Value | 0x65 | 0x65 | 0x65 | 0x19 | 0x0C | 0x09 |
| Maximum Resolution (bits) | 8 | 8 | 8 | 6 | 5 | 5 |

15.3.5 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCPx pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

15.3.6 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency (Fosc). Any changes in the system clock frequency will result in changes to the PWM frequency. Refer to **Section 7.0 “Oscillator Module”** for additional details.

15.3.7 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

15.3.8 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Disable the PWM pin (CCPx) output driver(s) by setting the associated TRIS bit(s).
2. Load the PR2 register with the PWM period value.
3. Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.

4. Load the CCPRxL register and the DCxBx bits of the CCPxCON register, with the PWM duty cycle value.
5. Configure and start Timer2:
 - Clear the TMR2IF interrupt flag bit of the PIR1 register. See Note below.
 - Configure the T2CKPS bits of the T2CON register with the Timer2 prescale value.
 - Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output pin:
 - Wait until Timer2 overflows, TMR2IF bit of the PIR1 register is set. See Note below.
 - Enable the PWM pin (CCPx) output driver(s) by clearing the associated TRIS bit(s).

Note: In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

16.1 AUSART Asynchronous Mode

The AUSART transmits and receives data using the standard non-return-to-zero (NRZ) format. NRZ is implemented with two levels: a VOH Mark state which represents a '1' data bit, and a VOL Space state which represents a '0' data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port idles in the Mark state. Each character transmission consists of one Start bit followed by eight or nine data bits and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is 8 bits. Each transmitted bit persists for a period of 1/(Baud Rate). An on-chip dedicated 8-bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. Refer to Table 16-5 for examples of baud rate Configurations.

The AUSART transmits and receives the LSb first. The AUSART's transmitter and receiver are functionally independent, but share the same data format and baud rate. Parity is not supported by the hardware, but can be implemented in software and stored as the ninth data bit.

16.1.1 AUSART ASYNCHRONOUS TRANSMITTER

The AUSART transmitter block diagram is shown in Figure 16-1. The heart of the transmitter is the serial Transmit Shift Register (TSR), which is not directly accessible by software. The TSR obtains its data from the transmit buffer, which is the TXREG register.

16.1.1.1 Enabling the Transmitter

The AUSART transmitter is enabled for asynchronous operations by configuring the following three control bits:

- TXEN = 1
- SYNC = 0
- SPEN = 1

All other AUSART control bits are assumed to be in their default state.

Setting the TXEN bit of the TXSTA register enables the transmitter circuitry of the AUSART. Clearing the SYNC bit of the TXSTA register configures the AUSART for asynchronous operation. Setting the SPEN bit of the RCSTA register enables the AUSART and automatically configures the TX/CK I/O pin as an output.

Note 1: When the SPEN bit is set the RX/DT I/O pin is automatically configured as an input, regardless of the state of the corresponding TRIS bit and whether or not the AUSART receiver is enabled. The RX/DT pin data can be read via a normal PORT read but PORT latch data output is precluded.

- 2:** The TXIF transmitter interrupt flag is set when the TXEN enable bit is set.

16.1.1.2 Transmitting Data

A transmission is initiated by writing a character to the TXREG register. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the TXREG until the Stop bit of the previous character has been transmitted. The pending character in the TXREG is then transferred to the TSR in one Tcy immediately following the Stop bit transmission. The transmission of the Start bit, data bits and Stop bit sequence commences immediately following the transfer of the data to the TSR from the TXREG.

16.1.1.3 Transmit Interrupt Flag

The TXIF interrupt flag bit of the PIR1 register is set whenever the AUSART transmitter is enabled and no character is being held for transmission in the TXREG. In other words, the TXIF bit is only clear when the TSR is busy with a character and a new character has been queued for transmission in the TXREG. The TXIF flag bit is not cleared immediately upon writing TXREG. TXIF becomes valid in the second instruction cycle following the write execution. Polling TXIF immediately following the TXREG write will return invalid results. The TXIF bit is read-only, it cannot be set or cleared by software.

The TXIF interrupt can be enabled by setting the TXIE interrupt enable bit of the PIE1 register. However, the TXIF flag bit will be set whenever the TXREG is empty, regardless of the state of TXIE enable bit.

To use interrupts when transmitting data, set the TXIE bit only when there is more data to send. Clear the TXIE interrupt enable bit upon writing the last character of the transmission to the TXREG.

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FIGURE 16-4: ASYNCHRONOUS TRANSMISSION (BACK-TO-BACK)

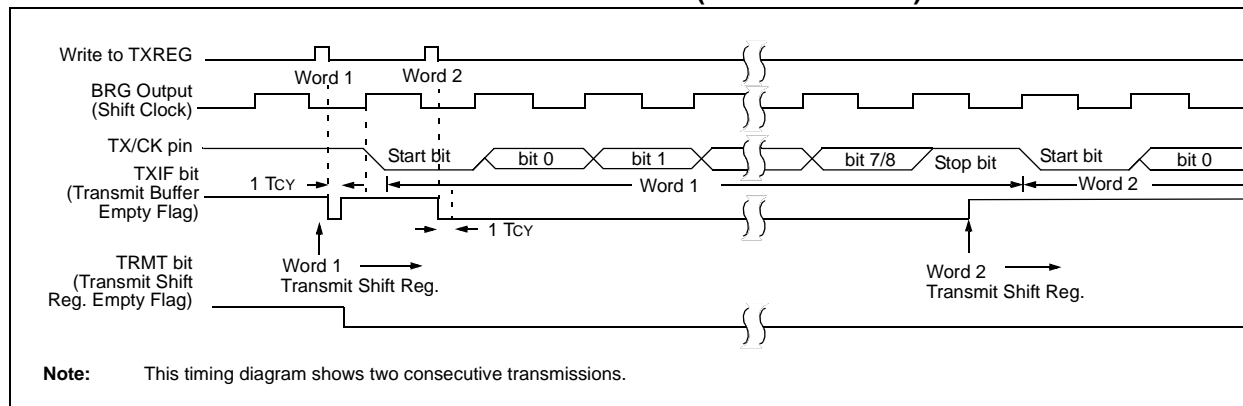


TABLE 16-1: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|--------|-------------------------------|--------|--------|--------|--------|--------|--------|--------|-------------------|---------------------------|
| INTCON | GIE | PEIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 0000 000x | 0000 000x |
| PIE1 | TMR1GIE | ADIE | RCIE | TXIE | SSPIE | CCP1IE | TMR2IE | TMR1IE | 0000 0000 | 0000 0000 |
| PIR1 | TMR1GIF | ADIF | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF | 0000 0000 | 0000 0000 |
| RCSTA | SPEN | RX9 | SREN | CREN | ADDEN | FERR | OERR | RX9D | 0000 000x | 0000 000x |
| SPBRG | BRG7 | BRG6 | BRG5 | BRG4 | BRG3 | BRG2 | BRG1 | BRG0 | 0000 0000 | 0000 0000 |
| TRISC | TRISC7 | TRISC6 | TRISC5 | TRISC4 | TRISC3 | TRISC2 | TRISC1 | TRISC0 | 1111 1111 | 1111 1111 |
| TXREG | AUSART Transmit Data Register | | | | | | | | 0000 0000 | 0000 0000 |
| TXSTA | CSRC | TX9 | TXEN | SYNC | — | BRGH | TRMT | TX9D | 0000 -010 | 0000 -010 |

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Asynchronous Transmission.

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TABLE 16-5: BAUD RATES FOR ASYNCHRONOUS MODES

| BAUD RATE | SYNC = 0, BRGH = 0 | | | | | | | | | | | |
|-----------|--------------------|---------|-----------------------|-------------------|---------|-----------------------|--------------------|---------|-----------------------|--------------------|---------|-----------------------|
| | Fosc = 20.000 MHz | | | Fosc = 18.432 MHz | | | Fosc = 16.0000 MHz | | | Fosc = 11.0592 MHz | | |
| | Actual Rate | % Error | SPBRG value (decimal) | Actual Rate | % Error | SPBRG value (decimal) | Actual Rate | % Error | SPBRG value (decimal) | Actual Rate | % Error | SPBRG value (decimal) |
| 300 | — | — | — | — | — | — | — | — | — | — | — | — |
| 1200 | 1221 | 1.73 | 255 | 1200 | 0.00 | 239 | 1201 | 0.08 | 207 | 1200 | 0.00 | 143 |
| 2400 | 2404 | 0.16 | 129 | 2400 | 0.00 | 119 | 2403 | 0.16 | 103 | 2400 | 0.00 | 71 |
| 9600 | 9470 | -1.36 | 32 | 9600 | 0.00 | 29 | 9615 | 0.16 | 25 | 9600 | 0.00 | 17 |
| 10417 | 10417 | 0.00 | 29 | 10286 | -1.26 | 27 | 10416 | -0.01 | 23 | 10165 | -2.42 | 16 |
| 19.2k | 19.53k | 1.73 | 15 | 19.20k | 0.00 | 14 | 19.23k | 0.16 | 12 | 19.20k | 0.00 | 8 |
| 57.6k | — | — | — | 57.60k | 0.00 | 7 | — | — | — | 57.60k | 0.00 | 2 |
| 115.2k | — | — | — | — | — | — | — | — | — | — | — | — |

| BAUD RATE | SYNC = 0, BRGH = 0 | | | | | | | | | | | |
|-----------|--------------------|---------|-----------------------|------------------|---------|-----------------------|-------------------|---------|-----------------------|------------------|---------|-----------------------|
| | Fosc = 8.000 MHz | | | Fosc = 4.000 MHz | | | Fosc = 3.6864 MHz | | | Fosc = 1.000 MHz | | |
| | Actual Rate | % Error | SPBRG value (decimal) | Actual Rate | % Error | SPBRG value (decimal) | Actual Rate | % Error | SPBRG value (decimal) | Actual Rate | % Error | SPBRG value (decimal) |
| 300 | — | — | — | 300 | 0.16 | 207 | 300 | 0.00 | 191 | 300 | 0.16 | 51 |
| 1200 | 1202 | 0.16 | 103 | 1202 | 0.16 | 51 | 1200 | 0.00 | 47 | 1202 | 0.16 | 12 |
| 2400 | 2404 | 0.16 | 51 | 2404 | 0.16 | 25 | 2400 | 0.00 | 23 | — | — | — |
| 9600 | 9615 | 0.16 | 12 | — | — | — | 9600 | 0.00 | 5 | — | — | — |
| 10417 | 10417 | 0.00 | 11 | 10417 | 0.00 | 5 | — | — | — | — | — | — |
| 19.2k | — | — | — | — | — | — | 19.20k | 0.00 | 2 | — | — | — |
| 57.6k | — | — | — | — | — | — | 57.60k | 0.00 | 0 | — | — | — |
| 115.2k | — | — | — | — | — | — | — | — | — | — | — | — |

| BAUD RATE | SYNC = 0, BRGH = 1 | | | | | | | | | | | |
|-----------|--------------------|---------|-----------------------|-------------------|---------|-----------------------|--------------------|---------|-----------------------|--------------------|---------|-----------------------|
| | Fosc = 20.000 MHz | | | Fosc = 18.432 MHz | | | Fosc = 16.0000 MHz | | | Fosc = 11.0592 MHz | | |
| | Actual Rate | % Error | SPBRG value (decimal) | Actual Rate | % Error | SPBRG value (decimal) | Actual Rate | % Error | SPBRG value (decimal) | Actual Rate | % Error | SPBRG value (decimal) |
| 300 | — | — | — | — | — | — | — | — | — | — | — | — |
| 1200 | — | — | — | — | — | — | — | — | — | — | — | — |
| 2400 | — | — | — | — | — | — | — | — | — | — | — | — |
| 9600 | 9615 | 0.16 | 129 | 9600 | 0.00 | 119 | 9615 | 0.16 | 103 | 9600 | 0.00 | 71 |
| 10417 | 10417 | 0.00 | 119 | 10378 | -0.37 | 110 | 10417 | 0.00 | 95 | 10473 | 0.53 | 65 |
| 19.2k | 19.23k | 0.16 | 64 | 19.20k | 0.00 | 59 | 19.23k | 0.16 | 51 | 19.20k | 0.00 | 35 |
| 57.6k | 56.82k | -1.36 | 21 | 57.60k | 0.00 | 19 | 58.8k | 2.12 | 16 | 57.60k | 0.00 | 11 |
| 115.2k | 113.64k | -1.36 | 10 | 115.2k | 0.00 | 9 | — | — | — | 115.2k | 0.00 | 5 |

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TABLE 16-5: BAUD RATES FOR ASYNCHRONOUS MODES

| BAUD RATE | SYNC = 0, BRGH = 1 | | | | | | | | | | | |
|-----------|--------------------|---------|-----------------------|------------------|---------|-----------------------|-------------------|---------|-----------------------|------------------|---------|-----------------------|
| | Fosc = 8.000 MHz | | | Fosc = 4.000 MHz | | | Fosc = 3.6864 MHz | | | Fosc = 1.000 MHz | | |
| | Actual Rate | % Error | SPBRG value (decimal) | Actual Rate | % Error | SPBRG value (decimal) | Actual Rate | % Error | SPBRG value (decimal) | Actual Rate | % Error | SPBRG value (decimal) |
| 300 | — | — | — | — | — | — | — | — | — | 300 | 0.16 | 207 |
| 1200 | — | — | — | 1202 | 0.16 | 207 | 1200 | 0.00 | 191 | 1202 | 0.16 | 51 |
| 2400 | 2404 | 0.16 | 207 | 2404 | 0.16 | 103 | 2400 | 0.00 | 95 | 2404 | 0.16 | 25 |
| 9600 | 9615 | 0.16 | 51 | 9615 | 0.16 | 25 | 9600 | 0.00 | 23 | — | — | — |
| 10417 | 10417 | 0.00 | 47 | 10417 | 0.00 | 23 | 10473 | 0.53 | 21 | 10417 | 0.00 | 5 |
| 19.2k | 19231 | 0.16 | 25 | 19.23k | 0.16 | 12 | 19.2k | 0.00 | 11 | — | — | — |
| 57.6k | 55556 | -3.55 | 8 | — | — | — | 57.60k | 0.00 | 3 | — | — | — |
| 115.2k | — | — | — | — | — | — | 115.2k | 0.00 | 1 | — | — | — |

17.0 SSP MODULE OVERVIEW

The Synchronous Serial Port (SSP) module is a serial interface useful for communicating with other peripherals or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I²C)

17.1 SPI Mode

The SPI mode allows eight bits of data to be synchronously transmitted and received, simultaneously. The SSP module can be operated in one of two SPI modes:

- Master mode
- Slave mode

SPI is a full-duplex protocol, with all communication being bidirectional and initiated by a master device. All clocking is provided by the master device and all bits are transmitted, MSb first. Care must be taken to ensure that all devices on the SPI bus are setup to allow all controllers to send and receive data at the same time.

A typical SPI connection between microcontroller devices is shown in Figure 17-1. Addressing of more than one slave device is accomplished via multiple hardware slave select lines. External hardware and additional I/O pins must be used to support multiple slave select addressing. This prevents extra overhead in software for communication.

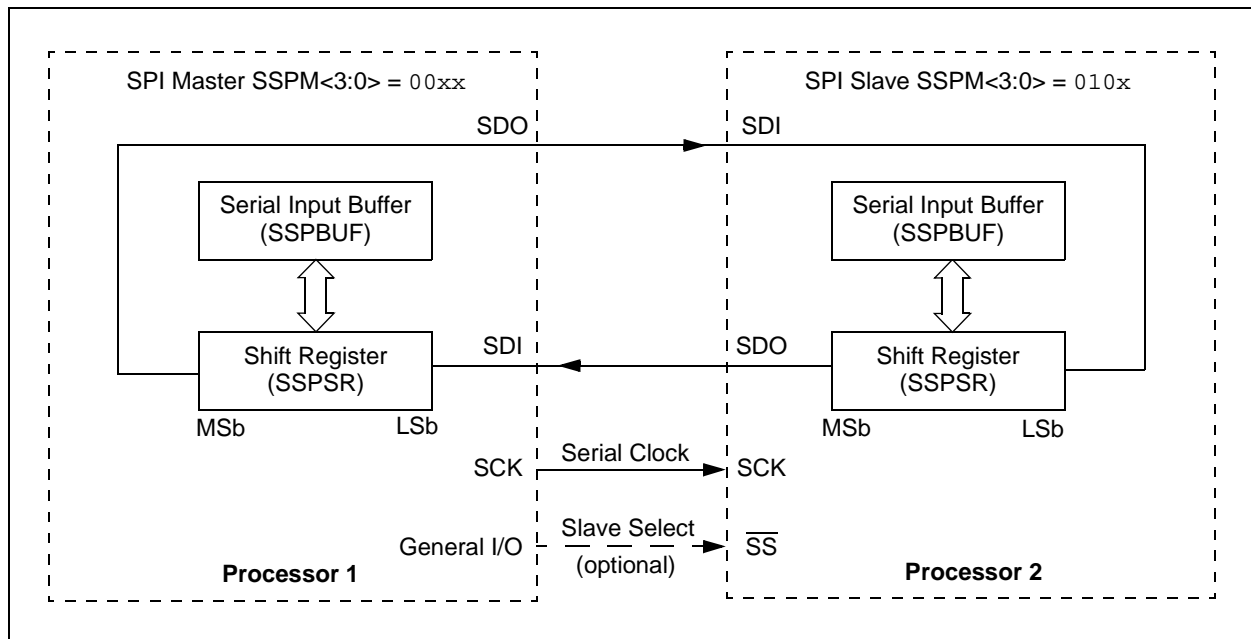
For SPI communication, typically three pins are used:

- Serial Data Out (SDO)
- Serial Data In (SDI)
- Serial Clock (SCK)

Additionally, a fourth pin may be used when in a Slave mode of operation:

- Slave Select (\overline{SS})

FIGURE 17-1: TYPICAL SPI MASTER/SLAVE CONNECTION



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REGISTER 17-1: SSPCON: SYNC SERIAL PORT CONTROL REGISTER (SPI MODE)

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| WCOL | SSPOV | SSPEN | CKP | SSPM3 | SSPM2 | SSPM1 | SSPM0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **WCOL**: Write Collision Detect bit
1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision
- bit 6 **SSPOV**: Receive Overflow Indicator bit
1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in Slave mode. The user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register.
0 = No overflow
- bit 5 **SSPEN**: Synchronous Serial Port Enable bit
1 = Enables serial port and configures SCK, SDO and SDI as serial port pins⁽¹⁾
0 = Disables serial port and configures these pins as I/O port pins
- bit 4 **CKP**: Clock Polarity Select bit
1 = Idle state for clock is a high level
0 = Idle state for clock is a low level
- bit 3-0 **SSPM<3:0>**: Synchronous Serial Port Mode Select bits
0000 = SPI Master mode, clock = Fosc/4
0001 = SPI Master mode, clock = Fosc/16
0010 = SPI Master mode, clock = Fosc/64
0011 = SPI Master mode, clock = TMR2 output/2
0100 = SPI Slave mode, clock = SCK pin. \overline{SS} pin control enabled.
0101 = SPI Slave mode, clock = SCK pin. \overline{SS} pin control disabled. \overline{SS} can be used as I/O pin.

Note 1: When enabled, these pins must be properly configured as input or output.

DECFSZ Decrement f, Skip if 0

Syntax: [*label*] DECFSZ f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) - 1 \rightarrow (\text{destination});$
skip if result = 0

Status Affected: None

Description: The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.
If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a 2-cycle instruction.

INCFSZ Increment f, Skip if 0

Syntax: [*label*] INCFSZ f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) + 1 \rightarrow (\text{destination});$
skip if result = 0

Status Affected: None

Description: The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.
If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a 2-cycle instruction.

GOTO Unconditional Branch

Syntax: [*label*] GOTO k

Operands: $0 \leq k \leq 2047$

Operation: $k \rightarrow \text{PC}<10:0>$
 $\text{PCLATH}<4:3> \rightarrow \text{PC}<12:11>$

Status Affected: None

Description: GOTO is an unconditional branch. The 11-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a 2-cycle instruction.

IORLW Inclusive OR literal with W

Syntax: [*label*] IORLW k

Operands: $0 \leq k \leq 255$

Operation: $(W) .OR. k \rightarrow (W)$

Status Affected: Z

Description: The contents of the W register are OR'ed with the 8-bit literal 'k'. The result is placed in the W register.

INCF Increment f

Syntax: [*label*] INCF f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) + 1 \rightarrow (\text{destination})$

Status Affected: Z

Description: The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

IORWF Inclusive OR W with f

Syntax: [*label*] IORWF f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(W) .OR. (f) \rightarrow (\text{destination})$

Status Affected: Z

Description: Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

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TABLE 23-2: OSCILLATOR PARAMETERS

| Standard Operating Conditions (unless otherwise stated) | | | | | | | | |
|--|----------|---|-----------------|------|------|------|---------------|---|
| Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | | | | | | | | |
| Param No. | Sym. | Characteristic | Freq. Tolerance | Min. | Typ† | Max. | Units | Conditions |
| OS08 | HFosc | Internal Calibrated HFINTOSC Frequency ⁽²⁾ | $\pm 2\%$ | — | 16.0 | — | MHz | $0^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, $V_{DD} \geq 2.5\text{V}$ |
| | | | $\pm 5\%$ | — | 16.0 | — | MHz | $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ |
| OS08A | MFosc | Internal Calibrated MFINTOSC Frequency ⁽²⁾ | $\pm 2\%$ | — | 500 | — | kHz | $0^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, $V_{DD} \geq 2.5\text{V}$ |
| | | | $\pm 5\%$ | — | 500 | 10 | kHz | $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ |
| OS10* | Tiosc st | HFINTOSC Wake-up from Sleep Start-up Time | — | — | 5 | 8 | μs | |
| | | MFINTOSC Wake-up from Sleep Start-up Time | — | — | 20 | 30 | μs | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.
- 2:** To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.
- 3:** By design.

FIGURE 23-7: CLKOUT AND I/O TIMING

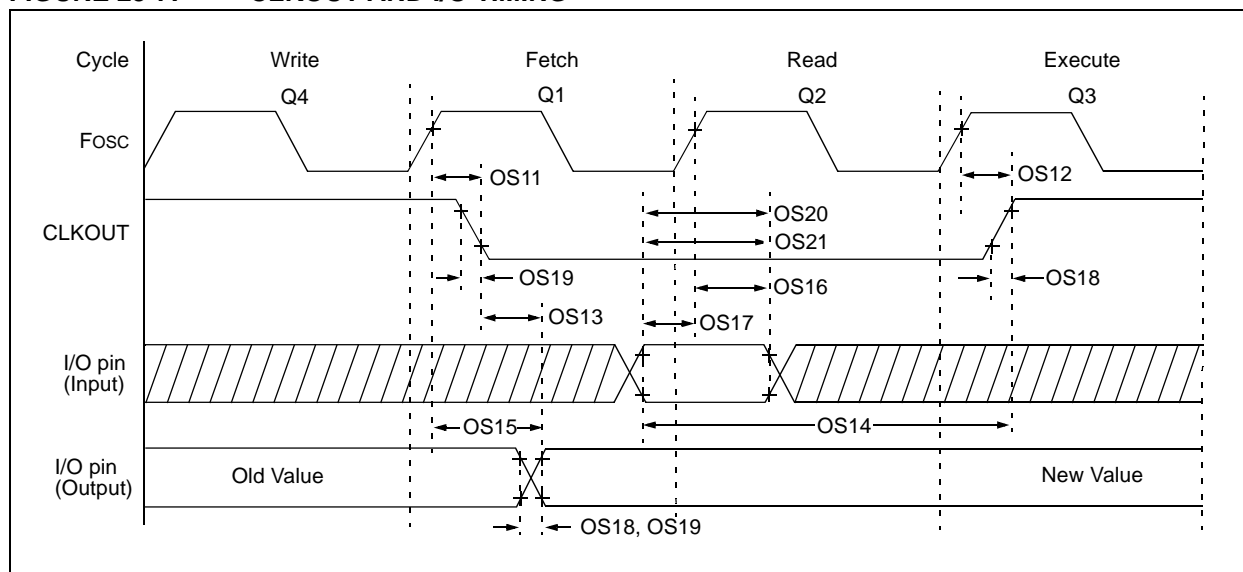


FIGURE 23-14: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

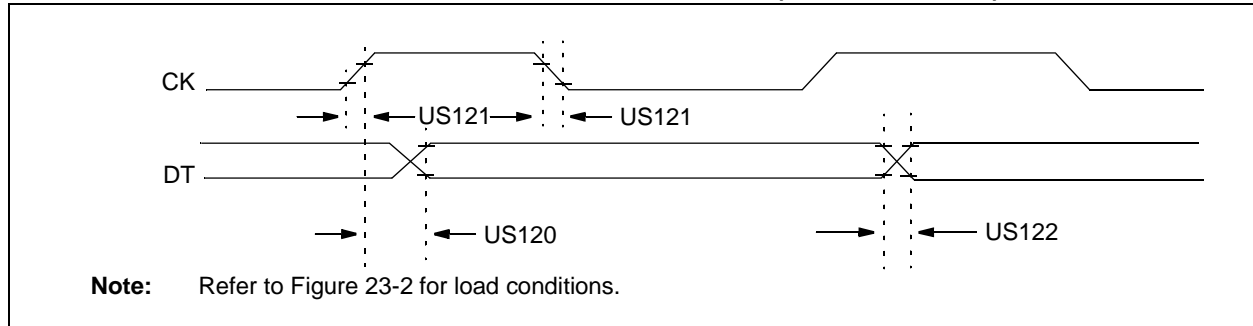


TABLE 23-9: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

| Standard Operating Conditions (unless otherwise stated) | | | | | | | |
|--|----------|--|----------|------|------|-------|------------|
| Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | | | | | | | |
| Param. No. | Symbol | Characteristic | | Min. | Max. | Units | Conditions |
| US120 | TCKH2DTV | SYNC XMIT (Master and Slave) Clock high to data-out valid | 3.0-5.5V | — | 80 | ns | |
| | | | 1.8-5.5V | — | 100 | ns | |
| US121 | TCKRF | Clock out rise time and fall time (Master mode) | 3.0-5.5V | — | 45 | ns | |
| | | | 1.8-5.5V | — | 50 | ns | |
| US122 | TDTRF | Data-out rise time and fall time | 3.0-5.5V | — | 45 | ns | |
| | | | 1.8-5.5V | — | 50 | ns | |

FIGURE 23-15: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

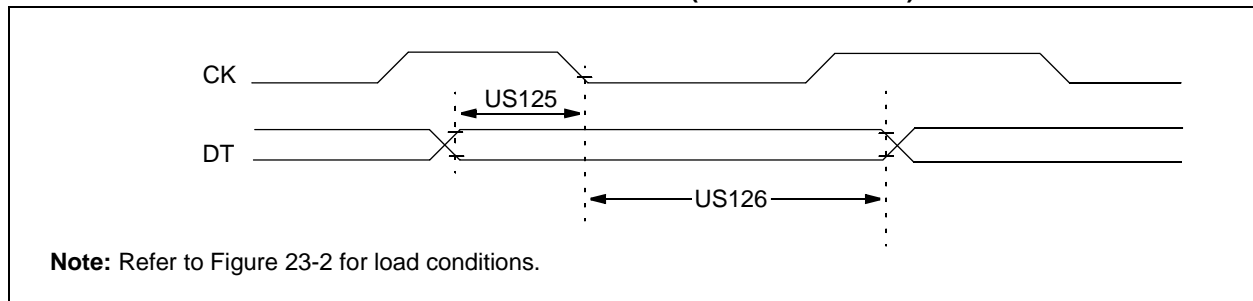


TABLE 23-10: USART SYNCHRONOUS RECEIVE REQUIREMENTS

| Standard Operating Conditions (unless otherwise stated) | | | | | | | |
|--|----------|--|------|------|-------|------------|--|
| Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | | | | | | | |
| Param. No. | Symbol | Characteristic | Min. | Max. | Units | Conditions | |
| US125 | TDTV2CKL | SYNC RCV (Master and Slave) Data-hold before CK \downarrow (DT hold time) | 10 | — | ns | | |
| US126 | TCKL2DTL | Data-hold after CK \downarrow (DT hold time) | 15 | — | ns | | |

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FIGURE 24-65: PIC16F722/3/4/6/7 CAP SENSOR HYSTERESIS, POWER MODE = HIGH

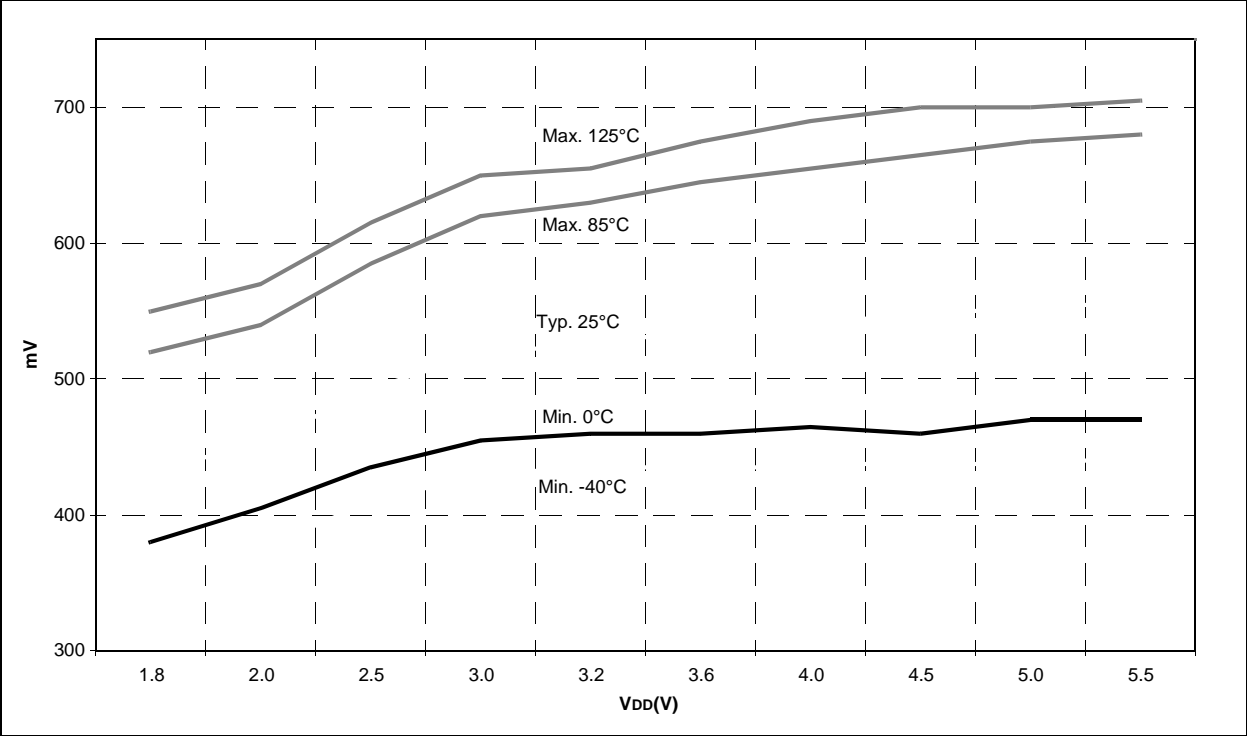
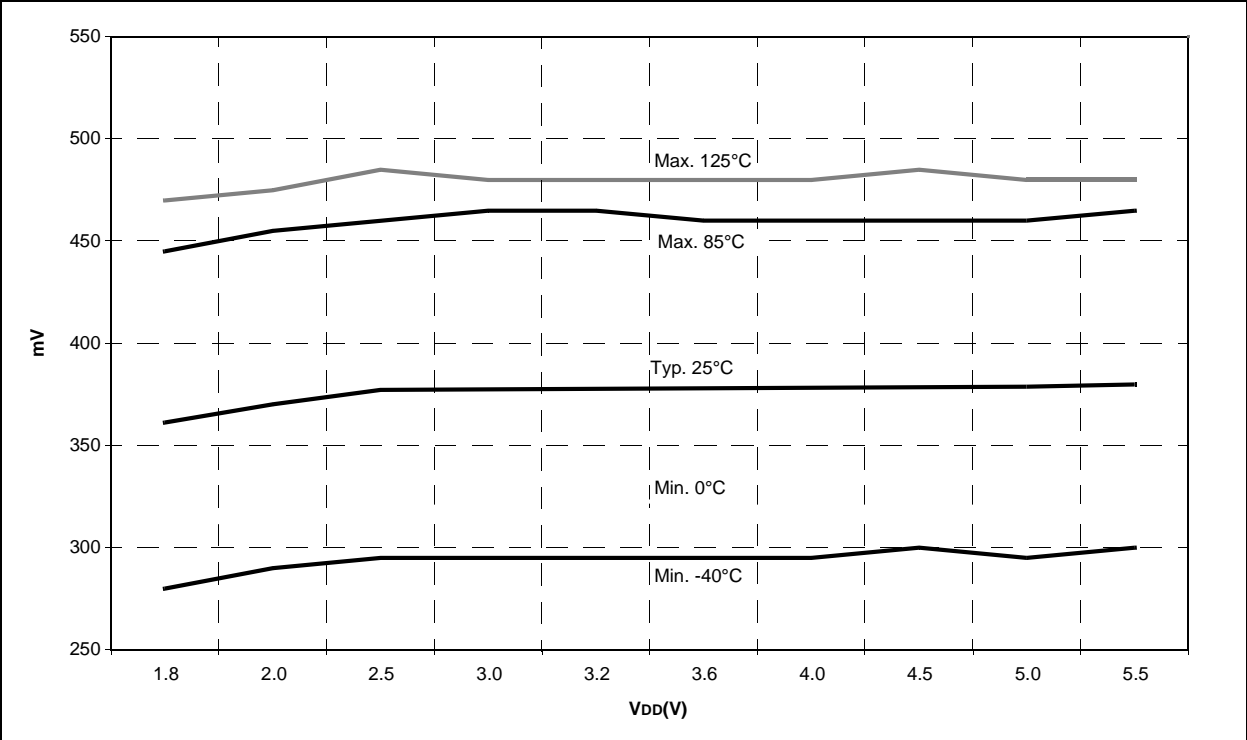


FIGURE 24-66: PIC16F722/3/4/6/7 CAP SENSOR HYSTERESIS, POWER MODE = MEDIUM

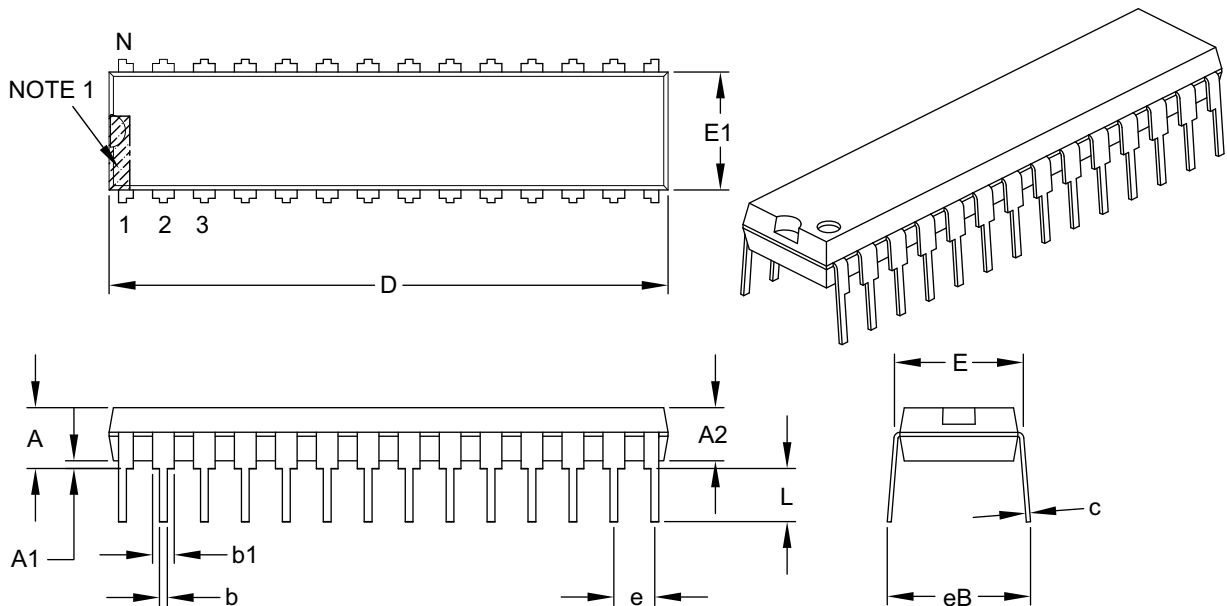


25.2 Package Details

The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units | | INCHES | | |
|----------------------------|----|----------|-------|-------|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 28 | | |
| Pitch | e | .100 BSC | | |
| Top to Seating Plane | A | – | – | .200 |
| Molded Package Thickness | A2 | .120 | .135 | .150 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .335 |
| Molded Package Width | E1 | .240 | .285 | .295 |
| Overall Length | D | 1.345 | 1.365 | 1.400 |
| Tip to Seating Plane | L | .110 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .050 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B