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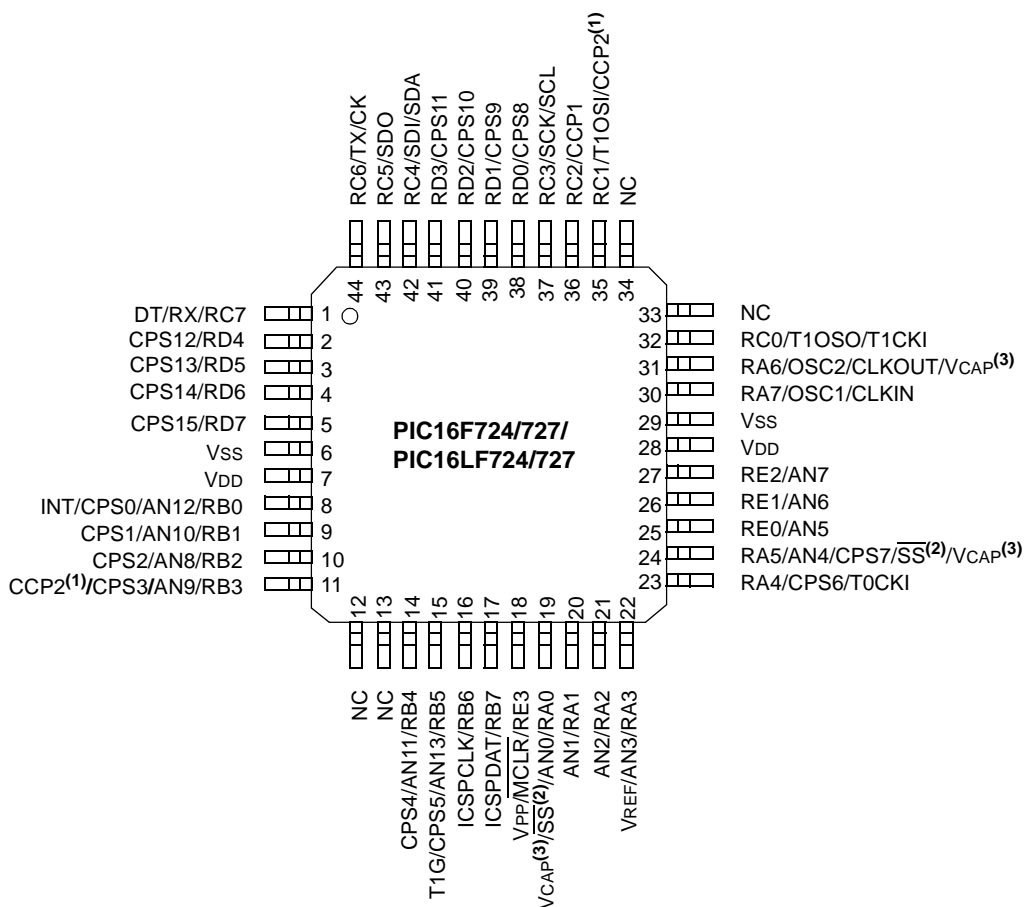
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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf726-i-ss

PIC16(L)F722/3/4/6/7

Pin Diagrams – 44-PIN TQFP (PIC16F724/727/PIC16LF724/727)



Note 1: CCP2 pin location may be selected as RB3 or RC1.

2: SS pin location may be selected as RA5 or RA0.

3: PIC16F724/727 devices only.

PIC16(L)F722/3/4/6/7

3.0 RESETS

The PIC16(L)F722/3/4/6/7 differentiates between various kinds of Reset:

- Power-on Reset (POR)
- WDT Reset during normal operation
- WDT Reset during Sleep
- $\overline{\text{MCLR}}$ Reset during normal operation
- $\overline{\text{MCLR}}$ Reset during Sleep
- Brown-out Reset (BOR)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on:

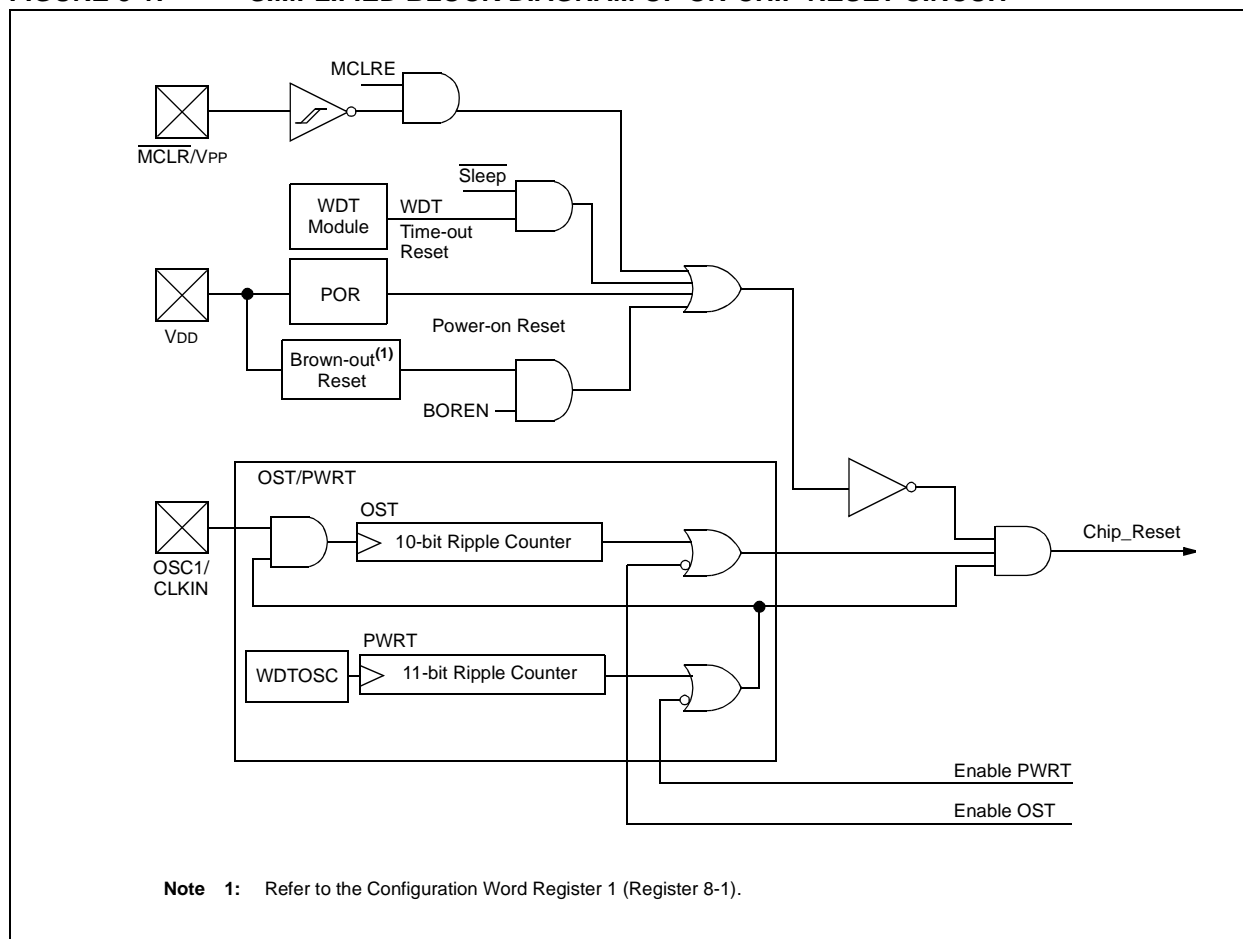
- Power-on Reset (POR)
- $\overline{\text{MCLR}}$ Reset
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Reset
- Brown-out Reset (BOR)

Most registers are not affected by a WDT wake-up since this is viewed as the resumption of normal operation. $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different Reset situations, as indicated in Table 3-3. These bits are used in software to determine the nature of the Reset.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 3-1.

The $\overline{\text{MCLR}}$ Reset path has a noise filter to detect and ignore small pulses. See **Section 23.0 "Electrical Specifications"** for pulse-width specifications.

FIGURE 3-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



PIC16(L)F722/3/4/6/7

REGISTER 6-13: TRISD: PORTD TRI-STATE REGISTER⁽¹⁾

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

TRISD<7:0>: PORTD Tri-State Control bits

1 = PORTD pin configured as an input (tri-stated)

0 = PORTD pin configured as an output

Note 1: TRISD is not implemented on PIC16F722/723/726/PIC16LF722/723/726 devices, read as '0'.

REGISTER 6-14: ANSELD: PORTD ANALOG SELECT REGISTER⁽²⁾

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

ANS<7:0>: Analog Select between Analog or Digital Function on Pins RD<7:0>, respectively

0 = Digital I/O. Pin is assigned to port or Digital special function.

1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital Input buffer disabled.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

2: ANSELD register is not implemented on the PIC16F722/723/726/PIC16LF722/723/726. Read as '0'.

Note: PORTD is available on PIC16F724/LF724 and PIC16F727/LF727 only.

6.5.2 RD0/CPS8

Figure 6-21 shows the diagram for these pins. They are configurable to function as one of the following:

- a general purpose I/O
- a capacitive sensing input

6.5.3 RD1/CPS9

Figure 6-21 shows the diagram for these pins. They are configurable to function as one of the following:

- a general purpose I/O
- a capacitive sensing input

6.5.4 RD2/CPS10

Figure 6-21 shows the diagram for these pins. They are configurable to function as one of the following:

- a general purpose I/O
- a capacitive sensing input

6.5.5 RD3/CPS11

Figure 6-21 shows the diagram for these pins. They are configurable to function as one of the following:

- a general purpose I/O
- a capacitive sensing input

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REGISTER 8-1: CONFIG1: CONFIGURATION WORD REGISTER 1 (CONTINUED)

bit 4	PWRT : Power-up Timer Enable bit 1 = PWRT disabled 0 = PWRT enabled
bit 3	WDTE : Watchdog Timer Enable bit 1 = WDT enabled 0 = WDT disabled
bit 2-0	FOSC<2:0> : Oscillator Selection bits 111 = RC oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, RC on RA7/OSC1/CLKIN 110 = RCIO oscillator: I/O function on RA6/OSC2/CLKOUT pin, RC on RA7/OSC1/CLKIN 101 = INTOSC oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN 100 = INTOSCIO oscillator: I/O function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN 011 = EC: I/O function on RA6/OSC2/CLKOUT pin, CLKIN on RA7/OSC1/CLKIN 010 = HS oscillator: High-speed crystal/resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN 001 = XT oscillator: Crystal/resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN 000 = LP oscillator: Low-power crystal on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN

- Note 1:** Enabling Brown-out Reset does not automatically enable Power-up Timer.
Note 2: The entire program memory will be erased when the code protection is turned off.
Note 3: When **MCLR** is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.
Note 4: MPLAB® X IDE masks unimplemented Configuration bits to '0'.

REGISTER 8-2: CONFIG2: CONFIGURATION WORD REGISTER 2

	U-1 ⁽¹⁾	U-1 ⁽¹⁾	U-1 ⁽¹⁾	U-1 ⁽¹⁾	U-1 ⁽¹⁾	U-1 ⁽¹⁾	U-1 ⁽¹⁾
	—	—	—	—	—	—	—
bit 15							bit 8

U-1 ⁽¹⁾	U-1 ⁽¹⁾	R/P-1	R/P-1	U-1 ⁽¹⁾	U-1 ⁽¹⁾	U-1 ⁽¹⁾	U-1 ⁽¹⁾
—	—	VCAPEN1	VCAPEN0	—	—	—	—
bit 7							bit 0

Legend:	P = Programmable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 13-6	Unimplemented: Read as '1'
bit 5-4	VCAPEN<1:0> : Voltage Regulator Capacitor Enable bits <u>For the PIC16LF72X:</u> These bits are ignored. All VCAP pin functions are disabled. <u>For the PIC16F72X:</u> 00 = VCAP functionality is enabled on RA0 01 = VCAP functionality is enabled on RA5 10 = VCAP functionality is enabled on RA6 11 = All VCAP functions are disabled (not recommended)
bit 3-0	Unimplemented: Read as '1'

- Note 1:** MPLAB® X IDE masks unimplemented Configuration bits to '0'.

9.3 A/D Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 9-3. The source impedance (Rs) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), refer to Figure 9-3. **The maximum recommended impedance for analog sources is 10 kΩ.** As the source

impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an A/D acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 9-1 may be used. This equation assumes that 1/2 LSB error is used (256 steps for the ADC). The 1/2 LSB error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 9-1: ACQUISITION TIME EXAMPLE

Assumptions: Temperature = 50°C and external impedance of 10kΩ 5.0V VDD

$$\begin{aligned} T_{ACQ} &= \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= T_{AMP} + T_C + T_{COFF} \\ &= 2\mu s + T_C + [(Temperature - 25^\circ C)(0.05\mu s/^\circ C)] \end{aligned}$$

The value for TC can be approximated with the following equations:

$$V_{APPLIED} \left(1 - \frac{1}{(2^{n+1}) - 1} \right) = V_{CHOLD} \quad ;[1] \text{ } V_{CHOLD} \text{ charged to within } 1/2 \text{ lsb}$$

$$V_{APPLIED} \left(1 - e^{\frac{-T_C}{RC}} \right) = V_{CHOLD} \quad ;[2] \text{ } V_{CHOLD} \text{ charge response to } V_{APPLIED}$$

$$V_{APPLIED} \left(1 - e^{\frac{-T_C}{RC}} \right) = V_{APPLIED} \left(1 - \frac{1}{(2^{n+1}) - 1} \right) \quad ;\text{combining [1] and [2]}$$

Note: Where n = number of bits of the ADC.

Solving for TC:

$$\begin{aligned} T_C &= -CHOLD(RIC + RSS + Rs) \ln(1/511) \\ &= -10pF(1k\Omega + 7k\Omega + 10k\Omega) \ln(0.001957) \\ &= 1.12\mu s \end{aligned}$$

Therefore:

$$\begin{aligned} T_{ACQ} &= 2MS + 1.12MS + [(50^\circ C - 25^\circ C)(0.05MS/^\circ C)] \\ &= 4.42MS \end{aligned}$$

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

TABLE 9-2: SUMMARY OF ASSOCIATED ADC REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	--00 0000	--00 0000
ADCON1	—	ADCS2	ADCS1	ADCS0	—	—	ADREF1	ADREF0	-000 --00	-000 --00
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	--11 1111	--11 1111
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	--11 1111	--11 1111
ANSELE	—	—	—	—	—	ANSE2	ANSE1	ANSE0	---- -111	---- -111
ADRES	A/D Result Register Byte								xxxx xxxx	uuuu uuuu
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000
FVRCON	FVRRDY	FVREN	—	—	—	—	ADFVR1	ADFVR0	q0-- --00	q0-- --00
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111	1111 1111
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
TRISE	—	—	—	—	TRISE3	TRISE2	TRISE1	TRISE0	---- 1111	---- 1111

Legend: x = unknown, u = unchanged, — = unimplemented read as '0', q = value depends on condition. Shaded cells are not used for ADC module.

PIC16(L)F722/3/4/6/7

13.0 TIMER2 MODULE

The Timer2 module is an 8-bit timer with the following features:

- 8-bit timer register (TMR2)
- 8-bit period register (PR2)
- Interrupt on TMR2 match with PR2
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16)

See Figure 13-1 for a block diagram of Timer2.

13.1 Timer2 Operation

The clock input to the Timer2 module is the system instruction clock ($F_{osc}/4$). The clock is fed into the Timer2 prescaler, which has prescale options of 1:1, 1:4 or 1:16. The output of the prescaler is then used to increment the TMR2 register.

The values of TMR2 and PR2 are constantly compared to determine when they match. TMR2 will increment from 00h until it matches the value in PR2. When a match occurs, two things happen:

- TMR2 is reset to 00h on the next increment cycle.
- The Timer2 postscaler is incremented.

The match output of the Timer2/PR2 comparator is then fed into the Timer2 postscaler. The postscaler has postscale options of 1:1 to 1:16 inclusive. The output of the Timer2 postscaler is used to set the TMR2IF interrupt flag bit in the PIR1 register.

The TMR2 and PR2 registers are both fully readable and writable. On any Reset, the TMR2 register is set to 00h and the PR2 register is set to FFh.

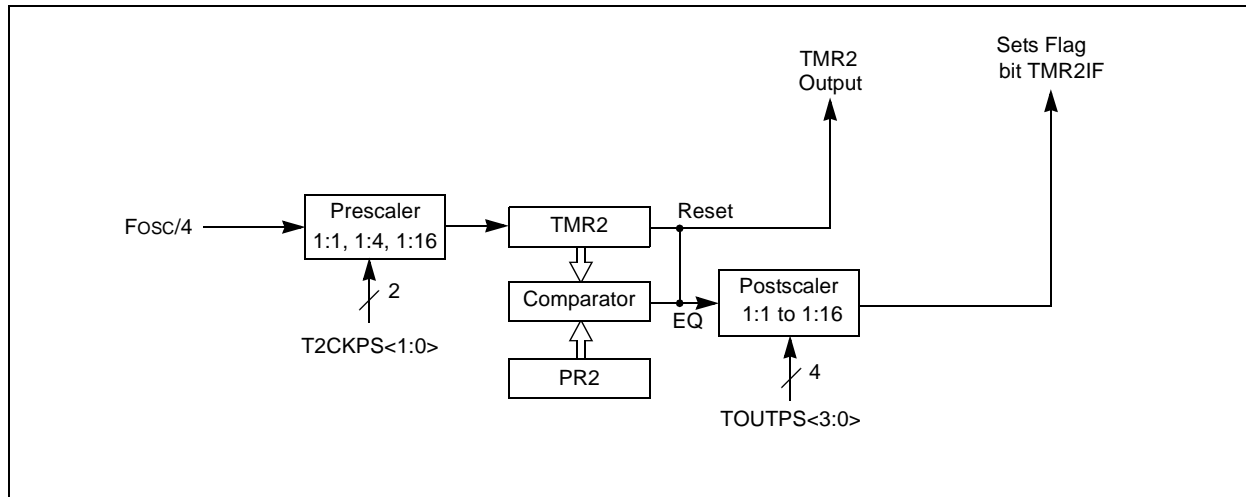
Timer2 is turned on by setting the TMR2ON bit in the T2CON register to a '1'. Timer2 is turned off by clearing the TMR2ON bit to a '0'.

The Timer2 prescaler is controlled by the T2CKPS bits in the T2CON register. The Timer2 postscaler is controlled by the TOUTPS bits in the T2CON register. The prescaler and postscaler counters are cleared when:

- A write to TMR2 occurs.
- A write to T2CON occurs.
- Any device Reset occurs (Power-on Reset, \overline{MCLR} Reset, Watchdog Timer Reset, or Brown-out Reset).

Note: TMR2 is not cleared when T2CON is written.

FIGURE 13-1: TIMER2 BLOCK DIAGRAM



14.1 Analog MUX

The capacitive sensing module can monitor up to 16 inputs. The capacitive sensing inputs are defined as CPS<15:0>. To determine if a frequency change has occurred the user must:

- Select the appropriate CPS pin by setting the CPSCH<3:0> bits of the CPSCON1 register
- Set the corresponding ANSEL bit
- Set the corresponding TRIS bit
- Run the software algorithm

Selection of the CPSx pin while the module is enabled will cause the capacitive sensing oscillator to be on the CPSx pin. Failure to set the corresponding ANSEL and TRIS bits can cause the capacitive sensing oscillator to stop, leading to false frequency readings.

14.2 Capacitive Sensing Oscillator

The capacitive sensing oscillator consists of a constant current source and a constant current sink, to produce a triangle waveform. The CPSOUT bit of the CPSCON0 register shows the status of the capacitive sensing oscillator, whether it is a sinking or sourcing current. The oscillator is designed to drive a capacitive load (single PCB pad) and at the same time, be a clock source to either Timer0 or Timer1. The oscillator has three different current settings as defined by CPSRNG<1:0> of the CPSCON0 register. The different current settings for the oscillator serve two purposes:

- Maximize the number of counts in a timer for a fixed time base
- Maximize the count differential in the timer during a change in frequency

14.3 Timer resources

To measure the change in frequency of the capacitive sensing oscillator, a fixed time base is required. For the period of the fixed time base, the capacitive sensing oscillator is used to clock either Timer0 or Timer1. The frequency of the capacitive sensing oscillator is equal to the number of counts in the timer divided by the period of the fixed time base.

14.4 Fixed Time Base

To measure the frequency of the capacitive sensing oscillator, a fixed time base is required. Any timer resource or software loop can be used to establish the fixed time base. It is up to the end user to determine the method in which the fixed time base is generated.

Note: The fixed time base can not be generated by timer resource the capacitive sensing oscillator is clocking.

14.4.1 TIMER0

To select Timer0 as the timer resource for the capacitive sensing module:

- Set the T0XCS bit of the CPSCON0 register
- Clear the T0CS bit of the OPTION register

When Timer0 is chosen as the timer resource, the capacitive sensing oscillator will be the clock source for Timer0. Refer to **Section 11.0 “Timer0 Module”** for additional information.

14.4.2 TIMER1

To select Timer1 as the timer resource for the capacitive sensing module, set the TMR1CS<1:0> of the T1CON register to ‘11’. When Timer1 is chosen as the timer resource, the capacitive sensing oscillator will be the clock source for Timer1. Because the Timer1 module has a gate control, developing a time base for the frequency measurement can be simplified using either:

- The Timer0 overflow flag
- The Timer2 overflow flag
- The WDT overflow flag

It is recommend that one of these flags, in conjunction with the toggle mode of the Timer1 Gate, is used to develop the fixed time base required by the software portion of the capacitive sensing module. Refer to **Section 12.0 “Timer1 Module with Gate Control”** for additional information.

TABLE 14-1: TIMER1 ENABLE FUNCTION

TMR1ON	TMR1GE	Timer1 Operation
0	0	Off
0	1	Off
1	0	On
1	1	Count Enabled by input

TABLE 15-4: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	--00 0000	--00 0000
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	--11 1111	--11 1111
APFCON	—	—	—	—	—	—	SSSEL	CCP2SEL	---- --00	---- --00
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000
CCPRxL	Capture/Compare/PWM Register X Low Byte								xxxx xxxx	uuuu uuuu
CCPRxH	Capture/Compare/PWM Register X High Byte								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIE2	—	—	—	—	—	—	—	CCP2IE	---- --0	---- --0
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIR2	—	—	—	—	—	—	—	CCP2IF	---- --0	---- --0
T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	—	TMR1ON	0000 00-0	uuuu uu-u
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/DONE	T1GVAL	T1GSS1	T1GSS0	0000 0x00	0000 0x00
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

Legend: — = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Compare.

16.1.1.4 TSR Status

The TRMT bit of the TXSTA register indicates the status of the TSR register. This is a read-only bit. The TRMT bit is set when the TSR register is empty and is cleared when a character is transferred to the TSR register from the TXREG. The TRMT bit remains clear until all bits have been shifted out of the TSR register. No interrupt logic is tied to this bit, so the user has to poll this bit to determine the TSR status.

Note: The TSR register is not mapped in data memory, so it is not available to the user.

16.1.1.5 Transmitting 9-Bit Characters

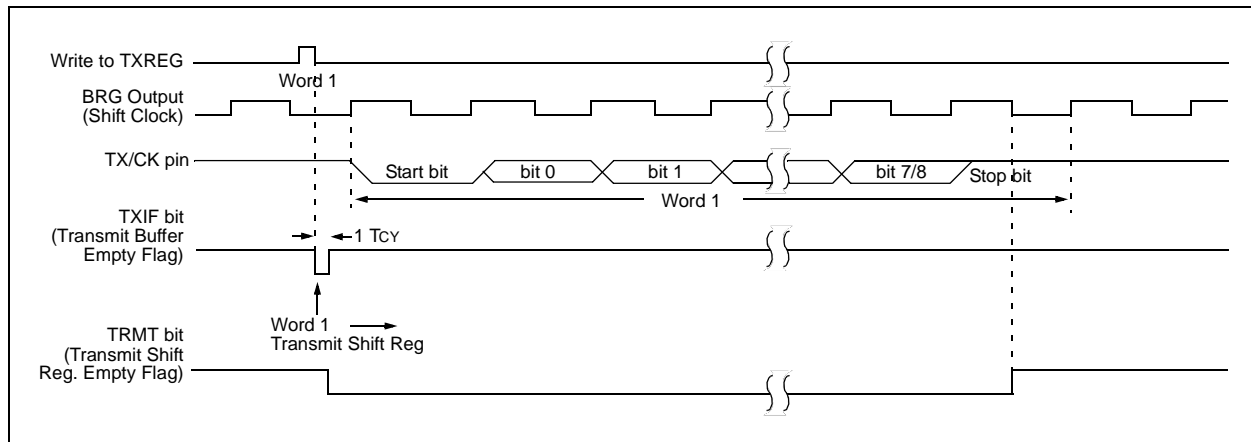
The AUSART supports 9-bit character transmissions. When the TX9 bit of the TXSTA register is set the AUSART will shift nine bits out for each character transmitted. The TX9D bit of the TXSTA register is the ninth, and Most Significant, data bit. When transmitting 9-bit data, the TX9D data bit must be written before writing the eight Least Significant bits into the TXREG. All nine bits of data will be transferred to the TSR shift register immediately after the TXREG is written.

A special 9-bit Address mode is available for use with multiple receivers. Refer to **Section 16.1.2.7 “Address Detection”** for more information on the Address mode.

16.1.1.6 Asynchronous Transmission Set-up:

1. Initialize the SPBRG register and the BRGH bit to achieve the desired baud rate (Refer to **Section 16.2 “AUSART Baud Rate Generator (BRG)”**).
2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
3. If 9-bit transmission is desired, set the TX9 control bit. A set ninth data bit will indicate that the eight Least Significant data bits are an address when the receiver is set for address detection.
4. Enable the transmission by setting the TXEN control bit. This will cause the TXIF interrupt bit to be set.
5. If interrupts are desired, set the TXIE interrupt enable bit of the PIE1 register. An interrupt will occur immediately provided that the GIE and PEIE bits of the INTCON register are also set.
6. If 9-bit transmission is selected, the ninth bit should be loaded into the TX9D data bit.
7. Load 8-bit data into the TXREG register. This will start the transmission.

FIGURE 16-3: ASYNCHRONOUS TRANSMISSION



16.1.2.8 Asynchronous Reception Set-up:

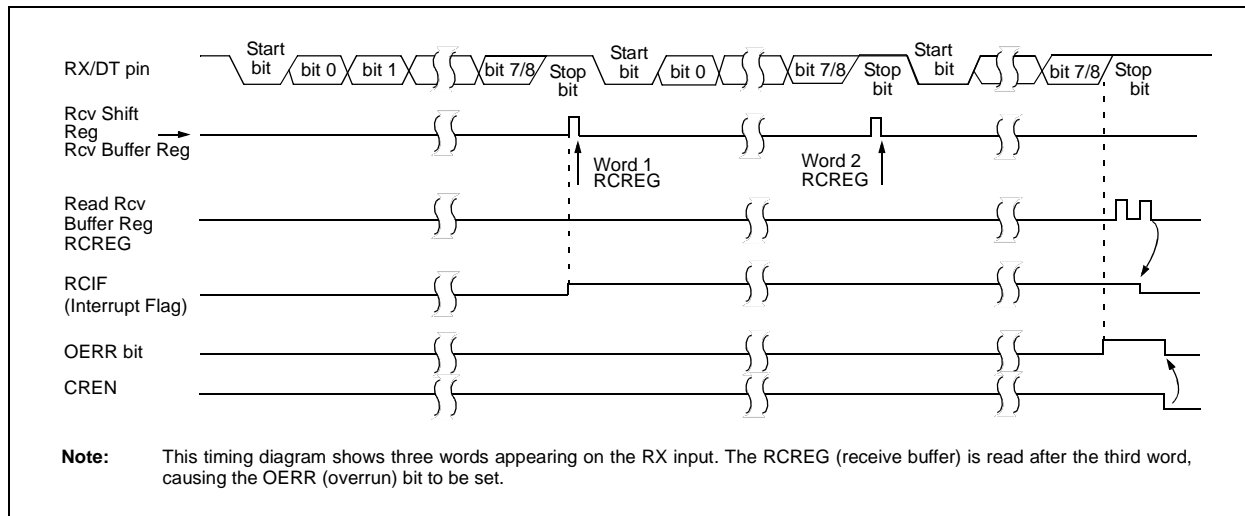
1. Initialize the SPBRG register and the BRGH bit to achieve the desired baud rate (refer to **Section 16.2 “AUSART Baud Rate Generator (BRG)”**).
2. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
3. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
4. If 9-bit reception is desired, set the RX9 bit.
5. Enable reception by setting the CREN bit.
6. The RCIF interrupt flag bit of the PIR1 register will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE bit of the PIE1 register was also set.
7. Read the RCSTA register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
8. Get the received eight Least Significant data bits from the receive buffer by reading the RCREG register.
9. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

16.1.2.9 9-bit Address Detection Mode Set-up

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:

1. Initialize the SPBRG register and the BRGH bit to achieve the desired baud rate (refer to **Section 16.2 “AUSART Baud Rate Generator (BRG)”**).
2. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
3. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
4. Enable 9-bit reception by setting the RX9 bit.
5. Enable address detection by setting the ADDEN bit.
6. Enable reception by setting the CREN bit.
7. The RCIF interrupt flag bit of the PIR1 register will be set when a character with the ninth bit set is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit of the PIE1 register was also set.
8. Read the RCSTA register to get the error flags. The ninth data bit will always be set.
9. Get the received eight Least Significant data bits from the receive buffer by reading the RCREG register. Software determines if this is the device's address.
10. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.
11. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and generate interrupts.

FIGURE 16-5: ASYNCHRONOUS RECEPTION



PIC16(L)F722/3/4/6/7

FIGURE 17-4: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 0)

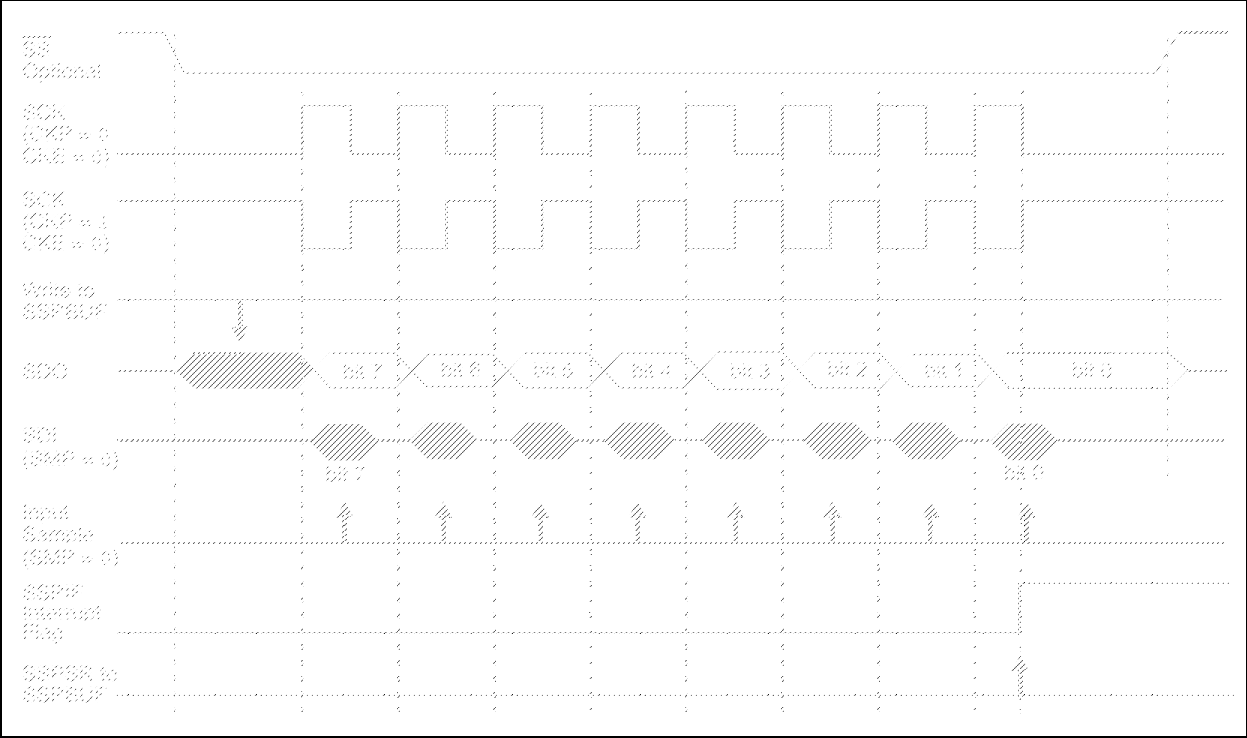
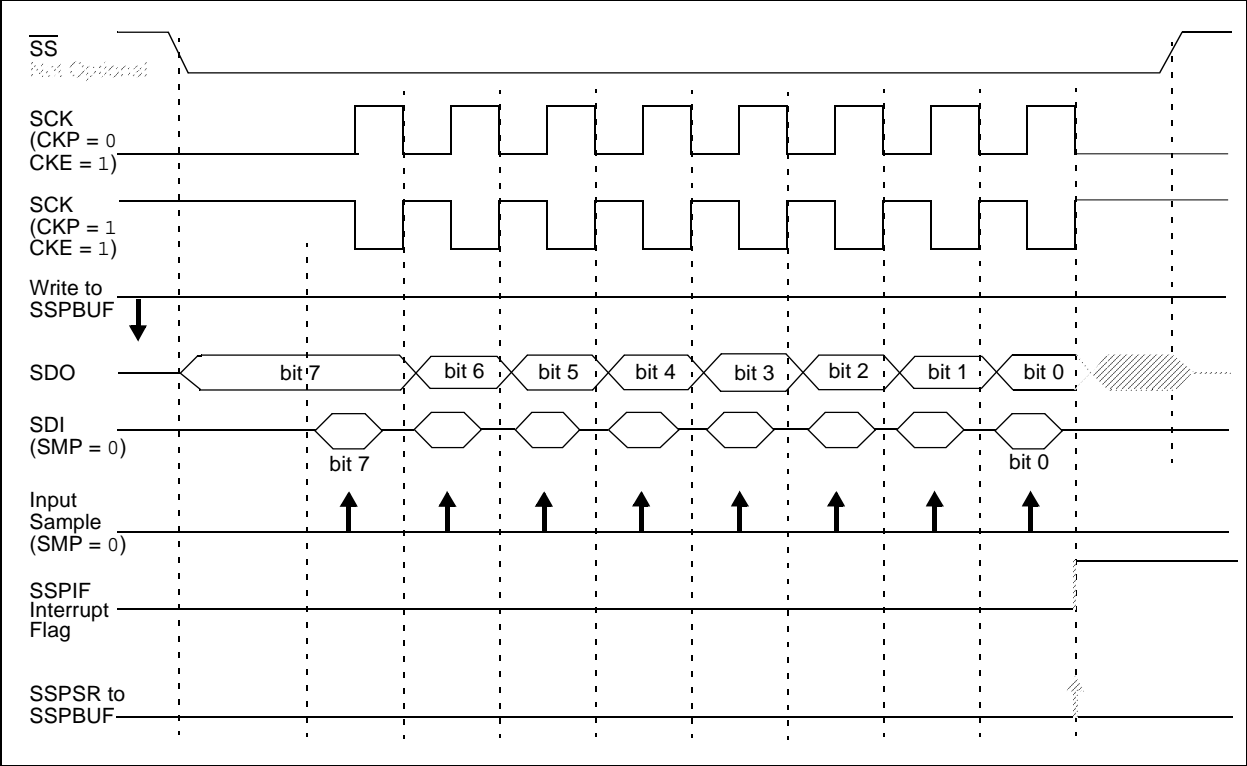


FIGURE 17-5: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)



PIC16(L)F722/3/4/6/7

17.2.7 CLOCK STRETCHING

During any SCL low phase, any device on the I²C bus may hold the SCL line low and delay, or pause, the transmission of data. This “stretching” of a transmission allows devices to slow down communication on the bus. The SCL line must be constantly sampled by the master to ensure that all devices on the bus have released SCL for more data.

Stretching usually occurs after an $\overline{\text{ACK}}$ bit of a transmission, delaying the first bit of the next byte. The SSP module hardware automatically stretches for two conditions:

- After a 10-bit address byte is received (update SSPADD register)
- Anytime the CKP bit of the SSPCON register is cleared by hardware

The module will hold SCL low until the CKP bit is set. This allows the user slave software to update SSPBUF with data that may not be readily available. In 10-bit addressing modes, the SSPADD register must be updated after receiving the first and second address bytes. The SSP module will hold the SCL line low until the SSPADD has a byte written to it. The UA bit of the SSPSTAT register will be set, along with SSPIF, indicating an address update is needed.

17.2.8 FIRMWARE MASTER MODE

Master mode of operation is supported in firmware using interrupt generation on the detection of the Start and Stop conditions. The Stop (P) and Start (S) bits of the SSPSTAT register are cleared from a Reset or when the SSP module is disabled (SSPEN cleared). The Stop (P) and Start (S) bits will toggle based on the Start and Stop conditions. Control of the I²C bus may be taken when the P bit is set or the bus is Idle and both the S and P bits are clear.

In Firmware Master mode, the SCL and SDA lines are manipulated by setting/clearing the corresponding TRIS bit(s). The output level is always low, irrespective of the value(s) in the corresponding PORT register bit(s). When transmitting a ‘1’, the TRIS bit must be set (input) and a ‘0’, the TRIS bit must be clear (output).

The following events will cause the SSP Interrupt Flag bit, SSPIF, to be set (SSP Interrupt will occur if enabled):

- Start condition
- Stop condition
- Data transfer byte transmitted/received

Firmware Master Mode of operation can be done with either the Slave mode Idle (SSPM<3:0> = 1011), or with either of the Slave modes in which interrupts are enabled. When both master and slave functionality is enabled, the software needs to differentiate the source(s) of the interrupt.

Refer to Application Note AN554, *Software Implementation of I²C™ Bus Master* (DS00554) for more information.

17.2.9 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allow the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the SSP module is disabled. The Stop (P) and Start (S) bits will toggle based on the Start and Stop conditions. Control of the I²C bus may be taken when the P bit of the SSPSTAT register is set or when the bus is Idle, and both the S and P bits are clear. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the Stop condition occurs.

In Multi-Master operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and a low level is present, the device needs to release the SDA and SCL lines (set TRIS bits). There are two stages where this arbitration of the bus can be lost. They are the Address Transfer and Data Transfer stages.

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage, communication to the device may be in progress. If addressed, an ACK pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to re-transfer the data at a later time.

Refer to Application Note AN578, *Use of the SSP Module in the I²C™ Multi-Master Environment* (DS00578) for more information.

19.0 POWER-DOWN MODE (SLEEP)

The Power-down mode is entered by executing a `SLEEP` instruction.

If the Watchdog Timer is enabled:

- `WDT` will be cleared but keeps running.
- `PD` bit of the `STATUS` register is cleared.
- `TO` bit of the `STATUS` register is set.
- Oscillator driver is turned off.
- Timer1 oscillator is unaffected
- I/O ports maintain the status they had before `SLEEP` was executed (driving high, low or high-impedance).

For lowest current consumption in this mode, all I/O pins should be either at `VDD` or `VSS`, with no external circuitry drawing current from the I/O pin. I/O pins that are high-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The `T0CKI` input should also be at `VDD` or `VSS` for lowest current consumption. The contribution from on-chip pull-ups on `PORTB` should be considered.

The `MCLR` pin must be at a logic high level when external `MCLR` is enabled.

Note: A Reset generated by a `WDT` time out does not drive `MCLR` pin low.

19.1 Wake-up from Sleep

The device can wake up from Sleep through one of the following events:

1. External Reset input on `MCLR` pin.
2. Watchdog Timer wake-up (if `WDT` was enabled).
3. Interrupt from `RB0/INT` pin, `PORTB` change or a peripheral interrupt.

The first event will cause a device Reset. The two latter events are considered a continuation of program execution. The `TO` and `PD` bits in the `STATUS` register can be used to determine the cause of device Reset. The `PD` bit, which is set on power-up, is cleared when Sleep is invoked. `TO` bit is cleared if `WDT` wake-up occurred.

The following peripheral interrupts can wake the device from Sleep:

1. `TMR1` Interrupt. Timer1 must be operating as an asynchronous counter.
2. `USART` Receive Interrupt (Synchronous Slave mode only)
3. A/D conversion (when A/D clock source is `RC`)
4. Interrupt-on-change
5. External Interrupt from `INT` pin
6. Capture event on `CCP1` or `CCP2`
7. `SSP` Interrupt in `SPI` or `I2C` Slave mode

Other peripherals cannot generate interrupts since during Sleep, no on-chip clocks are present.

When the `SLEEP` instruction is being executed, the next instruction (`PC + 1`) is prefetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the `GIE` bit. If the `GIE` bit is clear (disabled), the device continues execution at the instruction after the `SLEEP` instruction. If the `GIE` bit is set (enabled), the device executes the instruction after the `SLEEP` instruction, then branches to the interrupt address (0004h). In cases where the execution of the instruction following `SLEEP` is not desirable, the user should have a `NOP` after the `SLEEP` instruction.

Note: If the global interrupts are disabled (`GIE` is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from Sleep. The `SLEEP` instruction is completely executed.

The `WDT` is cleared when the device wakes up from Sleep, regardless of the source of wake-up.

21.0 INSTRUCTION SET SUMMARY

The PIC16(L)F722/3/4/6/7 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 14-bit word divided into an **opcode**, which specifies the instruction type and one or more **operands**, which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 21-1, while the various opcode fields are summarized in Table 21-1.

Table 21-2 lists the instructions recognized by the MPASM™ assembler.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a nominal instruction execution time of 1 μs. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

21.1 Read-Modify-Write Operations

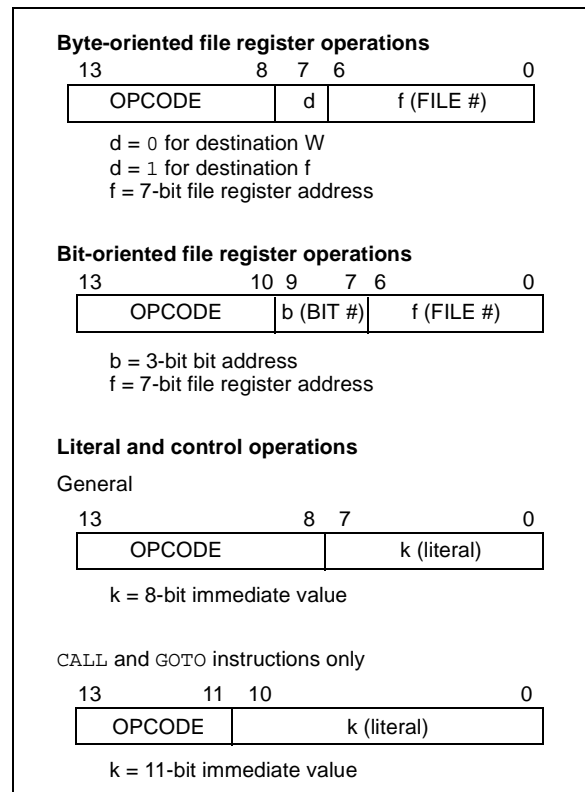
Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

For example, a `CLRF PORTB` instruction will read PORTB, clear all the data bits, then write the result back to PORTB. This example would have the unintended consequence of clearing the condition that set the RBIF flag.

TABLE 21-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
PC	Program Counter
TO	Time-out bit
C	Carry bit
DC	Digit carry bit
Z	Zero bit
PD	Power-down bit

FIGURE 21-1: GENERAL FORMAT FOR INSTRUCTIONS



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23.2 DC Characteristics: PIC16(L)F722/3/4/6/7-I/E (Industrial, Extended) (Continued)

PIC16LF722/3/4/6/7			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
PIC16F722/3/4/6/7			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
						VDD	Note
	Supply Current (IDD) ^(1, 2)						
D014		—	290	330	μA	1.8	Fosc = 4 MHz
		—	460	500	μA	3.0	EC Oscillator mode
D014		—	300	430	μA	1.8	Fosc = 4 MHz
		—	450	655	μA	3.0	EC Oscillator mode (Note 5)
		—	500	730	μA	5.0	
D015		—	100	130	μA	1.8	Fosc = 500 kHz
		—	120	150	μA	3.0	MFINTOSC mode
D015		—	115	195	μA	1.8	Fosc = 500 kHz
		—	135	200	μA	3.0	MFINTOSC mode (Note 5)
		—	150	220	μA	5.0	
D016		—	650	800	μA	1.8	Fosc = 8 MHz
		—	1000	1200	μA	3.0	HFINTOSC mode
D016		—	625	850	μA	1.8	Fosc = 8 MHz
		—	1000	1200	μA	3.0	HFINTOSC mode (Note 5)
		—	1100	1500	μA	5.0	
D017		—	1.0	1.2	mA	1.8	Fosc = 16 MHz
		—	1.5	1.85	mA	3.0	HFINTOSC mode
D017		—	1	1.2	mA	1.8	Fosc = 16 MHz
		—	1.5	1.7	mA	3.0	HFINTOSC mode (Note 5)
		—	1.7	2.1	mA	5.0	
D018		—	210	240	μA	1.8	Fosc = 4 MHz
		—	340	380	μA	3.0	EXTRC mode (Note 3, Note 5)
D018		—	225	320	μA	1.8	Fosc = 4 MHz
		—	360	445	μA	3.0	EXTRC mode (Note 3, Note 5)
		—	410	650	μA	5.0	
D019		—	1.6	1.9	mA	3.0	Fosc = 20 MHz
		—	2.0	2.8	mA	3.6	HS Oscillator mode
D019		—	1.6	2	mA	3.0	Fosc = 20 MHz
		—	1.9	3.2	mA	5.0	HS Oscillator mode (Note 5)

- Note** 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.
- 2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.
- 3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula $I_R = V_{DD}/2R_{EXT}$ (mA) with REXT in kΩ.
- 4: FVR and BOR are disabled.
- 5: 0.1 μF capacitor on VCAP (RA0).

TABLE 23-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET PARAMETERS

Standard Operating Conditions (unless otherwise stated) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$							
Param No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
30	TMCL	MCLR Pulse Width (low)	2 5	— —	— —	μs μs	$V_{DD} = 3.3\text{-}5\text{V}$, -40°C to $+85^{\circ}\text{C}$ $V_{DD} = 3.3\text{-}5\text{V}$
31	TWDTLP	Low Power Watchdog Timer Time-out Period (No Prescaler)	10	18	27	ms	$V_{DD} = 3.3\text{V}\text{-}5\text{V}$
32	TOST	Oscillator Start-up Timer Period ^{(1), (2)}	—	1024	—	Tosc	(Note 3)
33*	TPWRT	Power-up Timer Period, PWRTE = 0	40	65	140	ms	
34*	TIOZ	I/O high-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.0	μs	
35	VBOR	Brown-out Reset Voltage	2.38 1.80	2.5 1.9	2.73 2.11	V	BORV=2.5V BORV=1.9V
36*	VHYS	Brown-out Reset Hysteresis	0	25	50	mV	-40°C to $+85^{\circ}\text{C}$
37*	TBORDC	Brown-out Reset DC Response Time	1	3	5 10	μs	$V_{DD} \leq V_{BOR}$, -40°C to $+85^{\circ}\text{C}$ $V_{DD} \leq V_{BOR}$

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

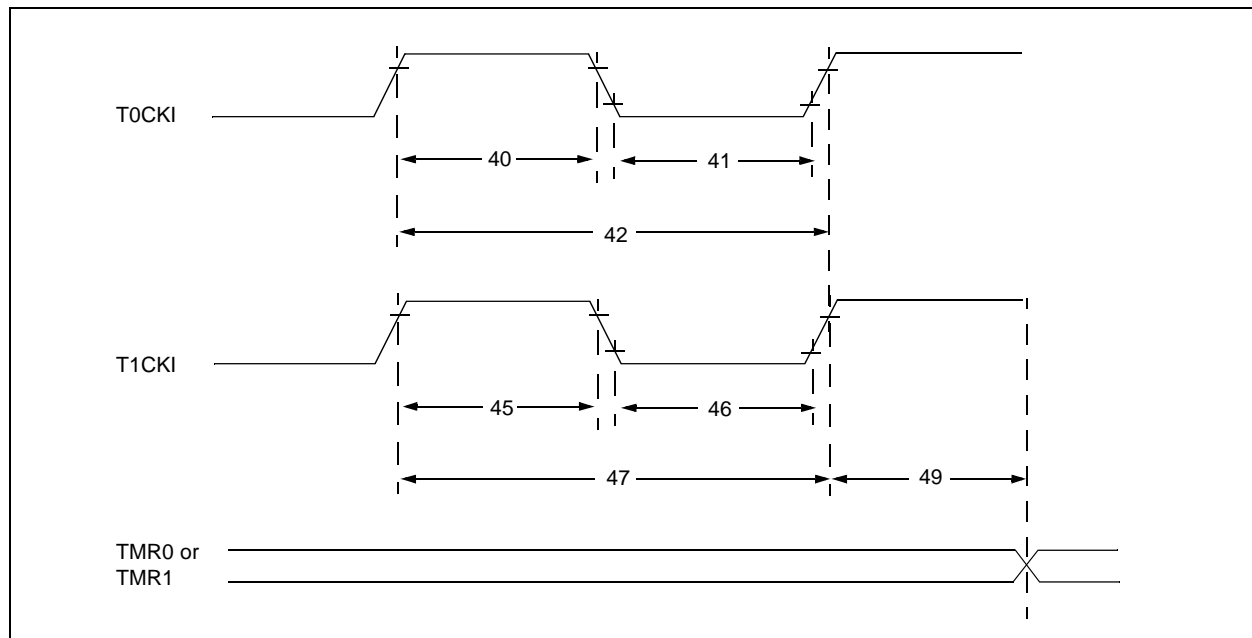
Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: By design.

3: Period of the slower clock.

4: To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

FIGURE 23-10: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS



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FIGURE 24-9: PIC16F722/3/4/6/7 MAXIMUM I_{DD} vs. F_{OSC} OVER V_{DD} , HS MODE, $V_{CAP} = 0.1 \mu F$

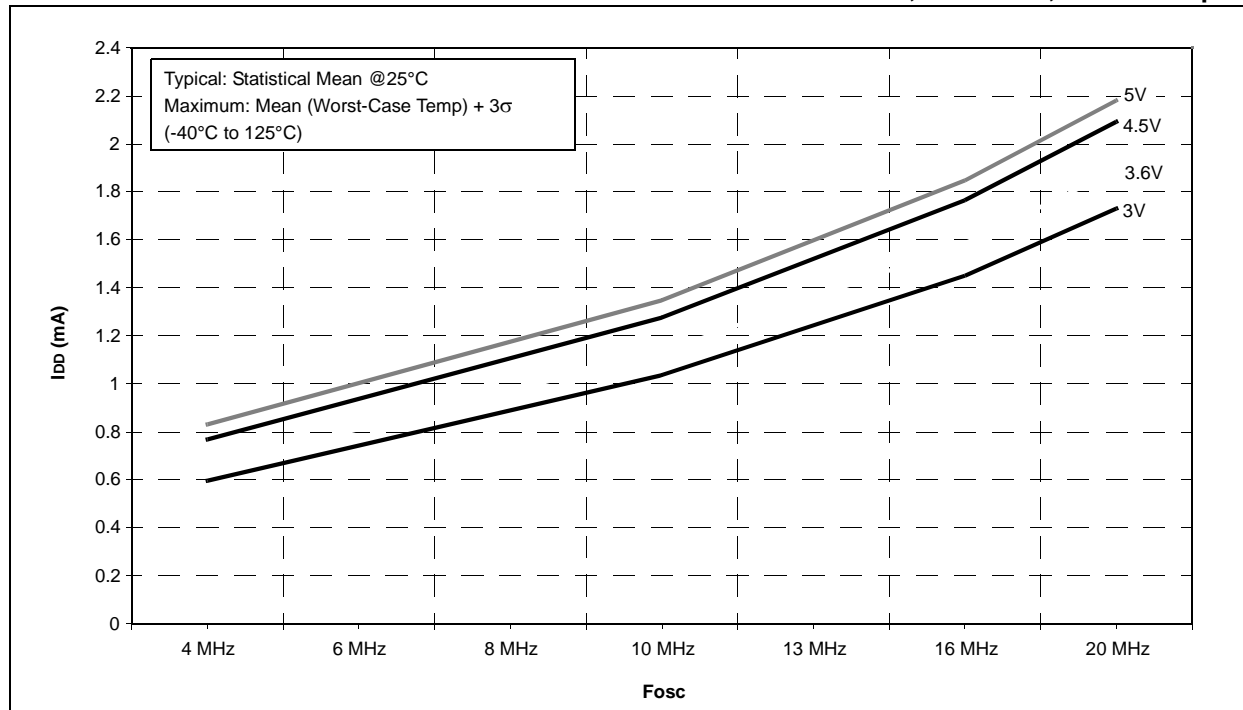
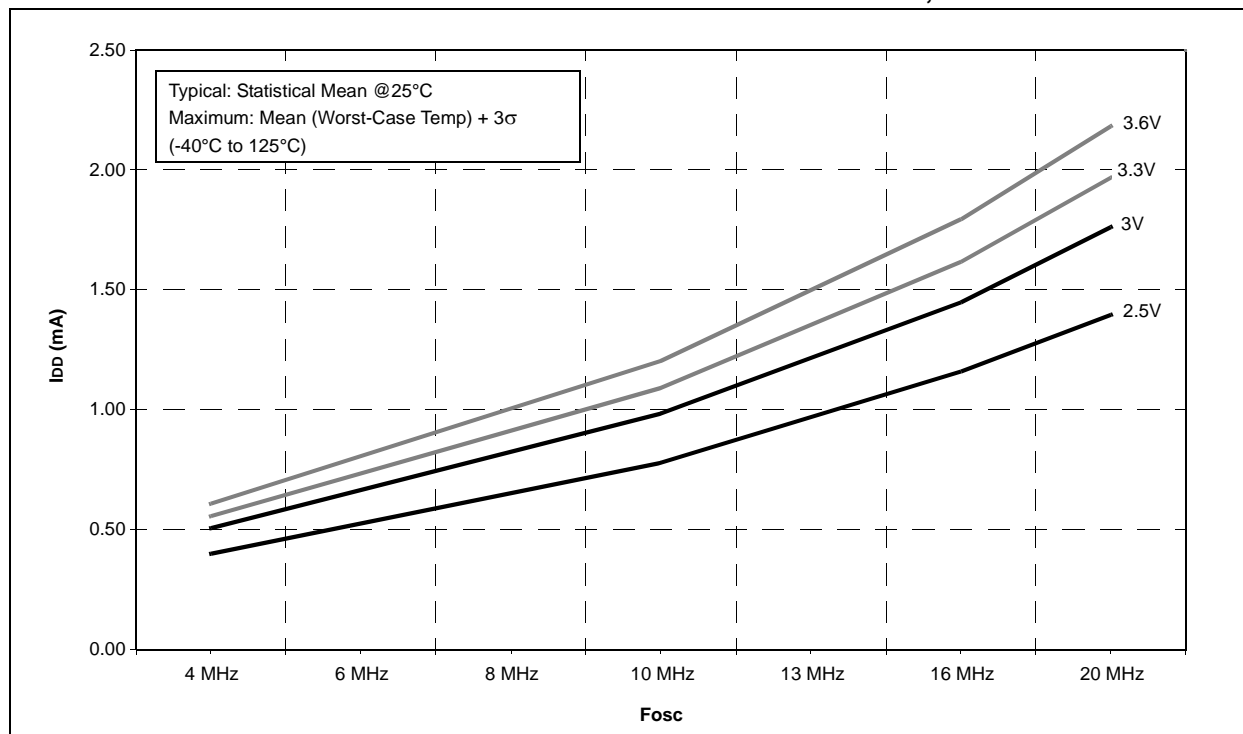
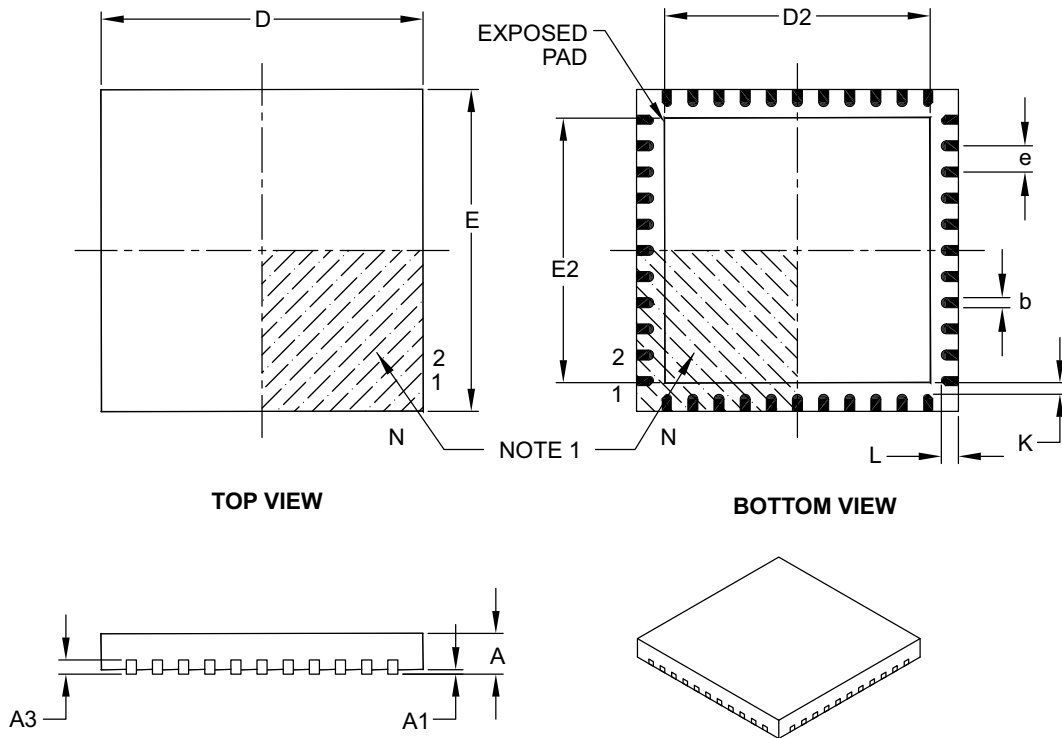


FIGURE 24-10: PIC16LF722/3/4/6/7 MAXIMUM I_{DD} vs. F_{OSC} OVER V_{DD} , HS MODE



44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	44		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	8.00 BSC		
Exposed Pad Width	E2	6.30	6.45	6.80
Overall Length	D	8.00 BSC		
Exposed Pad Length	D2	6.30	6.45	6.80
Contact Width	b	0.25	0.30	0.38
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103B