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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf727-e-ml

PIC16(L)F722/3/4/6/7

TABLE 2-1: PIC16(L)F722/3/4/6/7 SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Page
Bank 2											
100h ⁽²⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	29,37
101h	TMR0	Timer0 Module Register								xxxx xxxx	105,37
102h ⁽²⁾	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	28,37
103h ⁽²⁾	STATUS	IRP	RP1	RP0	\overline{TO}	\overline{PD}	Z	DC	C	0001 1xxx	25,37
104h ⁽²⁾	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	29,37
105h	—	Unimplemented								—	—
106h	—	Unimplemented								—	—
107h	—	Unimplemented								—	—
108h	CPSCON0	CPSON	—	—	—	CPSRNG1	CPSRNG0	CPSOUT	T0XCS	0--- 0000	126,38
109h	CPSCON1	—	—	—	—	CPSCH3	CPSCH2	CPSCH1	CPSCH0	---- 0000	127,38
10Ah ^(1, 2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	28,37
10Bh ⁽²⁾	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	44,37
10Ch	PMDATL	Program Memory Read Data Register Low Byte								xxxx xxxx	181,38
10Dh	PMADRL	Program Memory Read Address Register Low Byte								xxxx xxxx	181,38
10Eh	PMDATH	—	—	Program Memory Read Data Register High Byte					--xx xxxx	181,38	
10Fh	PMADRH	—	—	—	Program Memory Read Address Register High Byte					---x xxxx	181,38
Bank 3											
180h ⁽²⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	29,37
181h	OPTION_REG	\overline{RBPV}	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	26,37
182h ⁽²⁾	PCL	Program Counter (PC) Least Significant Byte								0000 0000	28,37
183h ⁽²⁾	STATUS	IRP	RP1	RP0	\overline{TO}	\overline{PD}	Z	DC	C	0001 1xxx	25,37
184h ⁽²⁾	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	29,37
185h	ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	--11 1111	52,38
186h	ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	--11 1111	61,38
187h	—	Unimplemented								—	—
188h	ANSELD	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	78,38
189h ⁽³⁾	ANSELE	—	—	—	—	—	ANSE2	ANSE1	ANSE0	---- -111	82,38
18Ah ^(1, 2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	28,37
18Bh ⁽²⁾	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	44,37
18Ch	PMCON1	Reserved	—	—	—	—	—	—	RD	1--- ---0	182,38
18Dh	—	Unimplemented								—	—
18Eh	—	Unimplemented								—	—
18Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

- Note 1:** The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter.
- 2:** These registers can be addressed from any bank.
- 3:** These registers/bits are not implemented on PIC16F722/723/726/PIC16LF722/723/726 devices, read as '0'.
- 4:** Accessible only when SSPM<3:0> = 1001.
- 5:** Accessible only when SSPM<3:0> ≠ 1001.
- 6:** This bit is always '1' as RE3 is input-only.

PIC16(L)F722/3/4/6/7

3.0 RESETS

The PIC16(L)F722/3/4/6/7 differentiates between various kinds of Reset:

- Power-on Reset (POR)
- WDT Reset during normal operation
- WDT Reset during Sleep
- $\overline{\text{MCLR}}$ Reset during normal operation
- $\overline{\text{MCLR}}$ Reset during Sleep
- Brown-out Reset (BOR)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on:

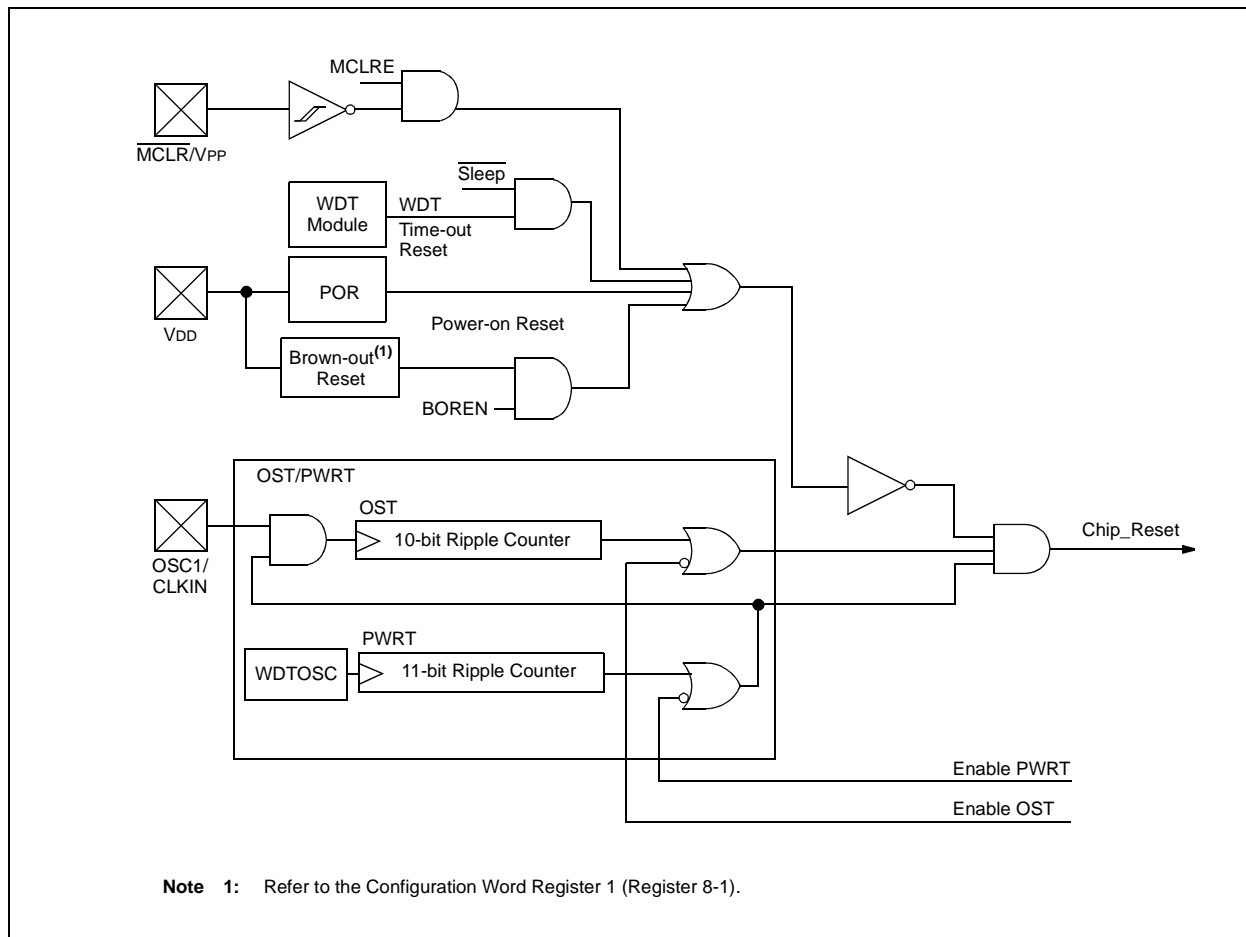
- Power-on Reset (POR)
- $\overline{\text{MCLR}}$ Reset
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Reset
- Brown-out Reset (BOR)

Most registers are not affected by a WDT wake-up since this is viewed as the resumption of normal operation. $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different Reset situations, as indicated in Table 3-3. These bits are used in software to determine the nature of the Reset.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 3-1.

The $\overline{\text{MCLR}}$ Reset path has a noise filter to detect and ignore small pulses. See **Section 23.0 "Electrical Specifications"** for pulse-width specifications.

FIGURE 3-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



5.0 LOW DROPOUT (LDO) VOLTAGE REGULATOR

The PIC16F722/3/4/6/7 devices differ from the PIC16LF722/3/4/6/7 devices due to an internal Low Dropout (LDO) voltage regulator. The PIC16F722/3/4/6/7 devices contain an internal LDO, while the PIC16LF722/3/4/6/7 ones do not.

The lithography of the die allows a maximum operating voltage of 3.6V on the internal digital logic. In order to continue to support 5.0V designs, a LDO voltage regulator is integrated on the die. The LDO voltage regulator allows for the internal digital logic to operate at 3.2V, while I/O's operate at 5.0V (V_{DD}).

The LDO voltage regulator requires an external bypass capacitor for stability. One of three pins, denoted as VCAP, can be configured for the external bypass capacitor. It is recommended that the capacitor be a ceramic cap between 0.1 to 1.0 μ F. The VCAP pin is not intended to supply power to external loads. An external voltage regulator should be used if this functionality is required. In addition, external devices should not supply power to the VCAP pin.

On power-up, the external capacitor will look like a large load on the LDO voltage regulator. To prevent erroneous operation, the device is held in Reset while a constant current source charges the external capacitor. After the cap is fully charged, the device is released from Reset. For more information, refer to **Section 23.0 "Electrical Specifications"**.

See Configuration Word 2 register (Register 8-2) for VCAP enable bits.

FIGURE 6-2: RA<3:1> BLOCK DIAGRAM

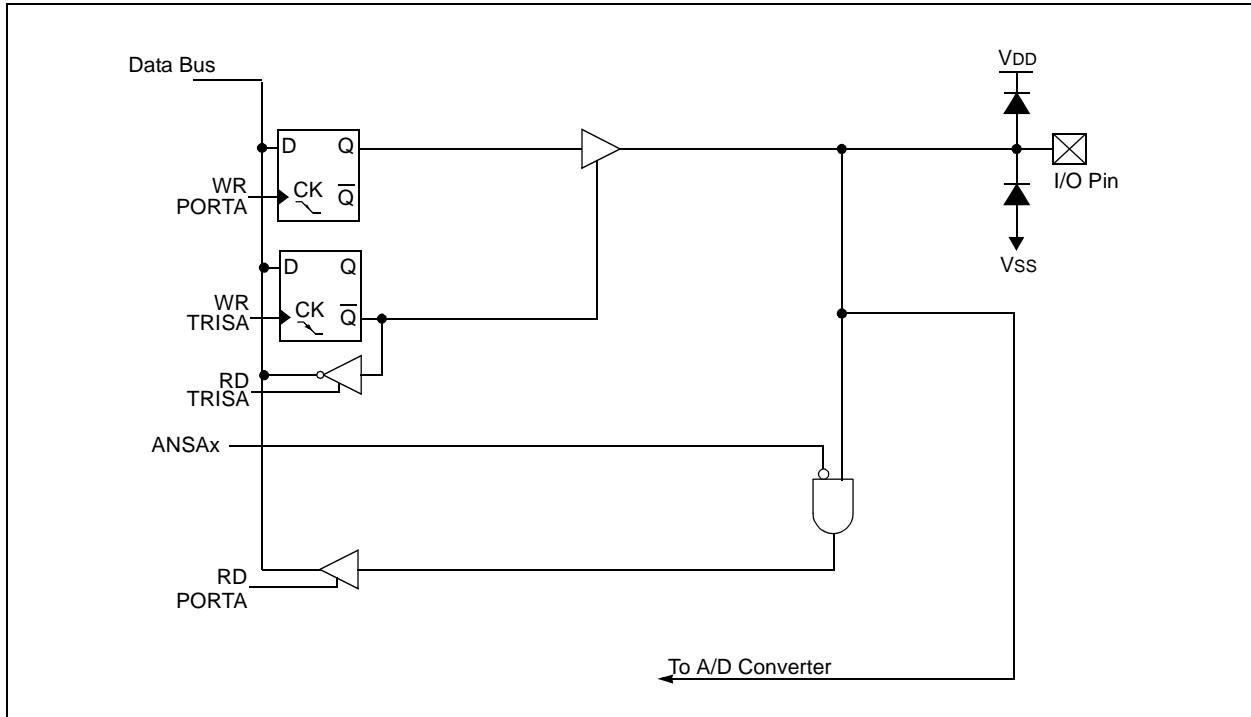
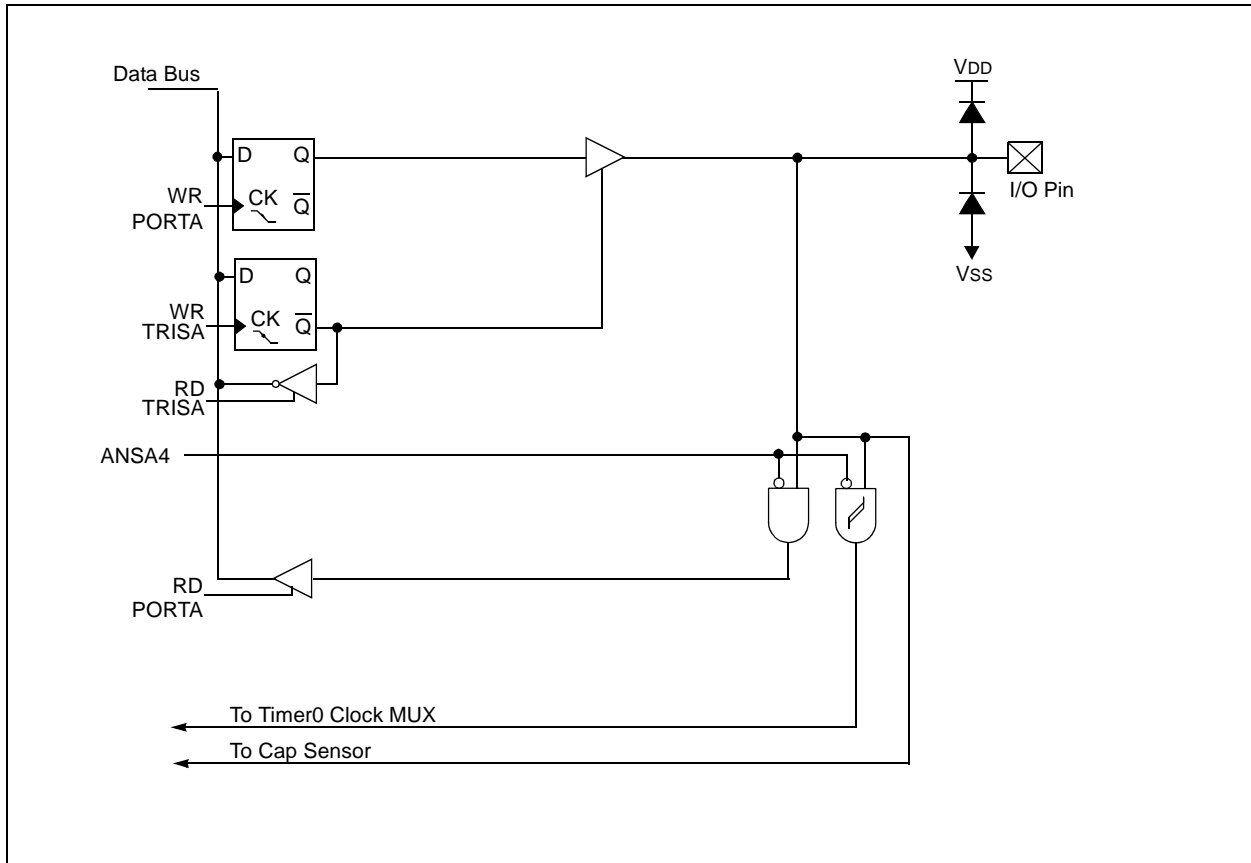
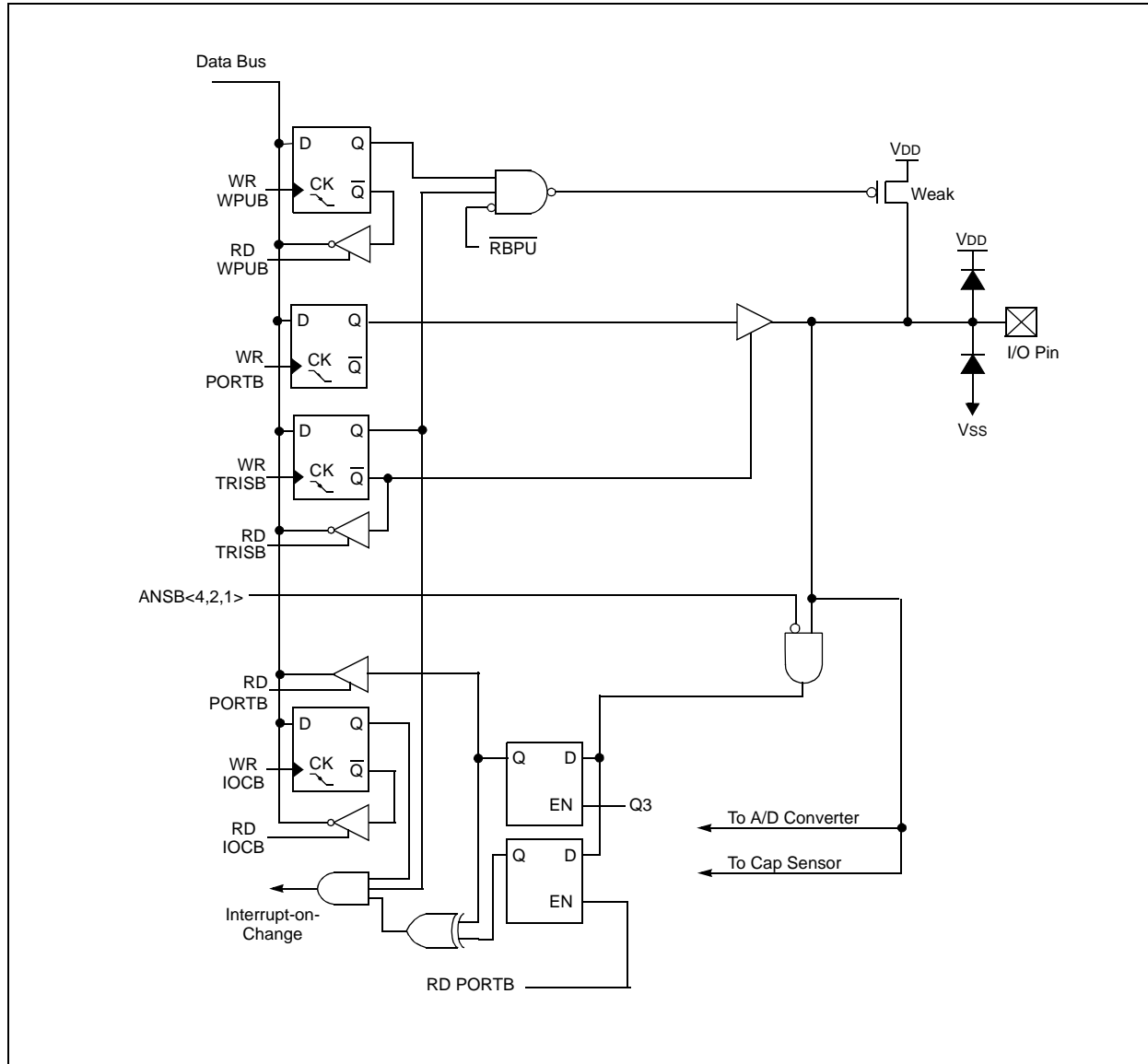


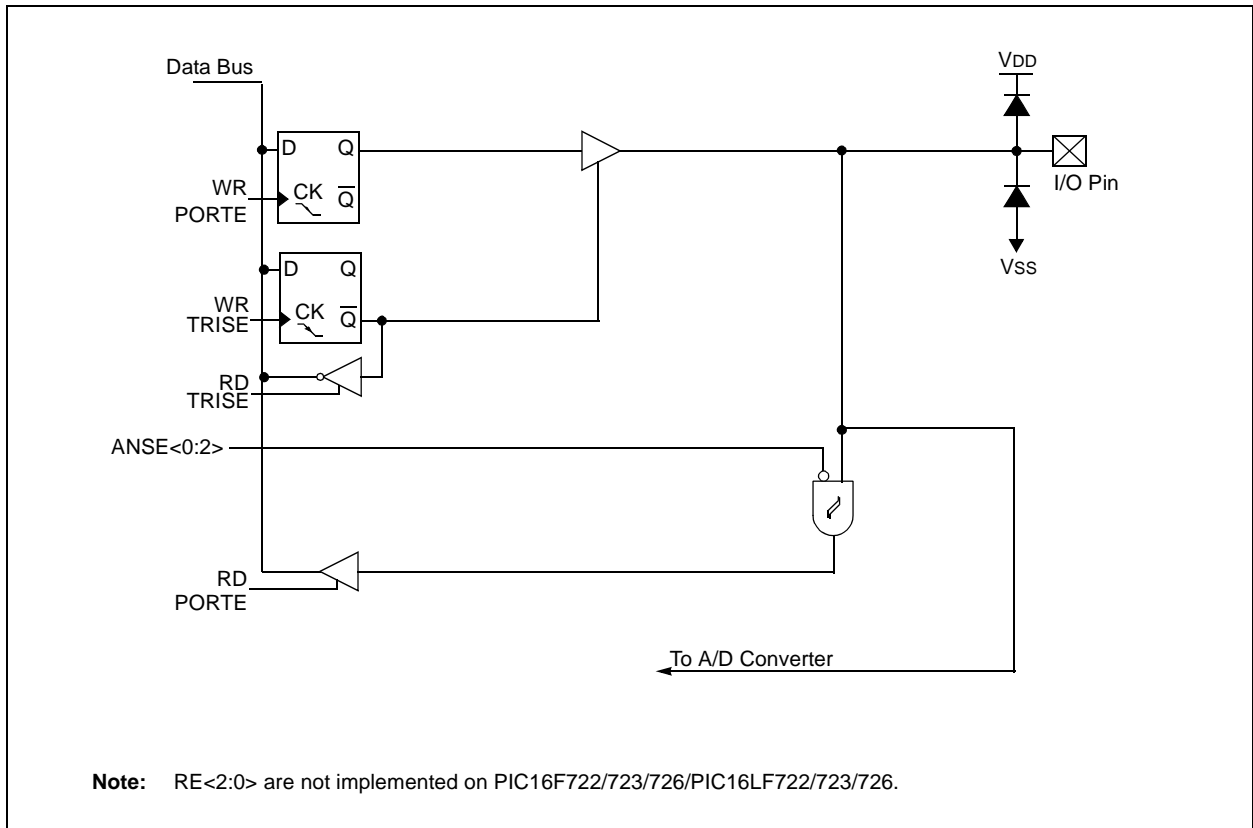
FIGURE 6-3: BLOCK DIAGRAM OF RA4



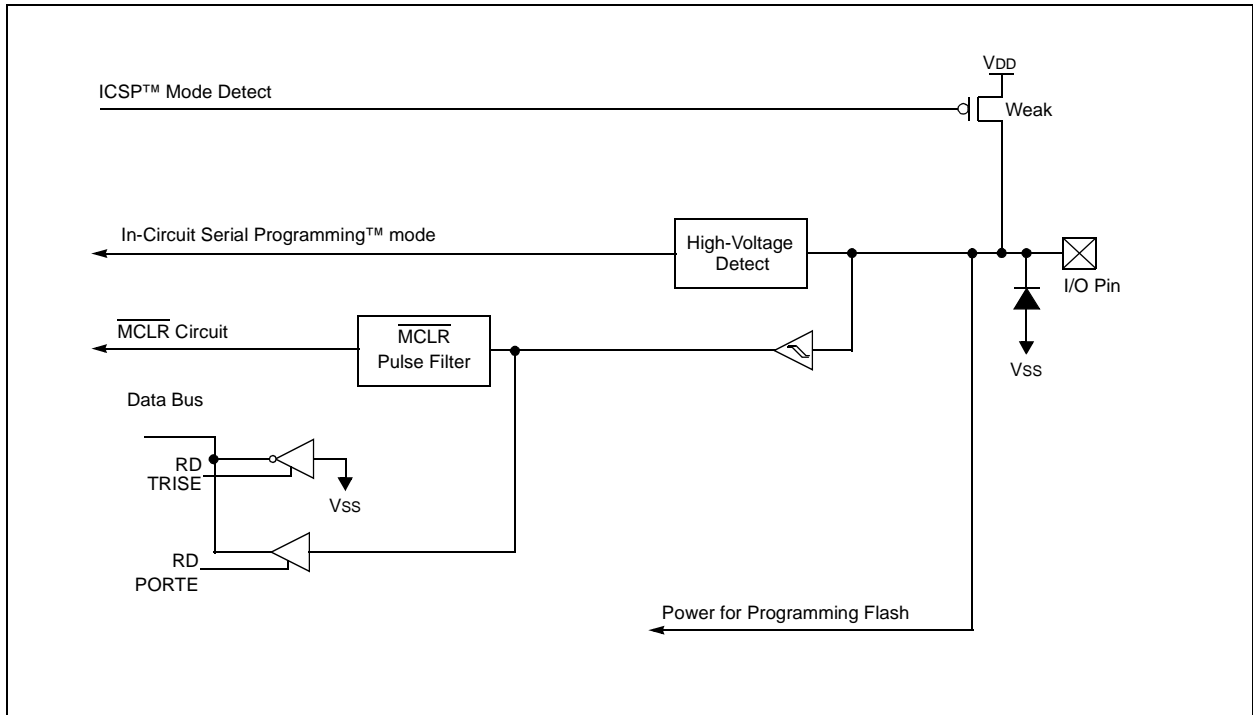
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FIGURE 6-8: BLOCK DIAGRAM OF RB4, RB<2:1>





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11.0 TIMER0 MODULE

The Timer0 module is an 8-bit timer/counter with the following features:

- 8-bit timer/counter register (TMR0)
- 8-bit prescaler (shared with Watchdog Timer)
- Programmable internal or external clock source
- Programmable external clock edge selection
- Interrupt on overflow
- TMR0 can be used to gate Timer1

Figure 11-1 is a block diagram of the Timer0 module.

11.1 Timer0 Operation

The Timer0 module can be used as either an 8-bit timer or an 8-bit counter.

11.1.1 8-BIT TIMER MODE

The Timer0 module will increment every instruction cycle, if used without a prescaler. 8-Bit Timer mode is selected by clearing the T0CS bit of the OPTION register.

When TMR0 is written, the increment is inhibited for two instruction cycles immediately following the write.

Note: The value written to the TMR0 register can be adjusted, in order to account for the two instruction cycle delay when TMR0 is written.

11.1.2 8-BIT COUNTER MODE

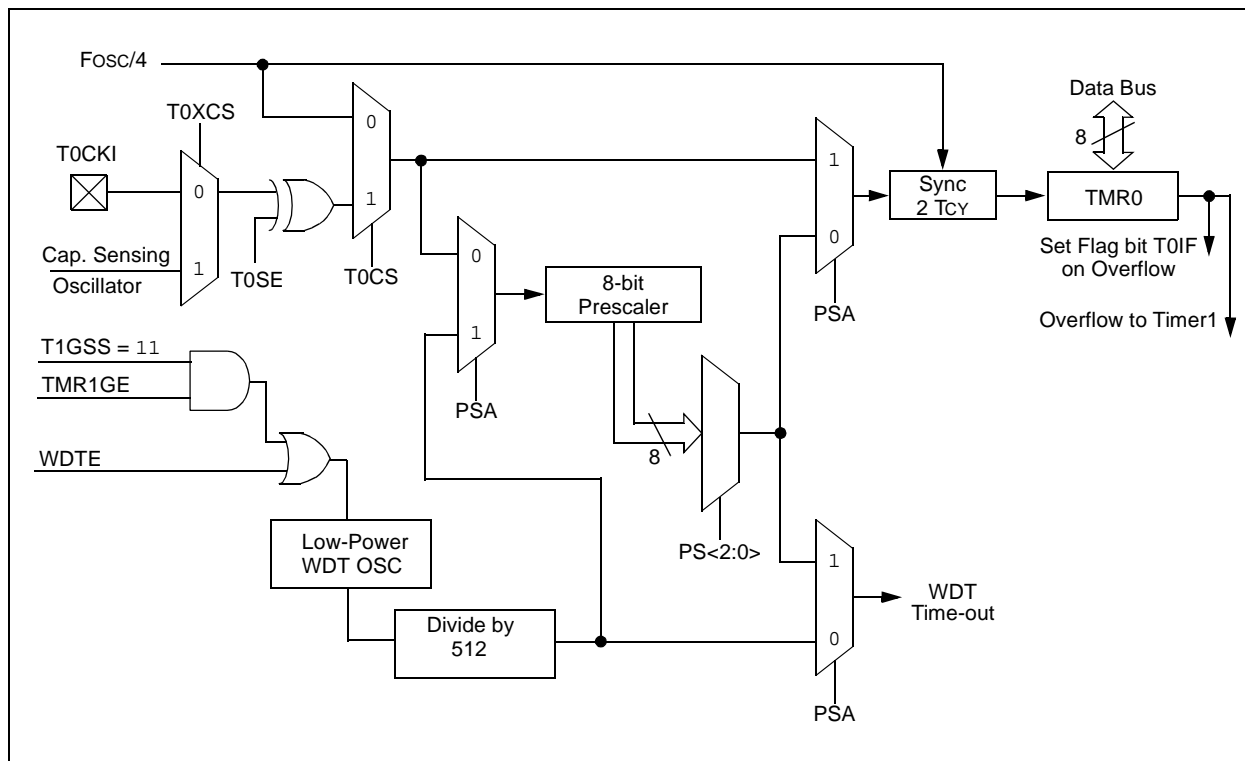
In 8-Bit Counter mode, the Timer0 module will increment on every rising or falling edge of the T0CKI pin or the Capacitive Sensing Oscillator (CPSOSC) signal.

8-Bit Counter mode using the T0CKI pin is selected by setting the T0CS bit in the OPTION register to '1' and resetting the T0XCS bit in the CPSCON0 register to '0'.

8-Bit Counter mode using the Capacitive Sensing Oscillator (CPSOSC) signal is selected by setting the T0CS bit in the OPTION register to '1' and setting the T0XCS bit in the CPSCON0 register to '1'.

The rising or falling transition of the incrementing edge for either input source is determined by the T0SE bit in the OPTION register.

FIGURE 11-1: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



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11.1.3 SOFTWARE PROGRAMMABLE PRESCALER

A single software programmable prescaler is available for use with either Timer0 or the Watchdog Timer (WDT), but not both simultaneously. The prescaler assignment is controlled by the PSA bit of the OPTION register. To assign the prescaler to Timer0, the PSA bit must be cleared to a '0'.

There are eight prescaler options for the Timer0 module ranging from 1:2 to 1:256. The prescale values are selectable via the PS<2:0> bits of the OPTION register. In order to have a 1:1 prescaler value for the Timer0 module, the prescaler must be assigned to the WDT module.

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register will clear the prescaler.

Note: When the prescaler is assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT.

11.1.4 TIMER0 INTERRUPT

Timer0 will generate an interrupt when the TMR0 register overflows from FFh to 00h. The T0IF interrupt flag bit of the INTCON register is set every time the TMR0 register overflows, regardless of whether or not the Timer0 interrupt is enabled. The T0IF bit can only be cleared in software. The Timer0 interrupt enable is the T0IE bit of the INTCON register.

Note: The Timer0 interrupt cannot wake the processor from Sleep since the timer is frozen during Sleep.
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11.1.5 8-BIT COUNTER MODE SYNCHRONIZATION

When in 8-Bit Counter mode, the incrementing edge on the T0CKI pin must be synchronized to the instruction clock. Synchronization can be accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the instruction clock. The high and low periods of the external clocking source must meet the timing requirements as shown in **Section 23.0 “Electrical Specifications”**.

15.3 PWM Mode

The PWM mode generates a Pulse-Width Modulated signal on the CCPx pin. The duty cycle, period and resolution are determined by the following registers:

- PR2
- T2CON
- CCPRxL
- CCPxCON

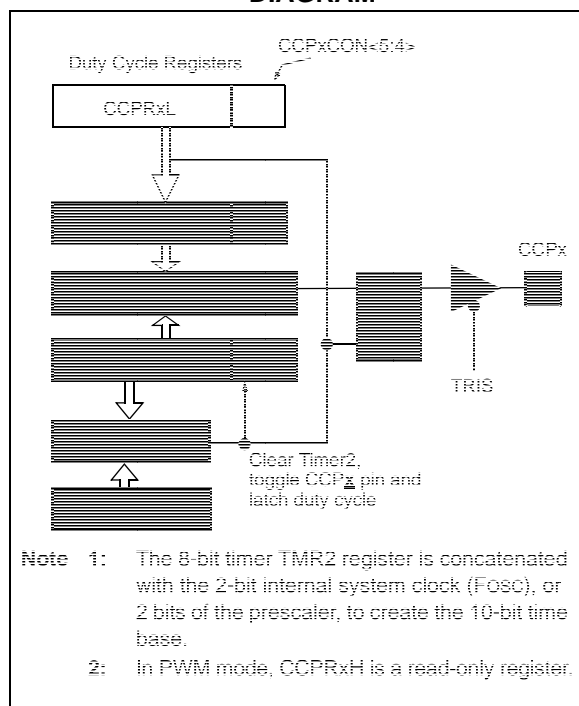
In Pulse-Width Modulation (PWM) mode, the CCP module produces up to a 10-bit resolution PWM output on the CCPx pin.

Figure 15-3 shows a simplified block diagram of PWM operation.

Figure 15-4 shows a typical waveform of the PWM signal.

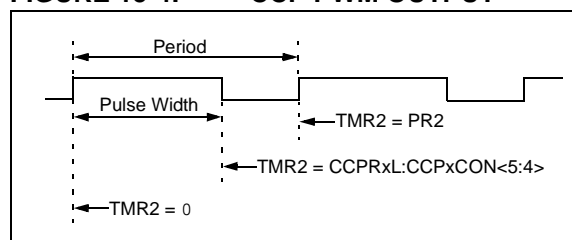
For a step-by-step procedure on how to set up the CCP module for PWM operation, refer to **Section 15.3.8 “Setup for PWM Operation”**.

FIGURE 15-3: SIMPLIFIED PWM BLOCK DIAGRAM



The PWM output (Figure 15-4) has a time base (period) and a time that the output stays high (duty cycle).

FIGURE 15-4: CCP PWM OUTPUT



15.3.1 CCPx PIN CONFIGURATION

In PWM mode, the CCPx pin is multiplexed with the PORT data latch. The user must configure the CCPx pin as an output by clearing the associated TRIS bit.

Either RC1 or RB3 can be selected as the CCP2 pin. Refer to **Section 6.1 “Alternate Pin Function”** for more information.

Note: Clearing the CCPxCON register will relinquish CCPx control of the CCPx pin.

16.4 AUSART Operation During Sleep

The AUSART will remain active during Sleep only in the Synchronous Slave mode. All other modes require the system clock and therefore cannot generate the necessary signals to run the Transmit or Receive Shift registers during Sleep.

Synchronous Slave mode uses an externally generated clock to run the Transmit and Receive Shift registers.

16.4.1 SYNCHRONOUS RECEIVE DURING SLEEP

To receive during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for Synchronous Slave Reception (refer to **Section 16.3.2.4 “Synchronous Slave Reception Setup:”**).
- If interrupts are desired, set the RCIE bit of the PIE1 register and the PEIE bit of the INTCON register.
- The RCIF interrupt flag must be cleared by reading RCREG to unload any pending characters in the receive buffer.

Upon entering Sleep mode, the device will be ready to accept data and clocks on the RX/DT and TX/CK pins, respectively. When the data word has been completely clocked in by the external device, the RCIF interrupt flag bit of the PIR1 register will be set. Thereby, waking the processor from Sleep.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the GIE global interrupt enable bit of the INTCON register is also set, then the Interrupt Service Routine at address 0004h will be called.

16.4.2 SYNCHRONOUS TRANSMIT DURING SLEEP

To transmit during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for Synchronous Slave Transmission (refer to **Section 16.3.2.2 “Synchronous Slave Transmission Setup:”**).
- The TXIF interrupt flag must be cleared by writing the output data to the TXREG, thereby filling the TSR and transmit buffer.
- If interrupts are desired, set the TXIE bit of the PIE1 register and the PEIE bit of the INTCON register.

Upon entering Sleep mode, the device will be ready to accept clocks on TX/CK pin and transmit data on the RX/DT pin. When the data word in the TSR has been completely clocked out by the external device, the pending byte in the TXREG will transfer to the TSR and the TXIF flag will be set. Thereby, waking the processor from Sleep. At this point, the TXREG is available to accept another character for transmission, which will clear the TXIF flag.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the GIE global interrupt enable bit is also set then the Interrupt Service Routine at address 0004h will be called.

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REGISTER 17-1: SSPCON: SYNC SERIAL PORT CONTROL REGISTER (SPI MODE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **WCOL**: Write Collision Detect bit
1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision
- bit 6 **SSPOV**: Receive Overflow Indicator bit
1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in Slave mode. The user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register.
0 = No overflow
- bit 5 **SSPEN**: Synchronous Serial Port Enable bit
1 = Enables serial port and configures SCK, SDO and SDI as serial port pins⁽¹⁾
0 = Disables serial port and configures these pins as I/O port pins
- bit 4 **CKP**: Clock Polarity Select bit
1 = Idle state for clock is a high level
0 = Idle state for clock is a low level
- bit 3-0 **SSPM<3:0>**: Synchronous Serial Port Mode Select bits
0000 = SPI Master mode, clock = Fosc/4
0001 = SPI Master mode, clock = Fosc/16
0010 = SPI Master mode, clock = Fosc/64
0011 = SPI Master mode, clock = TMR2 output/2
0100 = SPI Slave mode, clock = SCK pin. \overline{SS} pin control enabled.
0101 = SPI Slave mode, clock = SCK pin. \overline{SS} pin control disabled. \overline{SS} can be used as I/O pin.

Note 1: When enabled, these pins must be properly configured as input or output.

17.2 I²C Mode

The SSP module, in I²C mode, implements all slave functions, except general call support. It provides interrupts on Start and Stop bits in hardware to facilitate firmware implementations of the master functions. The SSP module implements the I²C Standard mode specifications:

- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- Start and Stop bit interrupts enabled to support firmware Master mode
- Address masking

Two pins are used for data transfer; the SCL pin (clock line) and the SDA pin (data line). The user must configure the two pin's data direction bits as inputs in the appropriate TRIS register. Upon enabling I²C mode, the I²C slew rate limiters in the I/O pads are controlled by the SMP bit of SSPSTAT register. The SSP module functions are enabled by setting the SSPEN bit of SSPCON register.

Data is sampled on the rising edge and shifted out on the falling edge of the clock. This ensures that the SDA signal is valid during the SCL high time. The SCL clock input must have minimum high and low times for proper operation. Refer to **Section 23.0 "Electrical Specifications"**.

FIGURE 17-7: I²C MODE BLOCK DIAGRAM

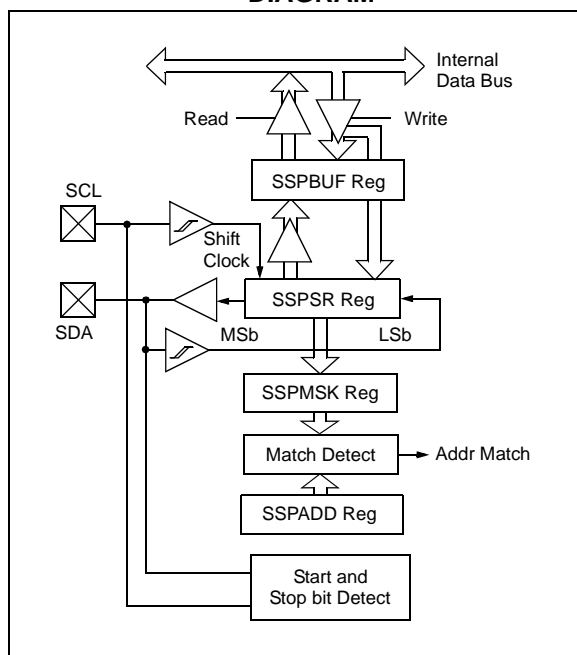
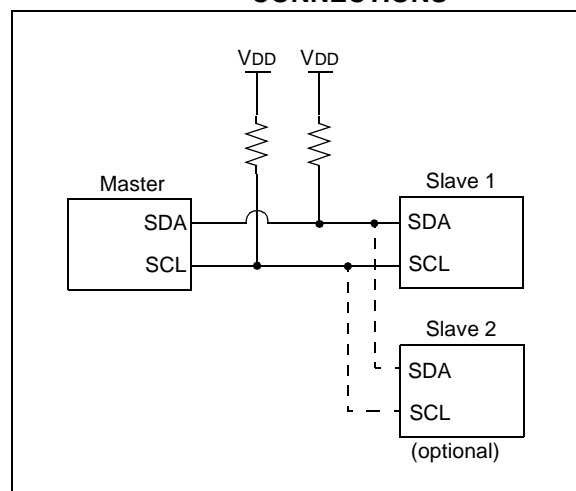


FIGURE 17-8: TYPICAL I²C CONNECTIONS



The SSP module has six registers for I²C operation. They are:

- SSP Control (SSPCON) register
- SSP Status (SSPSTAT) register
- Serial Receive/Transmit Buffer (SSPBUF) register
- SSP Shift Register (SSPSR), not directly accessible
- SSP Address (SSPADD) register
- SSP Address Mask (SSPMSK) register

17.2.1 HARDWARE SETUP

Selection of I²C mode, with the SSPEN bit of the SSPCON register set, forces the SCL and SDA pins to be open drain, provided these pins are programmed as inputs by setting the appropriate TRISC bits. The SSP module will override the input state with the output data, when required, such as for Acknowledge and slave-transmitter sequences.

Note: Pull-up resistors must be provided externally to the SCL and SDA pins for proper operation of the I²C module

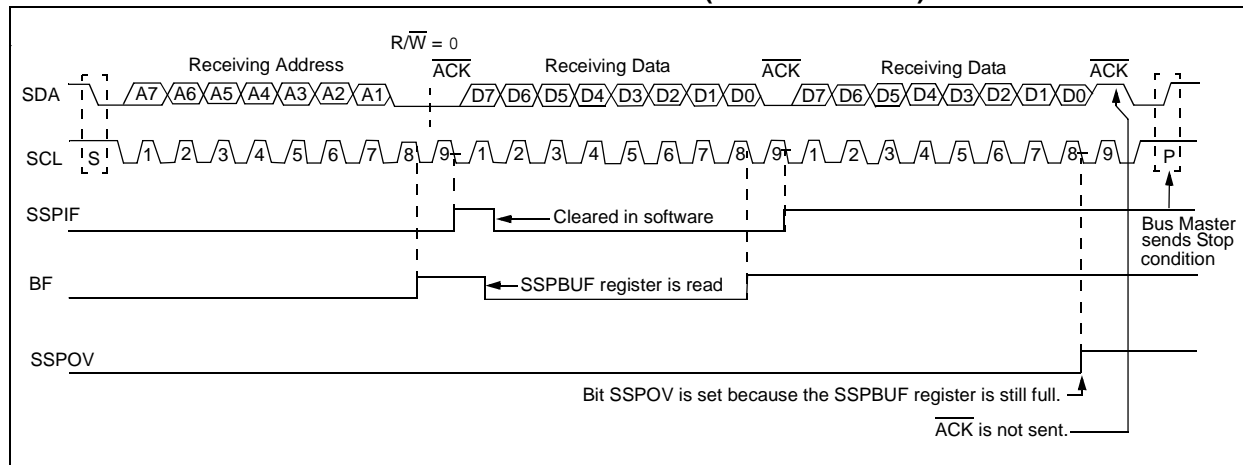
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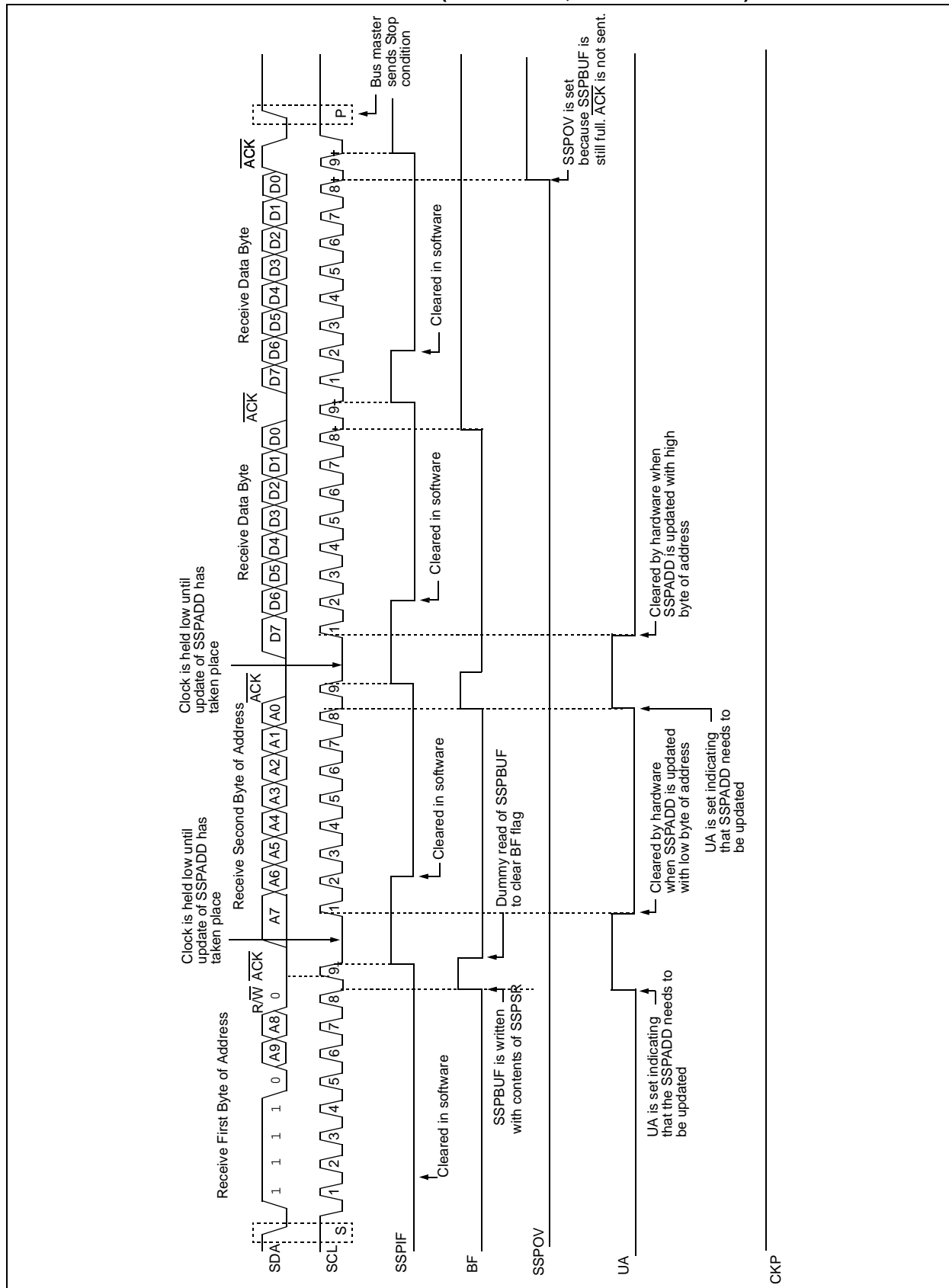
17.2.5 RECEPTION

When the R/\overline{W} bit of the received address byte is clear, the master will write data to the slave. If an address match occurs, the received address is loaded into the SSPBUF register. An address byte overflow will occur if that loaded address is not read from the SSPBUF before the next complete byte is received.

An SSP interrupt is generated for each data transfer byte. The BF, R/W and D/A bits of the SSPSTAT register are used to determine the status of the last received byte.

FIGURE 17-10: I²C WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)





RETFIE	Return from Interrupt
Syntax:	[<i>label</i>] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a 2-cycle instruction.
Words:	1
Cycles:	2
<u>Example:</u>	<pre>RETFIE</pre> <p>After Interrupt</p> <pre>PC = TOS GIE = 1</pre>

RETLW	Return with literal in W
Syntax:	[<i>label</i>] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the 8-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.
Words:	1
Cycles:	2
<u>Example:</u>	<pre>CALL TABLE;W contains table ;offset value • ;W now has table value • • ADDWF PC ;W = offset RETLW k1 ;Begin table RETLW k2 ; • • • RETLW kn ; End of table</pre> <p>Before Instruction W = 0x07</p> <p>After Instruction W = value of k8</p>

RETURN	Return from Subroutine
Syntax:	[<i>label</i>] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a 2-cycle instruction.

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RLF Rotate Left f through Carry

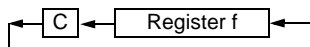
Syntax: [*label*] RLF *f*,*d*

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example: RLF REG1,0

Before Instruction

REG1 = 1110 0110
C = 0

After Instruction

REG1 = 1110 0110
W = 1100 1100
C = 1

SLEEP Enter Sleep mode

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → \overline{TO} ,
0 → \overline{PD}

Status Affected: \overline{TO} , \overline{PD}

Description: The power-down Status bit, \overline{PD} is cleared. Time-out Status bit, \overline{TO} is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

RRF Rotate Right f through Carry

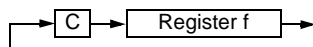
Syntax: [*label*] RRF *f*,*d*

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



SUBLW Subtract W from literal

Syntax: [*label*] SUBLW *k*

Operands: $0 \leq k \leq 255$

Operation: $k - (W) \rightarrow (W)$

Status Affected: C, DC, Z

Description: The W register is subtracted (2's complement method) from the 8-bit literal 'k'. The result is placed in the W register.

C = 0	$W > k$
C = 1	$W \leq k$
DC = 0	$W<3:0> > k<3:0>$
DC = 1	$W<3:0> \leq k<3:0>$

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FIGURE 23-5: PIC16LF722/3/4/6/7 VOLTAGE FREQUENCY GRAPH, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$

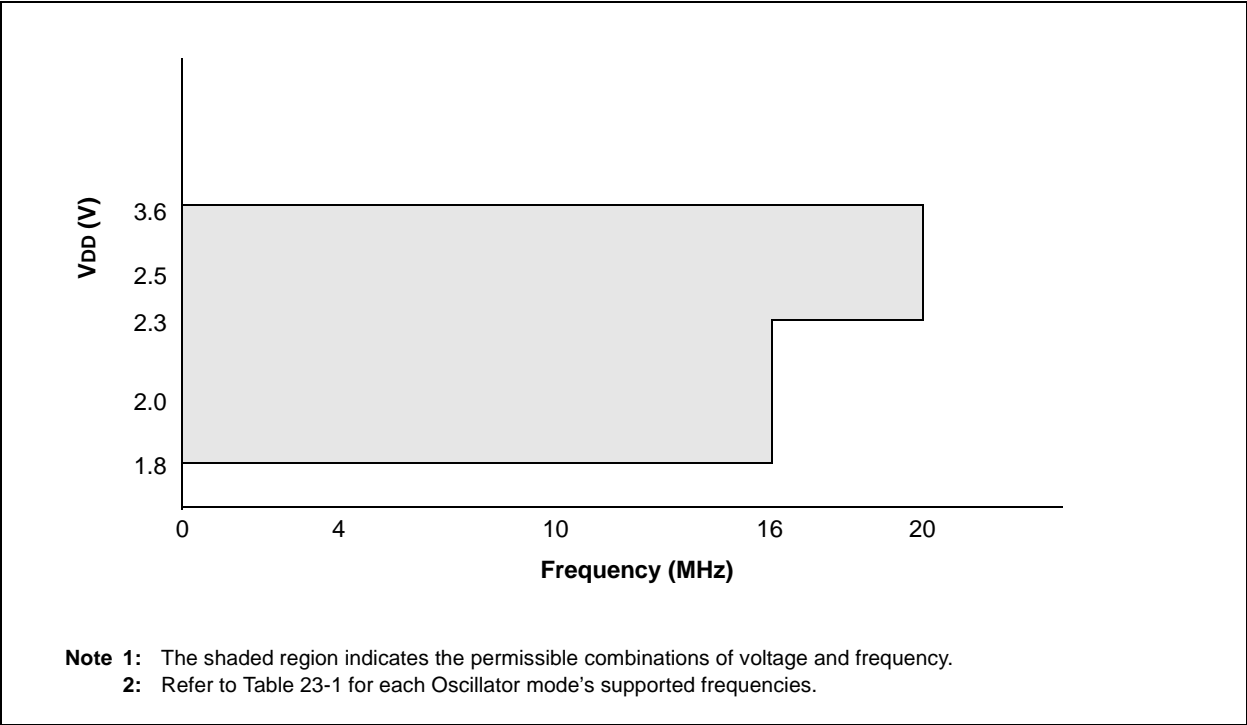
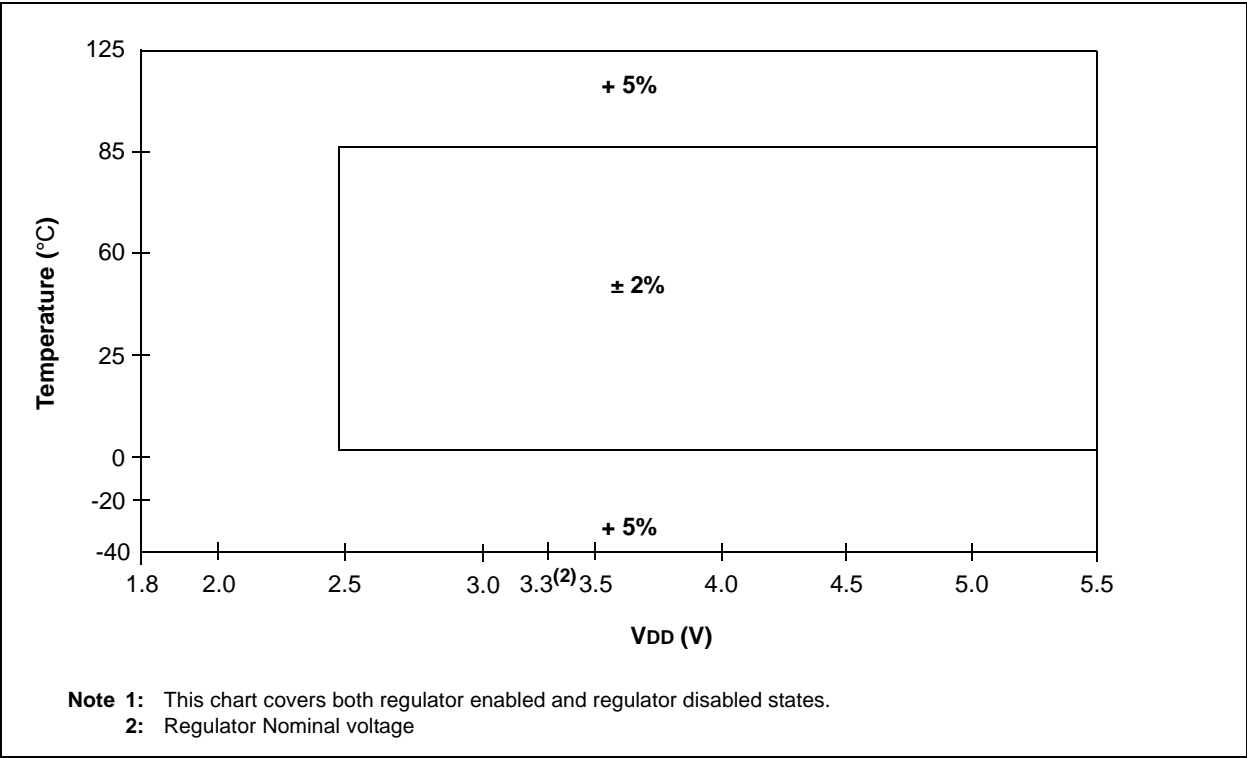


FIGURE 23-6: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE



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FIGURE 24-9: PIC16F722/3/4/6/7 MAXIMUM I_{DD} vs. F_{OSC} OVER V_{DD} , HS MODE, $V_{CAP} = 0.1 \mu F$

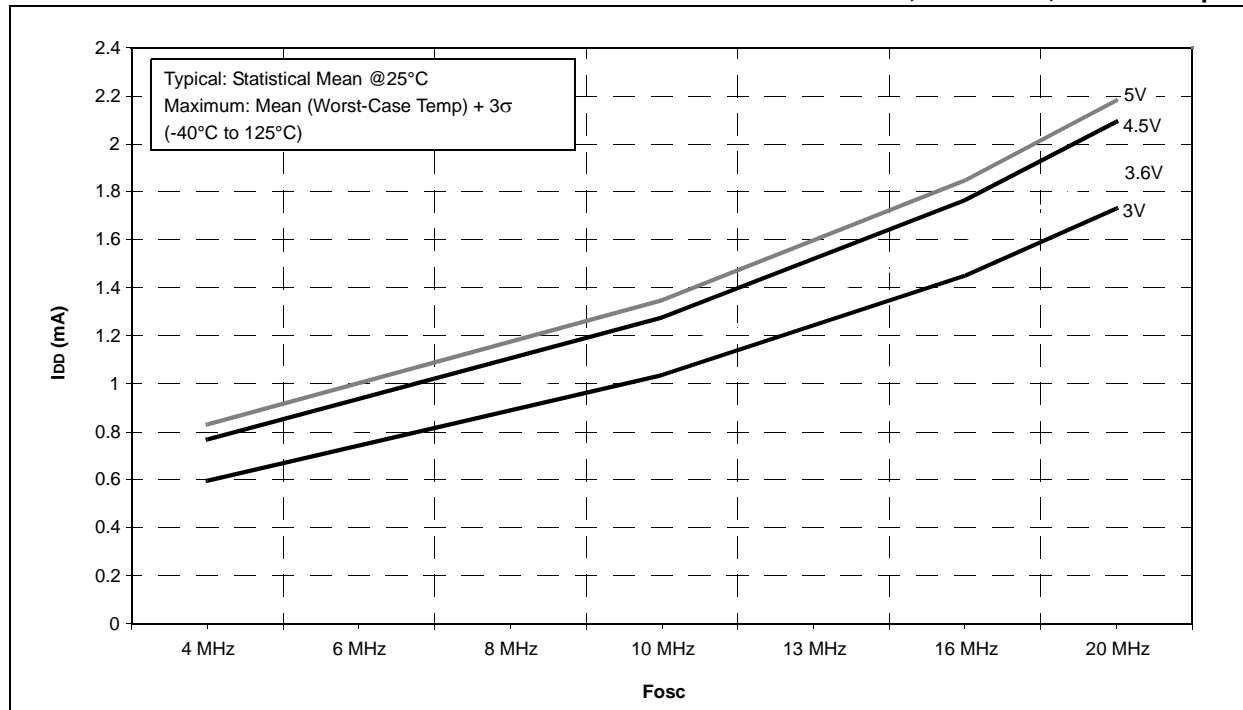
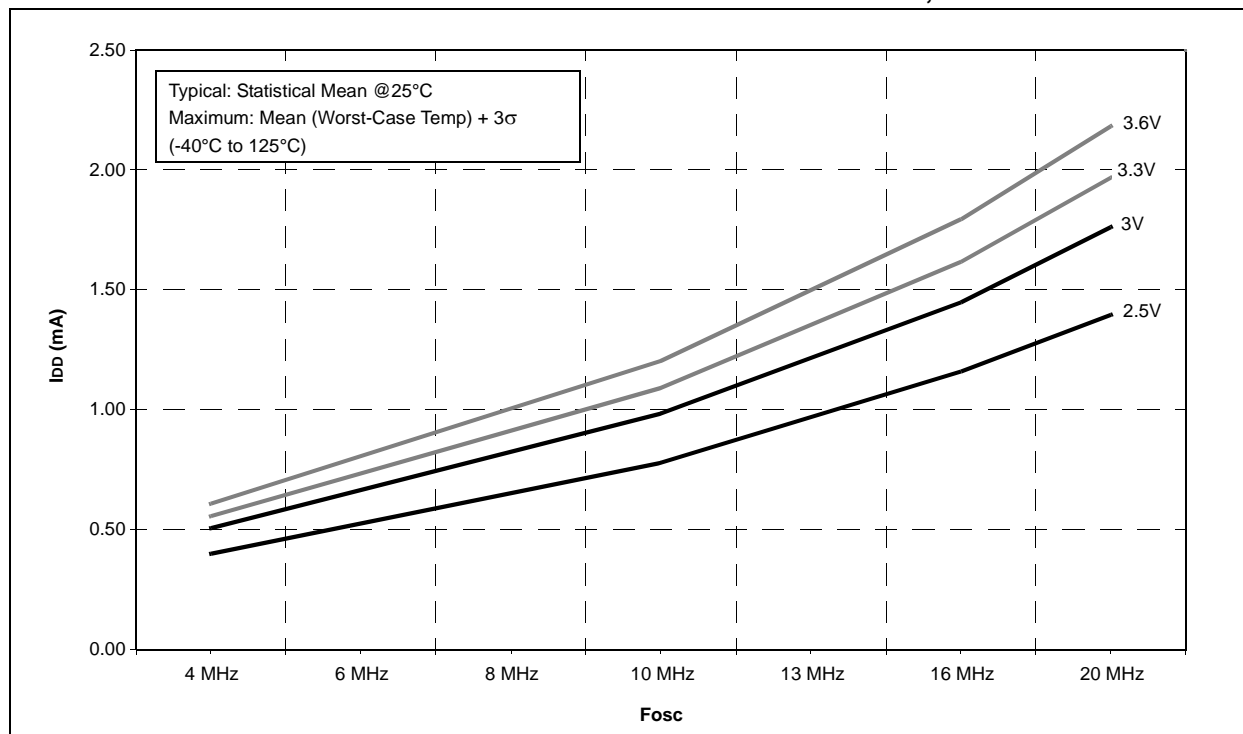
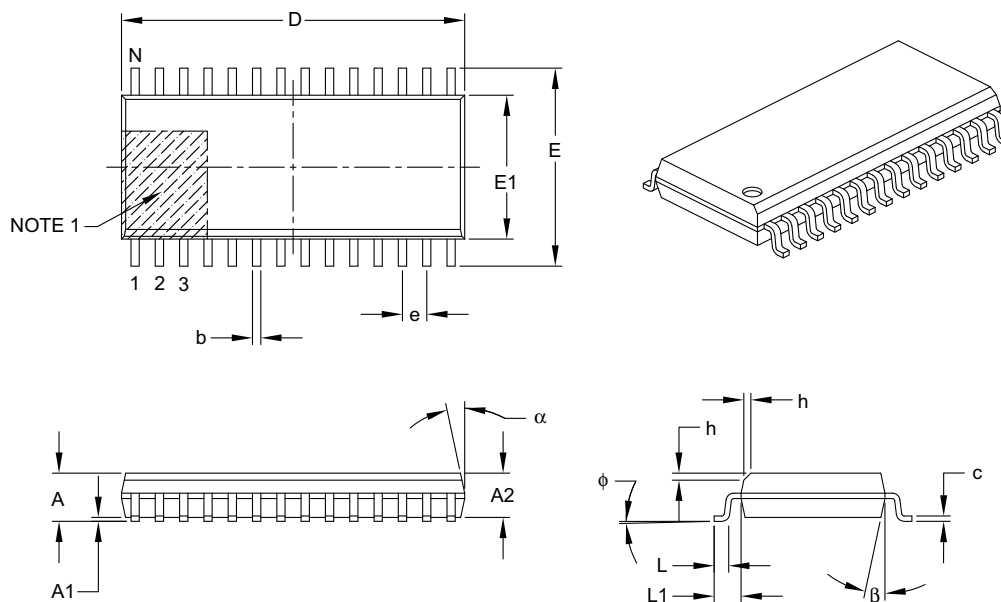


FIGURE 24-10: PIC16LF722/3/4/6/7 MAXIMUM I_{DD} vs. F_{OSC} OVER V_{DD} , HS MODE



28-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		28		
Pitch	e		1.27 BSC		
Overall Height	A		–	–	2.65
Molded Package Thickness	A2		2.05	–	–
Standoff §	A1		0.10	–	0.30
Overall Width	E		10.30 BSC		
Molded Package Width	E1		7.50 BSC		
Overall Length	D		17.90 BSC		
Chamfer (optional)	h		0.25	–	0.75
Foot Length	L		0.40	–	1.27
Footprint	L1		1.40 REF		
Foot Angle Top	phi		0°	–	8°
Lead Thickness	c		0.18	–	0.33
Lead Width	b		0.31	–	0.51
Mold Draft Angle Top	alpha		5°	–	15°
Mold Draft Angle Bottom	beta		5°	–	15°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-052B

28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

