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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf727t-i-ml

FIGURE 1-1: PIC16F722/723/726/PIC16LF722/723/726 BLOCK DIAGRAM



PIC16(L)F722/3/4/6/7

TABLE 1-1: PIC16(L)F722/3/4/6/7 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RD3/CPS11	RD3	ST	CMOS	General purpose I/O.
	CPS11	AN	—	Capacitive sensing input 11.
RD4/CPS12	RD4	ST	CMOS	General purpose I/O.
	CPS12	AN	—	Capacitive sensing input 12.
RD5/CPS13	RD5	ST	CMOS	General purpose I/O.
	CPS13	AN	—	Capacitive sensing input 13.
RD6/CPS14	RD6	ST	CMOS	General purpose I/O.
	CPS14	AN	—	Capacitive sensing input 14.
RD7/CPS15	RD7	ST	CMOS	General purpose I/O.
	CPS15	AN	—	Capacitive sensing input 15.
RE0/AN5	RE0	ST	CMOS	General purpose I/O.
	AN5	AN	—	A/D Channel 5 input.
RE1/AN6	RE1	ST	CMOS	General purpose I/O.
	AN6	AN	—	A/D Channel 6 input.
RE2/AN7	RE2	ST	CMOS	General purpose I/O.
	AN7	AN	—	A/D Channel 7 input.
RE3/MCLR/VPP	RE3	TTL	—	General purpose input.
	MCLR	ST	—	Master Clear with internal pull-up.
	VPP	HV	—	Programming voltage.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

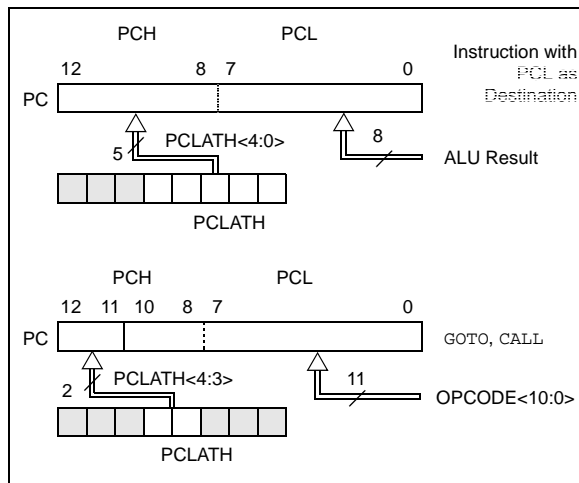
Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C = Schmitt Trigger input with I²C
HV = High Voltage XTAL = Crystal levels

Note: The PIC16F722/3/4/6/7 devices have an internal low dropout voltage regulator. An external capacitor must be connected to one of the available VCAP pins to stabilize the regulator. For more information, see **Section 5.0 “Low Dropout (LDO) Voltage Regulator”**. The PIC16LF722/3/4/6/7 devices do not have the voltage regulator and therefore no external capacitor is required.

2.3 PCL and PCLATH

The Program Counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 2-7 shows the two situations for the loading of the PC. The upper example in Figure 2-7 shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in Figure 2-7 shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 2-7: LOADING OF PC IN DIFFERENT SITUATIONS



2.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to the Application Note AN556, *Implementing a Table Read* (DS00556).

2.3.2 STACK

All devices have an 8-level x 13-bit wide hardware stack (refer to Figures 2-1 and 2-3). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth PUSH overwrites the value that was stored from the first PUSH. The tenth PUSH overwrites the second PUSH (and so on).

Note 1: There are no Status bits to indicate Stack Overflow or Stack Underflow conditions.

2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

2.4 Program Memory Paging

All devices are capable of addressing a continuous 8K word block of program memory. The CALL and GOTO instructions provide only 11 bits of address to allow branching within any 2K program memory page. When doing a CALL or GOTO instruction, the upper two bits of the address are provided by PCLATH<4:3>. When doing a CALL or GOTO instruction, the user must ensure that the page select bits are programmed so that the desired program memory page is addressed. If a return from a CALL instruction (or interrupt) is executed, the entire 13-bit PC is POPed off the stack. Therefore, manipulation of the PCLATH<4:3> bits is not required for the RETURN instructions (which POPs the address from the stack).

Note: The contents of the PCLATH register are unchanged after a RETURN or RETFIE instruction is executed. The user must rewrite the contents of the PCLATH register for any subsequent subroutine calls or GOTO instructions.

Example 2-1 shows the calling of a subroutine in page 1 of the program memory. This example assumes that PCLATH is saved and restored by the Interrupt Service Routine (if interrupts are used).

EXAMPLE 2-1: CALL OF A SUBROUTINE IN PAGE 1 FROM PAGE 0

```

ORG 500h
PAGESEL SUB_P1 ;Select page 1
                ;(800h-FFFh)
CALL SUB1_P1 ;Call subroutine in
:            ;page 1 (800h-FFFh)
:
ORG 900h ;page 1 (800h-FFFh)
SUB1_P1
:            ;called subroutine
:            ;page 1 (800h-FFFh)
:
RETURN ;return to
        ;Call subroutine
        ;in page 0
        ;(000h-7FFh)
    
```

3.4.2 WDT CONTROL

The WDTE bit is located in the Configuration Word Register 1. When set, the WDT runs continuously.

The PSA and PS<2:0> bits of the OPTION register control the WDT period. See **Section 11.0 “Timer0 Module”** for more information.

FIGURE 3-1: WATCHDOG TIMER BLOCK DIAGRAM

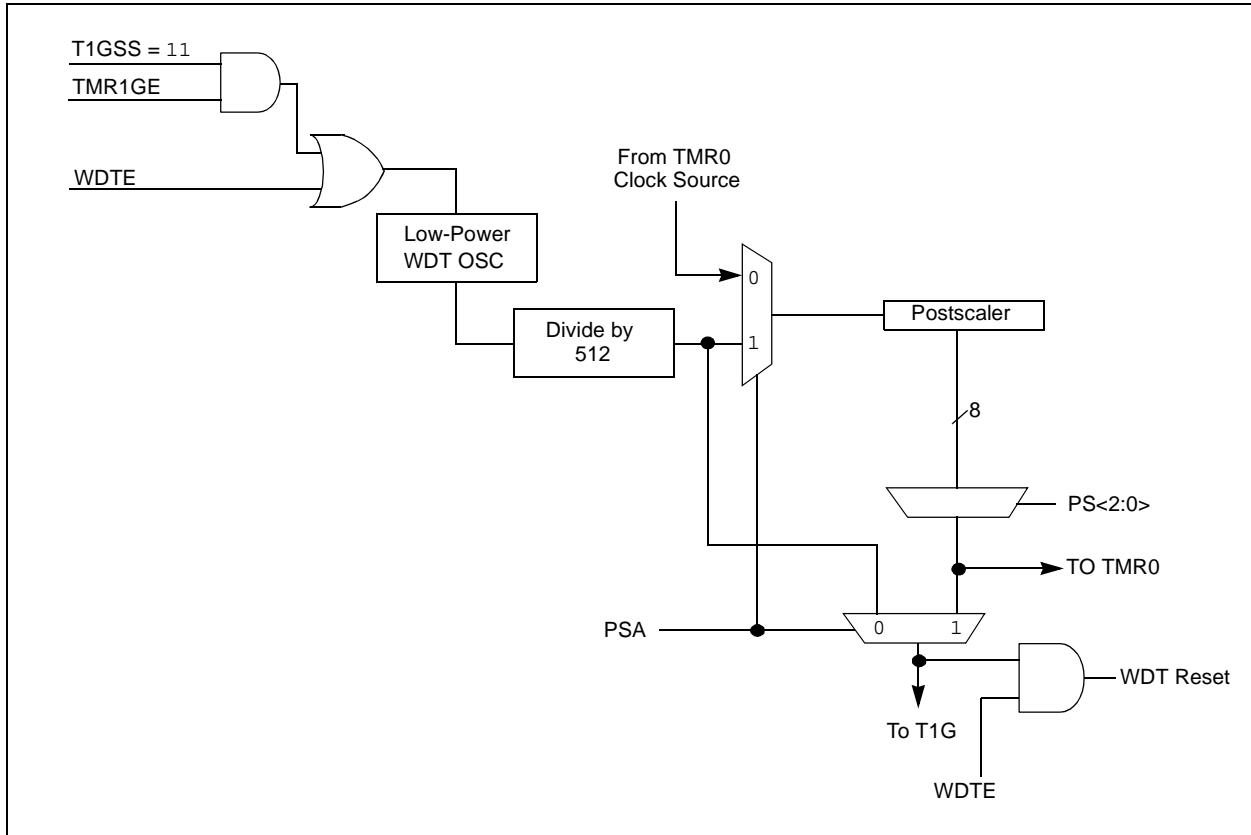


TABLE 3-1: WDT STATUS

Conditions	WDT
$WDTE = 0$	Cleared
CLRWDT Command	
Exit Sleep + System Clock = T1OSC, EXTRC, INTOSC, EXTCLK	
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST

TABLE 3-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	0000h	0001 1xxx	---- --0x
MCLR Reset during normal operation	0000h	000u uuuu	---- --uu
MCLR Reset during Sleep	0000h	0001 0uuu	---- --uu
WDT Reset	0000h	0000 uuuu	---- --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu
Brown-out Reset	0000h	0001 1xxx	---- --10
Interrupt Wake-up from Sleep	PC + 1 ⁽¹⁾	uuu1 0uuu	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and Global Interrupt Enable bit, GIE, is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

TABLE 3-6: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets ⁽¹⁾
STATUS	IRP	RP1	RP0	\overline{TO}	\overline{PD}	Z	DC	C	0001 1xxx	000q quuu
PCON	—	—	—	—	—	—	\overline{POR}	\overline{BOR}	---- --qq	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition. Shaded cells are not used by Resets.

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

EXAMPLE 4-1: SAVING W, STATUS AND PCLATH REGISTERS IN RAM

```
MOVWF    W_TEMP           ;Copy W to W_TEMP register
SWAPF    STATUS,W         ;Swap status to be saved into W
                        ;Swaps are used because they do not affect the status bits
BANKSEL  STATUS_TEMP      ;Select regardless of current bank
MOVWF    STATUS_TEMP      ;Copy status to bank zero STATUS_TEMP register
MOVF     PCLATH,W         ;Copy PCLATH to W register
MOVWF    PCLATH_TEMP      ;Copy W register to PCLATH_TEMP
:
:(ISR)           ;Insert user code here
:
BANKSEL  STATUS_TEMP      ;Select regardless of current bank
MOVF     PCLATH_TEMP,W    ;
MOVWF    PCLATH           ;Restore PCLATH
SWAPF    STATUS_TEMP,W    ;Swap STATUS_TEMP register into W
                        ;(sets bank to original state)
MOVWF    STATUS           ;Move W into STATUS register
SWAPF    W_TEMP,F         ;Swap W_TEMP
SWAPF    W_TEMP,W         ;Swap W_TEMP into W
```

4.5.1 INTCON REGISTER

The INTCON register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, PORTB change and external RB0/INT/SEG0 pin interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

7.0 OSCILLATOR MODULE

7.1 Overview

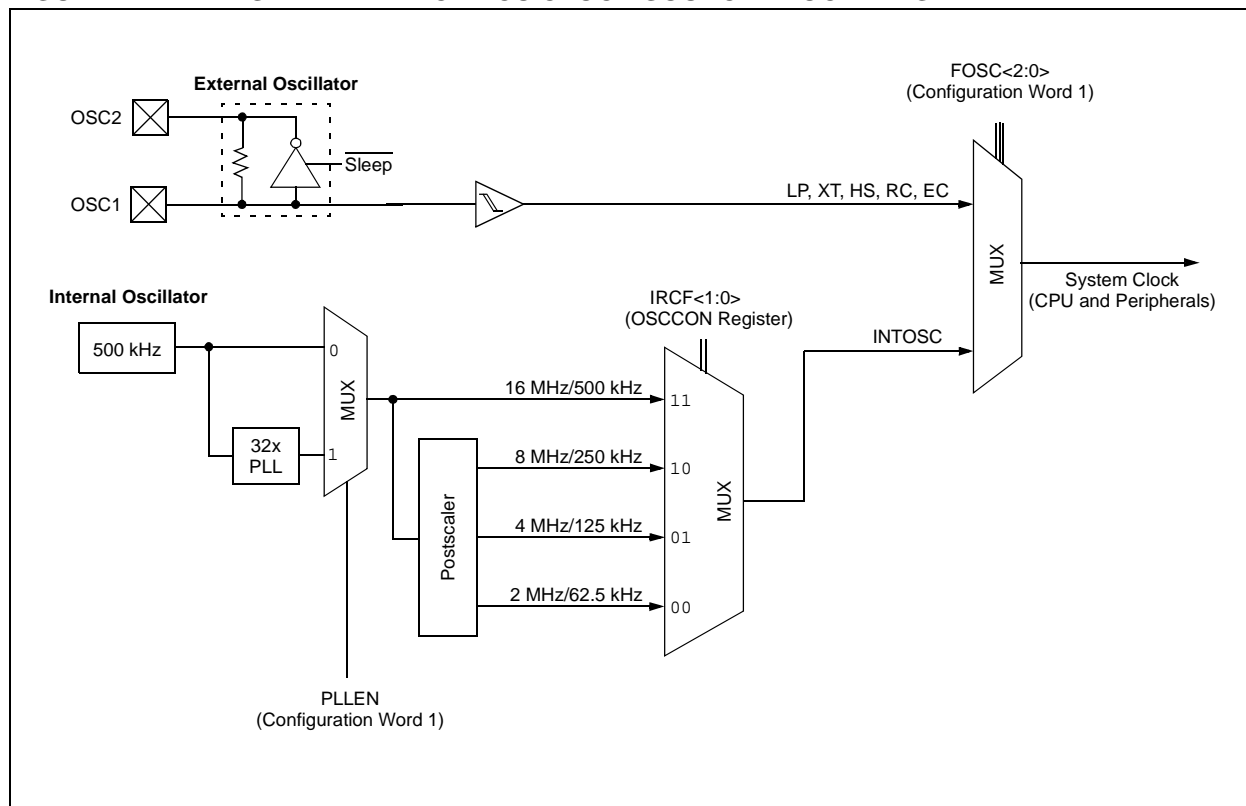
The oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 7-1 illustrates a block diagram of the oscillator module.

Clock sources can be configured from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system can be configured to use an internal calibrated high-frequency oscillator as clock source, with a choice of selectable speeds via software.

Clock source modes are configured by the FOSC bits in Configuration Word 1 (CONFIG1). The oscillator module can be configured for one of eight modes of operation.

1. RC – External Resistor-Capacitor (RC) with Fosc/4 output on OSC2/CLKOUT.
2. RCIO – External Resistor-Capacitor (RC) with I/O on OSC2/CLKOUT.
3. INTOSC – Internal oscillator with Fosc/4 output on OSC2 and I/O on OSC1/CLKIN.
4. INTOSCIO – Internal oscillator with I/O on OSC1/CLKIN and OSC2/CLKOUT.
5. EC – External clock with I/O on OSC2/CLKOUT.
6. HS – High Gain Crystal or Ceramic Resonator mode.
7. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode.
8. LP – Low-Power Crystal mode.

FIGURE 7-1: SIMPLIFIED PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



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11.1.3 SOFTWARE PROGRAMMABLE PRESCALER

A single software programmable prescaler is available for use with either Timer0 or the Watchdog Timer (WDT), but not both simultaneously. The prescaler assignment is controlled by the PSA bit of the OPTION register. To assign the prescaler to Timer0, the PSA bit must be cleared to a '0'.

There are eight prescaler options for the Timer0 module ranging from 1:2 to 1:256. The prescale values are selectable via the PS<2:0> bits of the OPTION register. In order to have a 1:1 prescaler value for the Timer0 module, the prescaler must be assigned to the WDT module.

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register will clear the prescaler.

Note: When the prescaler is assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT.

11.1.4 TIMER0 INTERRUPT

Timer0 will generate an interrupt when the TMR0 register overflows from FFh to 00h. The T0IF interrupt flag bit of the INTCON register is set every time the TMR0 register overflows, regardless of whether or not the Timer0 interrupt is enabled. The T0IF bit can only be cleared in software. The Timer0 interrupt enable is the T0IE bit of the INTCON register.

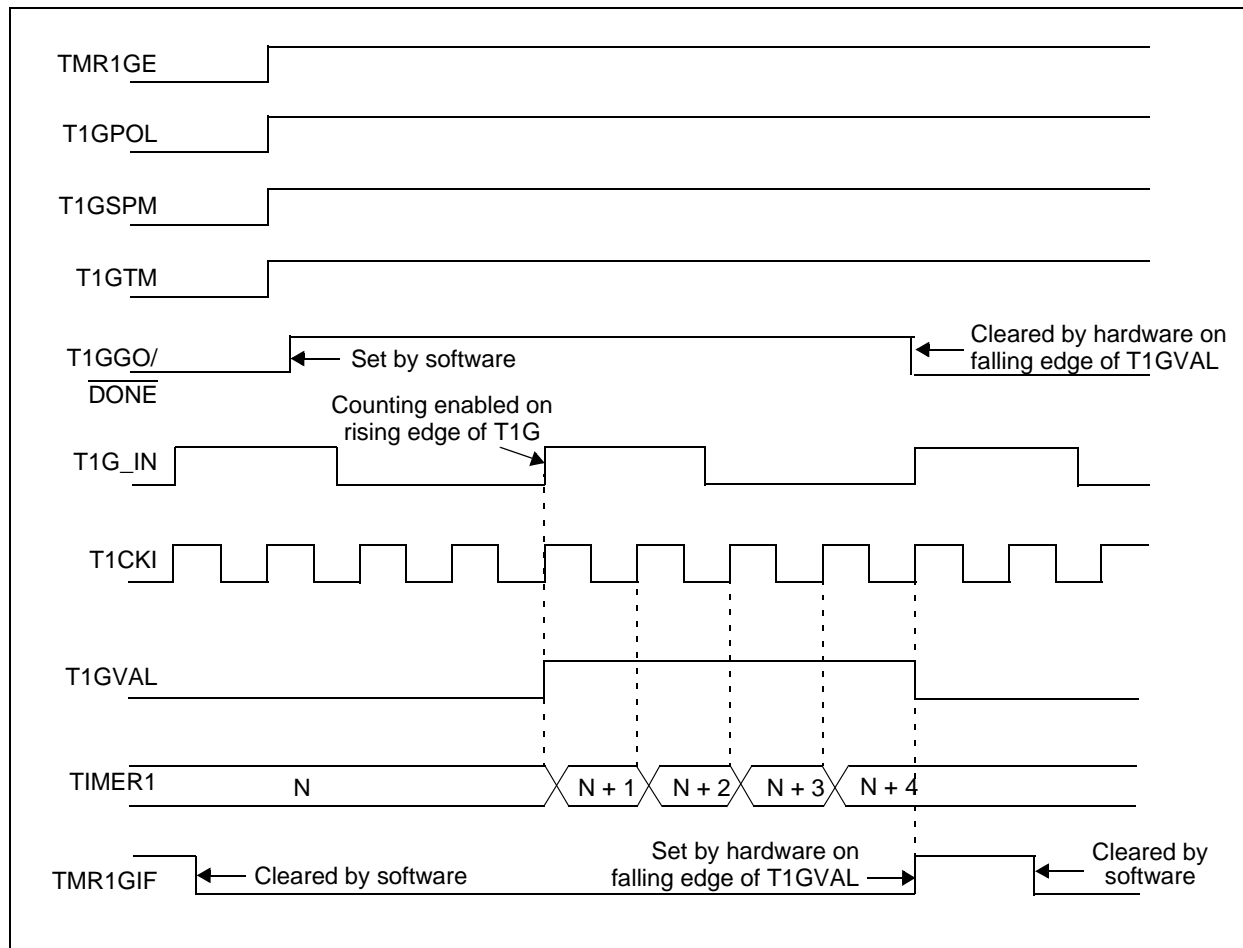
Note: The Timer0 interrupt cannot wake the processor from Sleep since the timer is frozen during Sleep.
--

11.1.5 8-BIT COUNTER MODE SYNCHRONIZATION

When in 8-Bit Counter mode, the incrementing edge on the T0CKI pin must be synchronized to the instruction clock. Synchronization can be accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the instruction clock. The high and low periods of the external clocking source must meet the timing requirements as shown in **Section 23.0 “Electrical Specifications”**.

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FIGURE 12-6: TIMER1 GATE SINGLE-PULSE AND TOGGLE COMBINED MODE



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12.12 Timer1 Gate Control Register

The Timer1 Gate Control register (T1GCON), shown in Register 12-2, is used to control Timer1 Gate.

REGISTER 12-2: T1GCON: TIMER1 GATE CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-x	R/W-0	R/W-0
TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/ DONE	T1GVAL	T1GSS1	T1GSS0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **TMR1GE:** Timer1 Gate Enable bit

If TMR1ON = 0:

This bit is ignored

If TMR1ON = 1:

1 = Timer1 counting is controlled by the Timer1 gate function

0 = Timer1 counts regardless of Timer1 gate function

bit 6 **T1GPOL:** Timer1 Gate Polarity bit

1 = Timer1 gate is active-high (Timer1 counts when gate is high)

0 = Timer1 gate is active-low (Timer1 counts when gate is low)

bit 5 **T1GTM:** Timer1 Gate Toggle Mode bit

1 = Timer1 Gate Toggle mode is enabled.

0 = Timer1 Gate Toggle mode is disabled and toggle flip flop is cleared

Timer1 gate flip flop toggles on every rising edge.

bit 4 **T1GSPM:** Timer1 Gate Single Pulse Mode bit

1 = Timer1 gate Single-Pulse mode is enabled and is controlling Timer1 gate

0 = Timer1 gate Single-Pulse mode is disabled

bit 3 **T1GGO/DONE:** Timer1 Gate Single-Pulse Acquisition Status bit

1 = Timer1 gate single-pulse acquisition is ready, waiting for an edge

0 = Timer1 gate single-pulse acquisition has completed or has not been started

This bit is automatically cleared when T1GSPM is cleared.

bit 2 **T1GVAL:** Timer1 Gate Current State bit

Indicates the current state of the Timer1 gate that could be provided to TMR1H:TMR1L.

Unaffected by Timer1 Gate Enable (TMR1GE).

bit 1-0 **T1GSS<1:0>:** Timer1 Gate Source Select bits

00 = Timer1 Gate pin

01 = Timer0 Overflow output

10 = TMR2 Match PR2 output

11 = Watchdog Timer scaler overflow

Watchdog Timer oscillator is turned on if TMR1GE = 1, regardless of the state of TMR1ON

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15.3.4 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is ten bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 15-4.

EQUATION 15-4: PWM RESOLUTION

$$Resolution = \frac{\log[4(PR2 + 1)]}{\log(2)} \text{ bits}$$

Note: If the pulse-width value is greater than the period, the assigned PWM pin(s) will remain unchanged.

TABLE 15-5: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 15-6: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

15.3.5 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCPx pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

15.3.6 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency (Fosc). Any changes in the system clock frequency will result in changes to the PWM frequency. Refer to **Section 7.0 “Oscillator Module”** for additional details.

15.3.7 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

15.3.8 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Disable the PWM pin (CCPx) output driver(s) by setting the associated TRIS bit(s).
2. Load the PR2 register with the PWM period value.
3. Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.

4. Load the CCPRxL register and the DCxBx bits of the CCPxCON register, with the PWM duty cycle value.
5. Configure and start Timer2:
 - Clear the TMR2IF interrupt flag bit of the PIR1 register. See Note below.
 - Configure the T2CKPS bits of the T2CON register with the Timer2 prescale value.
 - Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output pin:
 - Wait until Timer2 overflows, TMR2IF bit of the PIR1 register is set. See Note below.
 - Enable the PWM pin (CCPx) output driver(s) by clearing the associated TRIS bit(s).

Note: In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

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16.1.2.4 Receive Framing Error

Each character in the receive FIFO buffer has a corresponding framing error Status bit. A framing error indicates that a Stop bit was not seen at the expected time. The framing error status is accessed via the FERR bit of the RCSTA register. The FERR bit represents the status of the top unread character in the receive FIFO. Therefore, the FERR bit must be read before reading the RCREG.

The FERR bit is read-only and only applies to the top unread character in the receive FIFO. A framing error (FERR = 1) does not preclude reception of additional characters. It is not necessary to clear the FERR bit. Reading the next character from the FIFO buffer will advance the FIFO to the next character and the next corresponding framing error.

The FERR bit can be forced clear by clearing the SPEN bit of the RCSTA register which resets the AUSART. Clearing the CREN bit of the RCSTA register does not affect the FERR bit. A framing error by itself does not generate an interrupt.

Note: If all receive characters in the receive FIFO have framing errors, repeated reads of the RCREG will not clear the FERR bit.
--

16.1.2.5 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before the FIFO is accessed. When this happens the OERR bit of the RCSTA register is set. The characters already in the FIFO buffer can be read but no additional characters will be received until the error is cleared. The error must be cleared by either clearing the CREN bit of the RCSTA register or by setting the AUSART by clearing the SPEN bit of the RCSTA register.

16.1.2.6 Receiving 9-bit Characters

The AUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set the AUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREG.

16.1.2.7 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RCSTA register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the ninth data bit set will be transferred to the receive FIFO buffer, thereby setting the RCIF interrupt bit of the PIR1 register. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.

PIC16(L)F722/3/4/6/7

FIGURE 17-4: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 0)

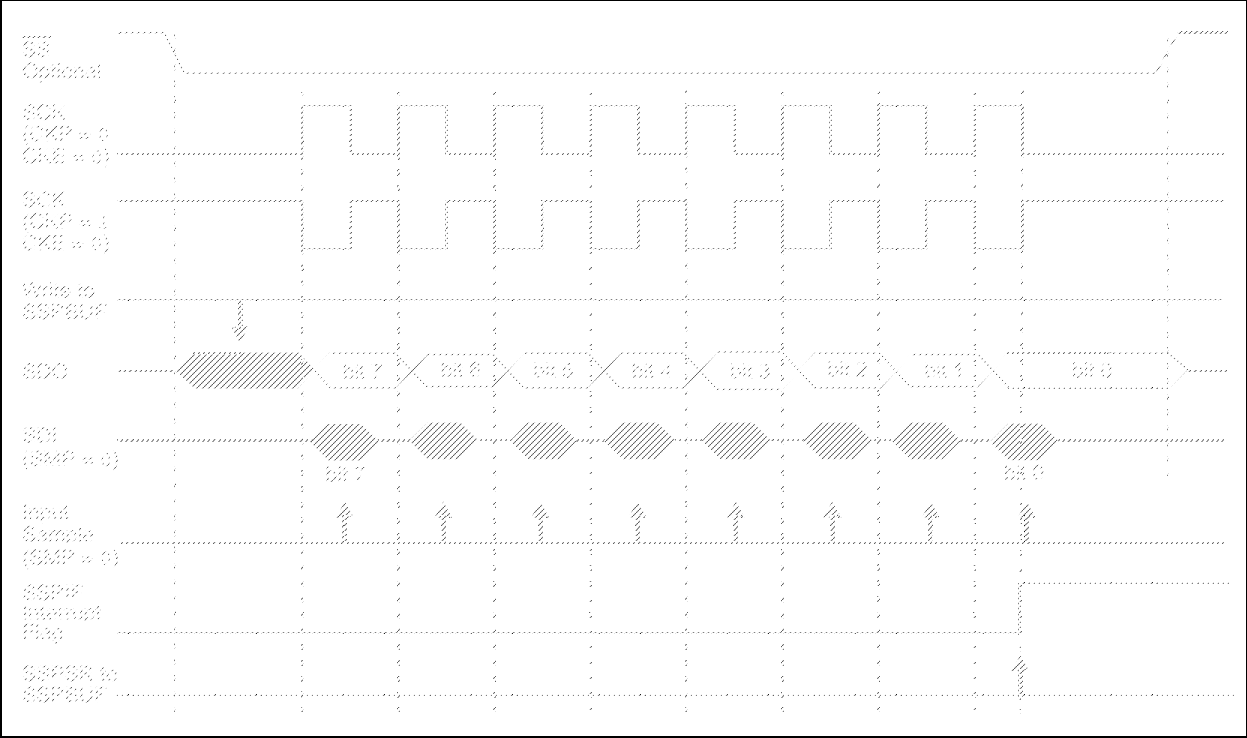
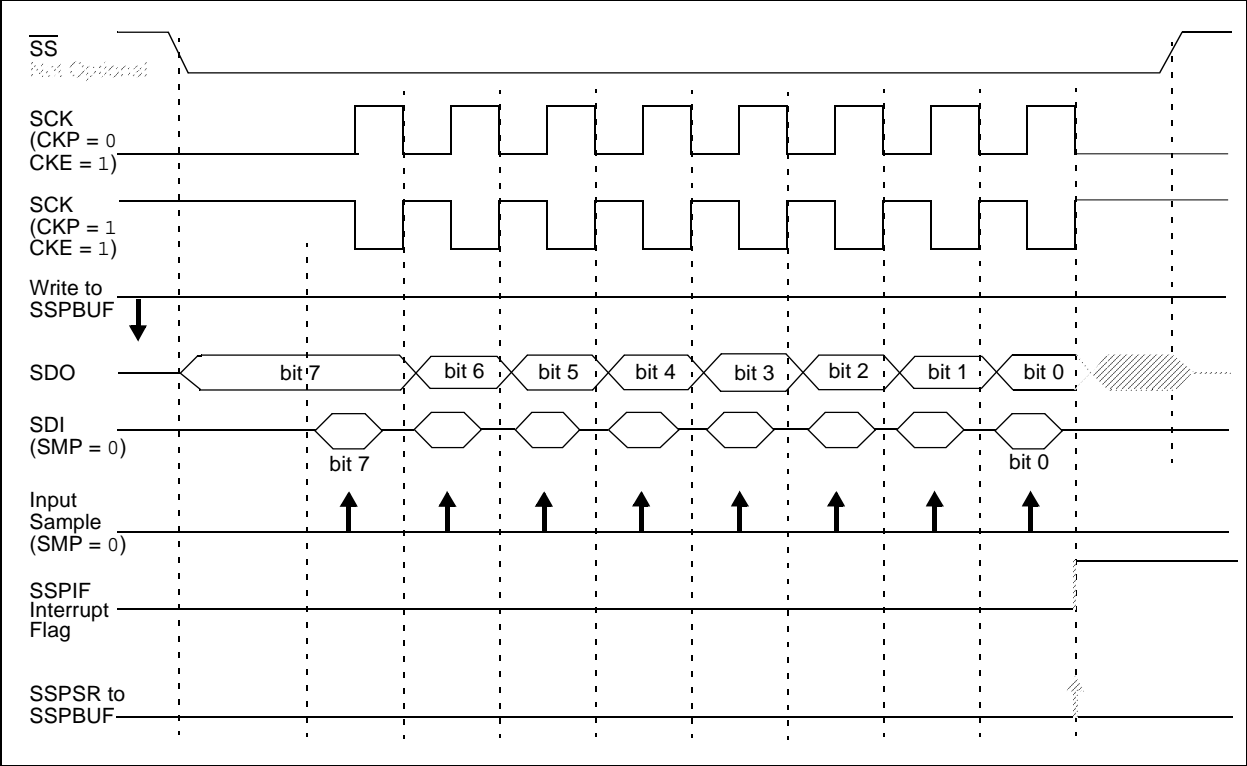


FIGURE 17-5: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)



PIC16(L)F722/3/4/6/7

17.2.2 START AND STOP CONDITIONS

During times of no data transfer (Idle time), both the clock line (SCL) and the data line (SDA) are pulled high through external pull-up resistors. The Start and Stop conditions determine the start and stop of data transmission. The Start condition is defined as a high-to-low transition of the SDA line while SCL is high. The Stop condition is defined as a low-to-high transition of the SDA line while SCL is high.

Figure 17-9 shows the Start and Stop conditions. A master device generates these conditions for starting and terminating data transfer. Due to the definition of the Start and Stop conditions, when data is being transmitted, the SDA line can only change state when the SCL line is low.

17.2.3 ACKNOWLEDGE

After the valid reception of an address or data byte, the hardware automatically will generate the Acknowledge (ACK) pulse and load the SSPBUF register with the received value currently in the SSPSR register. There are certain conditions that will cause the SSP module not to generate this ACK pulse. They include any or all of the following:

- The Buffer Full bit, BF of the SSPSTAT register, was set before the transfer was received.
- The SSP Overflow bit, SSPOV of the SSPCON register, was set before the transfer was received.
- The SSP Module is being operated in Firmware Master mode.

In such a case, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF of the PIR1 register is set. Table 17-2 shows the results of when a data transfer byte is received, given the status of bits BF and SSPOV. Flag bit BF is cleared by reading the SSPBUF register, while bit SSPOV is cleared through software.

FIGURE 17-9: START AND STOP CONDITIONS

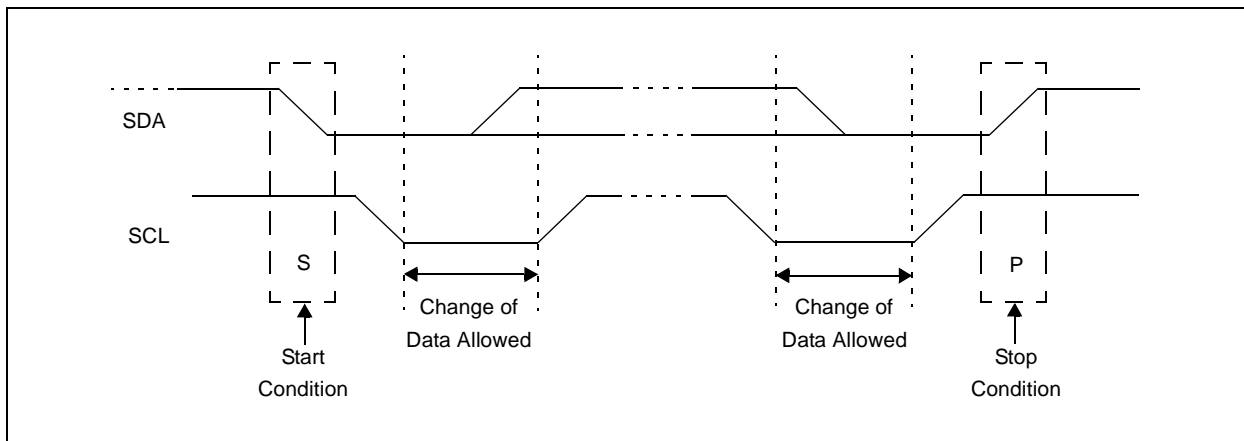


TABLE 17-2: DATA TRANSFER RECEIVED BYTE ACTIONS

Status Bits as Data Transfer is Received		SSPSR → SSPBUF	Generate $\overline{\text{ACK}}$ Pulse	Set bit SSPIF (SSP Interrupt occurs if enabled)
BF	SSPOV			
0	0	Yes	Yes	Yes
1	0	No	No	Yes
1	1	No	No	Yes
0	1	No	No	Yes

Note 1: Shaded cells show the conditions where the user software did not properly clear the overflow condition.

RETFIE	Return from Interrupt
Syntax:	[<i>label</i>] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a 2-cycle instruction.
Words:	1
Cycles:	2
<u>Example:</u>	<pre>RETFIE</pre> <p>After Interrupt</p> <pre>PC = TOS GIE = 1</pre>

RETLW	Return with literal in W
Syntax:	[<i>label</i>] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the 8-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.
Words:	1
Cycles:	2
<u>Example:</u>	<pre>CALL TABLE;W contains table ;offset value • ;W now has table value • • ADDWF PC ;W = offset RETLW k1 ;Begin table RETLW k2 ; • • • RETLW kn ; End of table</pre> <p>Before Instruction W = 0x07</p> <p>After Instruction W = value of k8</p>

RETURN	Return from Subroutine
Syntax:	[<i>label</i>] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a 2-cycle instruction.

PIC16(L)F722/3/4/6/7

RLF Rotate Left f through Carry

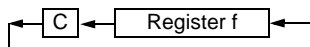
Syntax: [*label*] RLF *f*,*d*

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example: RLF REG1,0

Before Instruction

REG1 = 1110 0110
C = 0

After Instruction

REG1 = 1110 0110
W = 1100 1100
C = 1

SLEEP Enter Sleep mode

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → \overline{TO} ,
0 → \overline{PD}

Status Affected: \overline{TO} , \overline{PD}

Description: The power-down Status bit, \overline{PD} is cleared. Time-out Status bit, \overline{TO} is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

RRF Rotate Right f through Carry

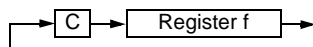
Syntax: [*label*] RRF *f*,*d*

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



SUBLW Subtract W from literal

Syntax: [*label*] SUBLW *k*

Operands: $0 \leq k \leq 255$

Operation: $k - (W) \rightarrow (W)$

Status Affected: C, DC, Z

Description: The W register is subtracted (2's complement method) from the 8-bit literal 'k'. The result is placed in the W register.

C = 0	$W > k$
C = 1	$W \leq k$
DC = 0	$W<3:0> > k<3:0>$
DC = 1	$W<3:0> \leq k<3:0>$

PIC16(L)F722/3/4/6/7

23.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings^(†)

Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to VSS, PIC16F72X	-0.3V to +6.5V
Voltage on VCAP pin with respect to VSS, PIC16F72X	-0.3V to +4.0V
Voltage on VDD with respect to VSS, PIC16LF72X	-0.3V to +4.0V
Voltage on $\overline{\text{MCLR}}$ with respect to VSS	-0.3V to +9.0V
Voltage on all other pins with respect to VSS	-0.3V to (VDD + 0.3V)
Total power dissipation ⁽¹⁾	800 mW
Maximum current out of VSS pin	95 mA
Maximum current into VDD pin	70 mA
Clamp current, I _K (V _{PIN} < 0 or V _{PIN} > VDD).....	± 20 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin.....	25 mA
Maximum current sunk by all ports ⁽²⁾ , -40°C ≤ T _A ≤ +85°C for industrial	200 mA
Maximum current sunk by all ports ⁽²⁾ , -40°C ≤ T _A ≤ +125°C for extended	90 mA
Maximum current sourced by all ports ⁽²⁾ , 40°C ≤ T _A ≤ +85°C for industrial	140 mA
Maximum current sourced by all ports ⁽²⁾ , -40°C ≤ T _A ≤ +125°C for extended.....	65 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

23.1 DC Characteristics: PIC16(L)F722/3/4/6/7-I/E (Industrial, Extended)

PIC16LF722/3/4/6/7		Standard Operating Conditions (unless otherwise stated)					
		Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
PIC16F722/3/4/6/7		Standard Operating Conditions (unless otherwise stated)					
		Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
Param. No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
D001	VDD	Supply Voltage					
		PIC16LF722/3/4/6/7	1.8	—	3.6	V	FOSC \leq 16 MHz: HFINTOSC, EC
			1.8	—	3.6	V	FOSC \leq 4 MHz
			2.3	—	3.6	V	FOSC \leq 20 MHz, EC
			2.5	—	3.6	V	FOSC \leq 20 MHz, HS
D001		PIC16F722/3/4/6/7	1.8	—	5.5	V	FOSC \leq 16 MHz: HFINTOSC, EC
			1.8	—	5.5	V	FOSC \leq 4 MHz
			2.3	—	5.5	V	FOSC \leq 20 MHz, EC
			2.5	—	5.5	V	FOSC \leq 20 MHz, HS
D002*	VDR	RAM Data Retention Voltage⁽¹⁾					
		PIC16LF722/3/4/6/7	1.5	—	—	V	Device in Sleep mode
D002*		PIC16F722/3/4/6/7	1.7	—	—	V	Device in Sleep mode
	VPOR*	Power-on Reset Release Voltage	—	1.6	—	V	
	VPORR*	Power-on Reset Rearm Voltage					
		PIC16LF722/3/4/6/7	—	0.8	—	V	Device in Sleep mode
		PIC16F722/3/4/6/7	—	1.7	—	V	Device in Sleep mode
D003	VFVR	Fixed Voltage Reference Voltage, Initial Accuracy	-8	—	6	%	VFVR = 1.024V, VDD \geq 2.5V
			-8	—	6	%	VFVR = 2.048V, VDD \geq 2.5V
			-8	—	6	%	VFVR = 4.096V, VDD \geq 4.75V; $-40 \leq T_A \leq 85^{\circ}\text{C}$
			-8	—	6	%	VFVR = 1.024V, VDD \geq 2.5V
			-8	—	6	%	VFVR = 2.048V, VDD \geq 2.5V
D004*	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See Section 3.2 "Power-on Reset (POR)" for details.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

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FIGURE 24-53: V_{OH} vs. I_{OH} OVER TEMPERATURE, $V_{DD} = 3.6V$

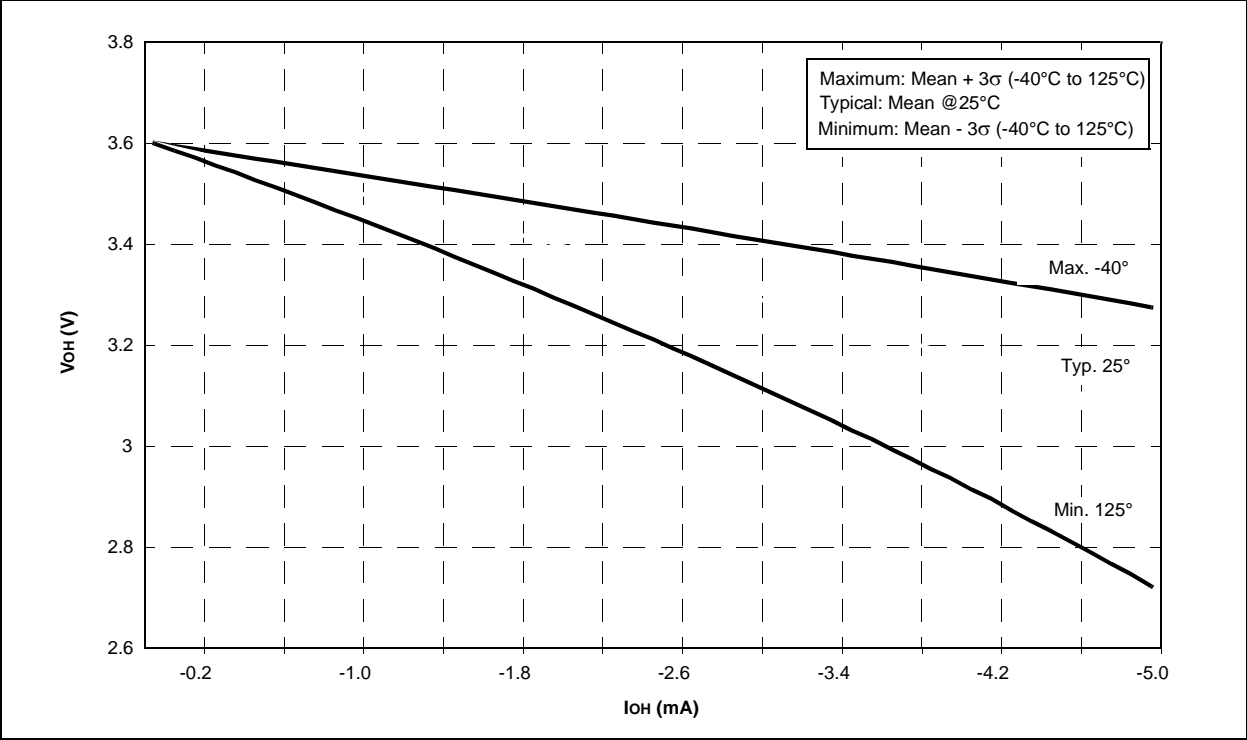
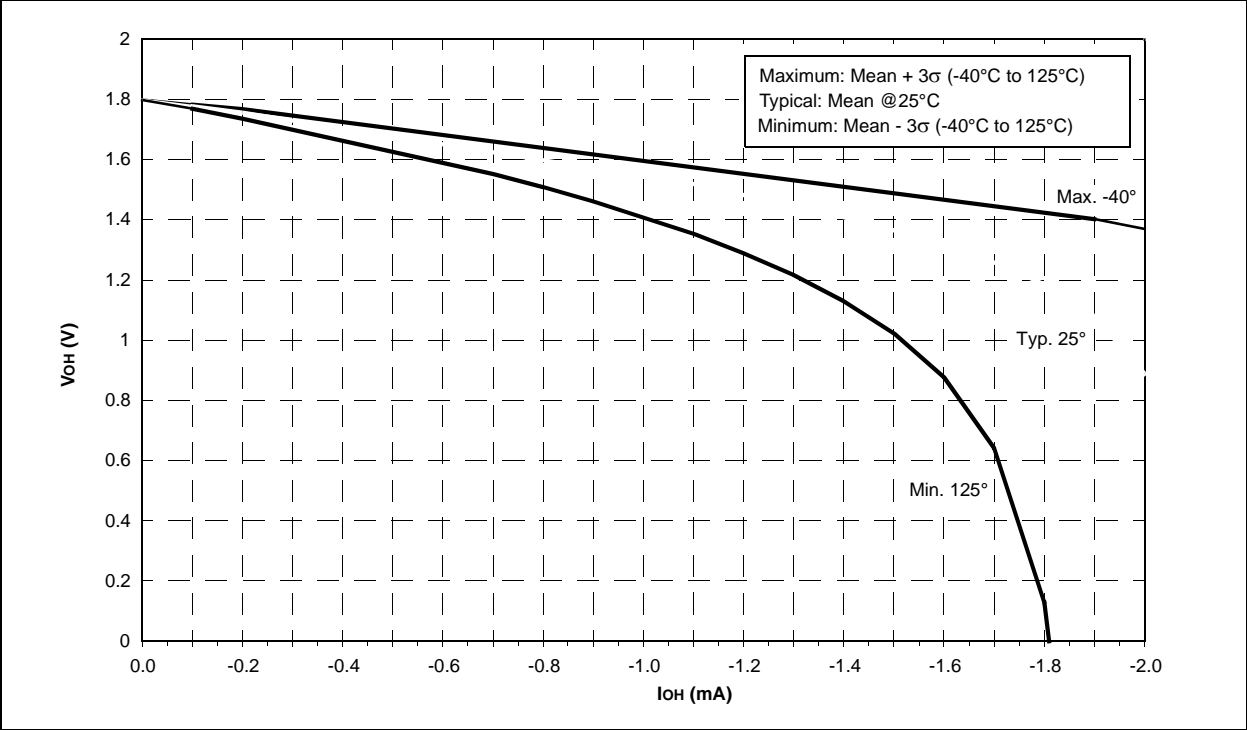


FIGURE 24-54: V_{OH} vs. I_{OH} OVER TEMPERATURE, $V_{DD} = 1.8V$



PIC16(L)F722/3/4/6/7

FIGURE 24-57: Vol vs. IoL OVER TEMPERATURE, VDD = 1.8V

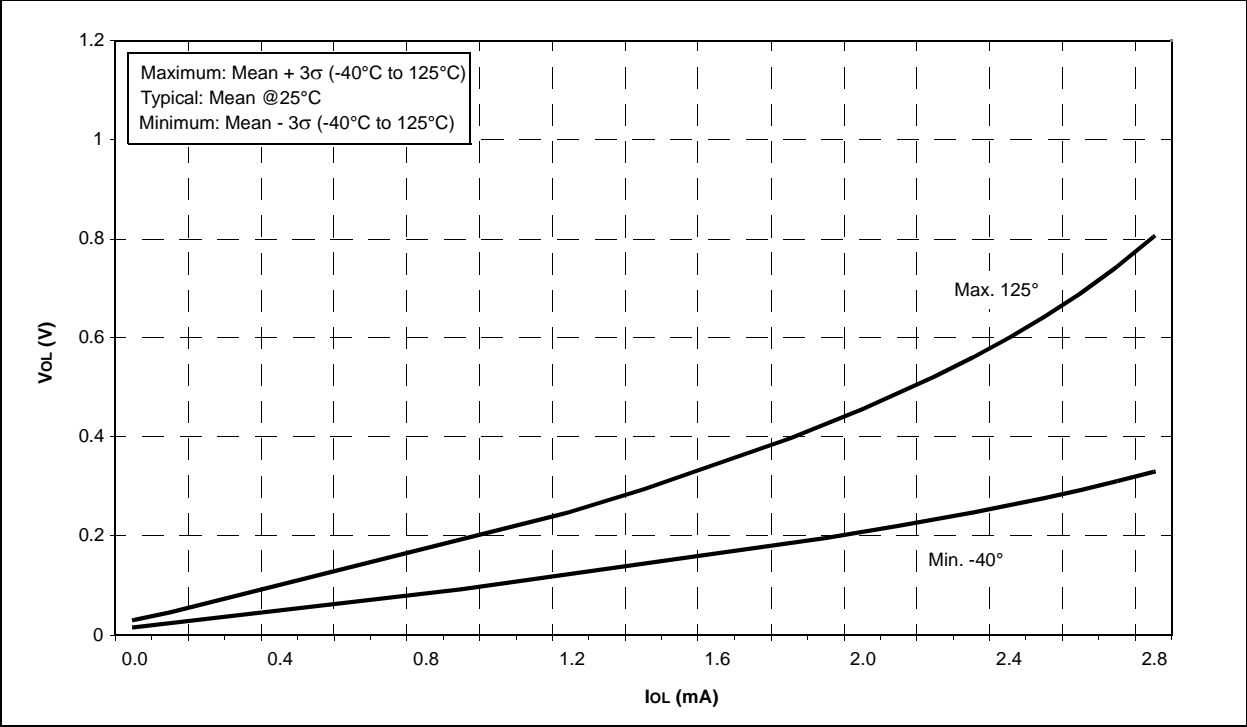


FIGURE 24-58: PIC16F722/3/4/6/7 PWRT PERIOD

