NXP USA Inc. - MSC8126MP8000 Datasheet

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC140 Core
Interface	DSI, Ethernet, RS-232
Clock Rate	500MHz
Non-Volatile Memory	External
On-Chip RAM	1.436MB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	431-BFBGA, FCBGA
Supplier Device Package	431-FCPBGA (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8126mp8000

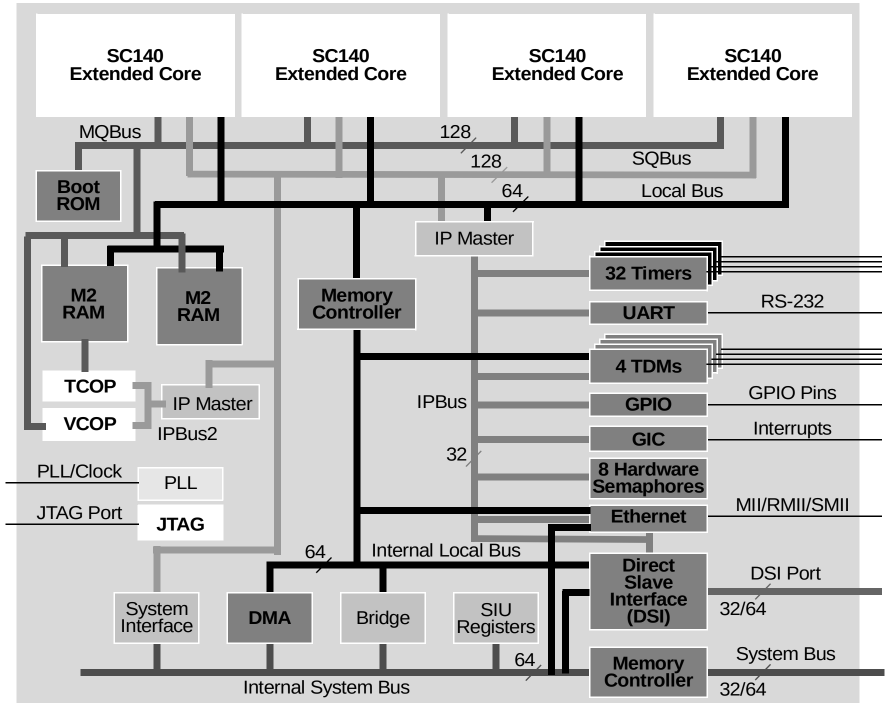
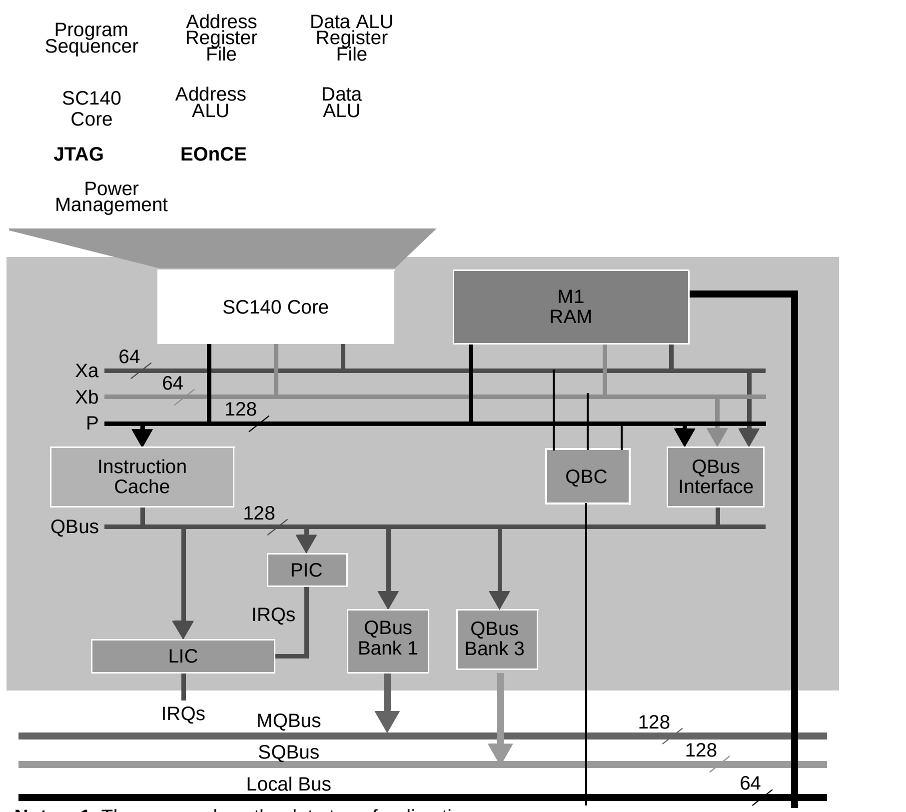


Figure 1. MSC8126 Block Diagram



Notes: 1. The arrows show the data transfer direction.
2. The QBus interface includes a bus switch, write buffer, fetch unit, and a control unit that defines four QBus banks. In addition, the QBC handles internal memory contentions.

Figure 2. StarCore SC140 DSP Extended Core Block Diagram

1 Pin Assignments

This section includes diagrams of the MSC8126 package ball grid array layouts and pinout allocation tables.

1.1 FC-PBGA Ball Layout Diagrams

Top and bottom views of the FC-PBGA package are shown in **Figure 3** and **Figure 4** with their ball location index numbers.

Bottom View

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2
B	GND	V_{DD}	V_{DD}	GPIO0	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	$\overline{NMI}$ OUT	GND	GND	V_{DD}	
C	GPIO6	GPIO5	GPIO3	GPIO7	GPIO1	GPIO2	GPIO30	GND	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	HCID1	GPIO28	$\overline{S}$ RESET	TDO	V_{DD}	GND
D	GPIO8	GND	V_{DDH}	GPIO4	V_{DDH}	GPIO29	GPIO31	V_{DD}	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	HCID3	HCID2	V_{DDH}	GND	EE1	EE0	TDI
E	GPIO12	GPIO10	GPIO13	GPIO9	GND	GND	V_{DD}	GND	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	HCID0	GPIO27	$\overline{HRESET}$	TMS	$\overline{TRST}$	TCK
F	GPIO19	GPIO14	GPIO11	GPIO16	GPIO18	GPIO20	ETHTX_CLK	ETHRX_CLK	V_{DD}	GND	V_{DD}	GND	V_{DD}	V_{DD}	V_{DD}	GND	HA22	HA29	$\overline{NMI}$	$\overline{RST}$ CONF	$\overline{PO}$ RESET
G	GPIO22	GPIO17	GND	GPIO15	$\overline{BCTL0}$	$\overline{CS1}$	V_{DD}	ETHCRS	$\overline{INT}$ OUT	V_{DD}	$\overline{ABB}$	BM0	BADDR31	V_{DD}	V_{DD}	$\overline{PWE0}$	HA17	HA23	HA25	HA27	HA24
H	A31	V_{DDH}	V_{DD}	GPIO21	GPIO24	$\overline{CS4}$	TT4	V_{DD}	$\overline{HTA}$	$\overline{DBB}$	$\overline{AACK}$	$\overline{ARTRY}$	BM1	V_{DD}	$\overline{PGTA}$	$\overline{PSD}$ CAS	TEST	HA19	V_{DD}	HA28	HA20
J	A30	GPIO25	GND	GPIO23	BCTL1	PSDA10	TT3	V_{DD}	GND	V_{DD}	$\overline{DBG}$	BM2	CLKIN	V_{DD}	BADDR27	PSDA MUX	GND	HA13	V_{DD}	HA26	HA18
K	A28	A29	A26	GND	$\overline{CS2}$	ALE	TT2	V_{DD}	CLKOUT	GND	GND	GND	GND	Res.	BADDR30	$\overline{POE}$	$\overline{PWE1}$	$\overline{PWE3}$	HA16	HA21	HA15
L	A22	A25	A27	V_{DDH}	$\overline{CS3}$	GND	GND	V_{DDH}	GND		MSC8126		GND	GND	BADDR29	BADDR28	V_{DDH}	V_{DDH}	HA11	HA14	HA12
M	A21	A24	V_{DDH}	GND	V_{DDH}	V_{DDH}	$\overline{HB}$ RST	V_{DDH}	GND				GND	V_{DDH}	V_{DD}	V_{DDH}	GND	GND	V_{DDH}	HD31	HD28
N	A20	A23	GPIO26	$\overline{PSDWE}$	$\overline{CS0}$	$\overline{HCS}$	$\overline{BG}$	$\overline{HRDS}$	GND				GND	$\overline{HBCS}$	HWBS0	V_{DDH}	$\overline{PWE2}$	HD24	HD29	HD30	HD26
P	A19	GND	V_{DDH}	DP0	$\overline{PSD}$ VAL	$\overline{TEA}$	$\overline{BR}$	$\overline{TA}$	GND	GND	V_{CCSYN}	GND_{SYN}	GND	HCLKIN	HWBS1	HWBS2	HWBS3	HD23	HD25	HD27	HD20
R	A16	A18	A17	DP2	$\overline{TS}$	DP3	DP6	DP7	TT0	V_{DD}	V_{DD}	V_{DD}	$\overline{GBL}$	TSZ3	TSZ1	HWBS4	HWBS6	HD22	GND	V_{DDH}	HD18
T	A14	A15	GND	D30	DP1	DP4	DP5	D23	D21	TT1	D16	V_{DD}	$\overline{TBST}$	TSZ2	TSZ0	HWBS5	HWBS7	HD0	HD1	HD21	HD17
U	A13	A12	V_{DDH}	D31	D28	D26	D25	D22	D19	D17	D15	D14	D11	D9	D8	D6	D3	D2	HD2	HD19	HD16
V	A11	A10	A9	A8	D29	D27	D24	GND	D20	D18	D13	D12	D10	D7	D5	D4	D1	D0	GND	V_{DDH}	HD3
W	A6	A7	GND	GND	HD32	V_{DDH}	HD33	V_{DDH}	HD40	GND	V_{DDH}	HDST0	HDST1	GND	V_{DDH}	V_{DDH}	GND	GND	HD4	HD5	HD6
Y	A5	A4	V_{DDH}	HD34	HD37	GND	V_{DDH}	GND	HD43	V_{DDH}	GND	HD51	V_{DDH}	GND	HD58	HD60	V_{DD}	HD9	V_{DDH}	HD15	HD7
AA	A3	A2	A0	HD35	HD38	HD42	GND	HD46	V_{DDH}	GND	V_{DDH}	HD52	HD54	V_{DDH}	GND	HD59	HD63	HD10	HD12	HD14	V_{DD}
AB	V_{DD}	A1	HD36	HD39	HD41	HD44	HD45	HD47	HD48	HD49	HD50	HD53	HD55	HD56	HD57	HD61	HD62	HD8	HD11	HD13	GND

Figure 4. MSC8126 Package, Bottom View

1.2 Signal List By Ball Location

Table 1 presents signal list sorted by ball number. -

Table 1. MSC8126 Signal Listing by Ball Designator

Des.	Signal Name	Des.	Signal Name
B3	V_{DD}	C18	GPIO1/TIMER0/CHIP_ID1/$\overline{\text{IRQ5}}$/ETHTXD1
B4	GND	C19	GPIO7/TDM3RCLK/$\overline{\text{IRQ5}}$/ETHTXD3
B5	GND	C20	GPIO3/TDM3TSYN/$\overline{\text{IRQ1}}$/ETHTXD2
B6	$\overline{\text{NMI\_OUT}}$	C21	GPIO5/TDM3TDAT/$\overline{\text{IRQ3}}$/ETHRXD3
B7	GND	C22	GPIO6/TDM3RSYN/$\overline{\text{IRQ4}}$/ETHRXD2
B8	V_{DD}	D2	TDI
B9	GND	D3	EE0
B10	V_{DD}	D4	EE1
B11	GND	D5	GND
B12	V_{DD}	D6	V_{DDH}
B13	GND	D7	HCID2
B14	V_{DD}	D8	HCID3/HA8
B15	GND	D9	GND
B16	V_{DD}	D10	V_{DD}
B17	GND	D11	GND
B18	V_{DD}	D12	V_{DD}
B19	GPIO0/CHIP_ID0/$\overline{\text{IRQ4}}$/ETHTXD0	D13	GND
B20	V_{DD}	D14	V_{DD}
B21	V_{DD}	D15	V_{DD}
B22	GND	D16	GPIO31/TIMER3/SCL
C2	GND	D17	GPIO29/CHIP_ID3/ETHTX_EN
C3	V_{DD}	D18	V_{DDH}
C4	TDO	D19	GPIO4/TDM3TCLK/$\overline{\text{IRQ2}}$/ETHTX_ER
C5	$\overline{\text{SRESET}}$	D20	V_{DDH}
C6	GPIO28/DREQ2/UTXD	D21	GND
C7	HCID1	D22	GPIO8/TDM3RDAT/$\overline{\text{IRQ6}}$/ETHCOL
C8	GND	E2	TCK
C9	V_{DD}	E3	$\overline{\text{TRST}}$
C10	GND	E4	TMS
C11	V_{DD}	E5	$\overline{\text{HRESET}}$
C12	GND	E6	GPIO27/DREQ1/URXD
C13	V_{DD}	E7	HCID0
C14	GND	E8	GND
C15	GND	E9	V_{DD}
C16	GPIO30/TIMER2/TMCLK/SDA	E10	GND
C17	GPIO2/TIMER1/CHIP_ID2/$\overline{\text{IRQ6}}$	E11	V_{DD}

Table 1. MSC8126 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
E12	GND	G6	HA17
E13	V_{DD}	G7	PWE0/PSDDQM0/PBS0
E14	GND	G8	V_{DD}
E15	GND	G9	V_{DD}
E16	V_{DD}	G10	IRQ3/BADDR31
E17	GND	G11	BM0/TC0/BNKSEL0
E18	GND	G12	ABB/IRQ4
E19	GPIO9/TDM2TSYN/IRQ7/ETHMDIO	G13	V_{DD}
E20	GPIO13/TDM2RCLK/IRQ11/ETHMDC	G14	IRQ7/INT_OUT
E21	GPIO10/TDM2TCLK/IRQ8/ETHRX_DV/ETHCRS_DV/NC	G15	ETHCRS/ETHRXD
E22	GPIO12/TDM2RSYN/IRQ10/ETHRXD1/ETHSYNC	G16	V_{DD}
F2	PORESET	G17	CS1
F3	RSTCONF	G18	BCTL0
F4	NMI	G19	GPIO15/TDM1TSYN/DREQ1
F5	HA29	G20	GND
F6	HA22	G21	GPIO17/TDM1TDAT/DACK1
F7	GND	G22	GPIO22/TDM0TCLK/DONE2/DRACK2
F8	V_{DD}	H2	HA20
F9	V_{DD}	H3	HA28
F10	V_{DD}	H4	V_{DD}
F11	GND	H5	HA19
F12	V_{DD}	H6	TEST
F13	GND	H7	PSDCAS/PGPL3
F14	V_{DD}	H8	PGTA/PUPMWAIT/PGPL4/PPBS
F15	ETHRX_CLK/ETHSYNC_IN	H9	V_{DD}
F16	ETHTX_CLK/ETHREF_CLK/ETHCLOCK	H10	BM1/TC1/BNKSEL1
F17	GPIO20/TDM1RDAT	H11	ARTRY
F18	GPIO18/TDM1RSYN/DREQ2	H12	AACK
F19	GPIO16/TDM1TCLK/DONE1/DRACK1	H13	DBB/IRQ5
F20	GPIO11/TDM2TDAT/IRQ9/ETHRX_ER/ETHTXD	H14	HTA
F21	GPIO14/TDM2RDAT/IRQ12/ETHRXD0/NC	H15	V_{DD}
F22	GPIO19/TDM1RCLK/DACK2	H16	TT4/CS7
G2	HA24	H17	CS4
G3	HA27	H18	GPIO24/TDM0RSYN/IRQ14
G4	HA25	H19	GPIO21/TDM0TSYN
G5	HA23	H20	V_{DD}
H21	V_{DDH}	K15	V_{DD}
H22	A31	K16	TT2/CS5
J2	HA18	K17	ALE

Table 1. MSC8126 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
T15	D23	V9	D7
T16	$\overline{\text{IRQ5}}$/DP5/$\overline{\text{DACK4}}$/$\overline{\text{EXT\_BG3}}$	V10	D10
T17	$\overline{\text{IRQ4}}$/DP4/$\overline{\text{DACK3}}$/$\overline{\text{EXT\_DBG3}}$	V11	D12
T18	$\overline{\text{IRQ1}}$/DP1/$\overline{\text{DACK1}}$/$\overline{\text{EXT\_BG2}}$	V12	D13
T19	D30	V13	D18
T20	GND	V14	D20
T21	A15	V15	GND
T22	A14	V16	D24
U2	HD16	V17	D27
U3	HD19	V18	D29
U4	HD2/DSI64	V19	A8
U5	D2	V20	A9
U6	D3	V21	A10
U7	D6	V22	A11
U8	D8	W2	HD6
U9	D9	W3	HD5/CNFGS
U10	D11	W4	HD4/MODCK2
U11	D14	W5	GND
U12	D15	W6	GND
U13	D17	W7	V_{DDH}
U14	D19	W8	V_{DDH}
U15	D22	W9	GND
U16	D25	W10	HDST1/HA10
U17	D26	W11	HDST0/HA9
U18	D28	W12	V_{DDH}
U19	D31	W13	GND
U20	V_{DDH}	W14	HD40/D40/ETHRXD0
W15	V_{DDH}	AA9	V_{DDH}
W16	HD33/D33/reserved	AA10	HD54/D54/ETHTX_EN
W17	V_{DDH}	AA11	HD52/D52
W18	HD32/D32/reserved	AA12	V_{DDH}
W19	GND	AA13	GND
W20	GND	AA14	V_{DDH}
W21	A7	AA15	HD46/D46/ETHTXT0
W22	A6	AA16	GND
Y2	HD7	AA17	HD42/D42/ETHRXD2/reserved
Y3	HD15	AA18	HD38/D38/reserved
Y4	V_{DDH}	AA19	HD35/D35/reserved
Y5	HD9	AA20	A0

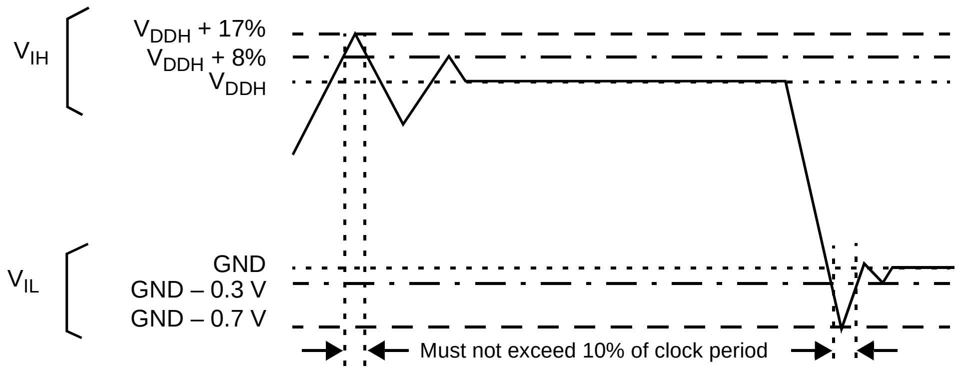


Figure 5. Overshoot/Undershoot Voltage for V_{IH} and V_{IL}

2.5 AC Timings

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs. When systems such as DSP farms are developed using the DSI, use a device loading of 4 pF per pin. AC timings are based on a 20 pF load, except where noted otherwise, and a 50 Ω transmission line. For loads smaller than 20 pF, subtract 0.06 ns per pF down to 10 pF load. For loads larger than 20 pF, add 0.06 ns for SIU/Ethernet/DSI delay and 0.07 ns for GPIO/TDM/timer delay. When calculating overall loading, also consider additional RC delay.

2.5.1 Output Buffer Impedances

Table 6. Output Buffer Impedances

Output Buffers	Typical Impedance (Ω)
System bus	50
Memory controller	50
Parallel I/O	50
Note: These are typical values at 65°C. The impedance may vary by ±25% depending on device process and operating temperature.	

2.5.2 Start-Up Timing

Starting the device requires coordination among several input sequences including clocking, reset, and power. **Section 2.5.3** describes the clocking characteristics. **Section 2.5.4** describes the reset and power-up characteristics. You must use the following guidelines when starting up an MSC8126 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the power-up sequence. See **Table 11** for timing.
- If possible, bring up the V_{DD} and V_{DDH} levels together. For designs with separate power supplies, bring up the V_{DD} levels and then the V_{DDH} levels (see **Figure 7**).
- CLKIN should start toggling at least 16 cycles (starting after V_{DDH} reaches its nominal level) before $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation (see **Figure 6** and **Figure 7**).
- CLKIN must not be pulled high during V_{DDH} power-up. CLKIN can toggle during this period.

Note: See **Section 3.1** for start-up sequencing recommendations and **Section 3.2** for power supply design recommendations.

The following figures show acceptable start-up sequence examples. **Figure 6** shows a sequence in which V_{DD} and V_{DDH} are raised together. **Figure 7** shows a sequence in which V_{DDH} is raised after V_{DD} and CLKIN begins to toggle as V_{DDH} rises.

Table 11. Reset Actions for Each Reset Source

Reset Action/Reset Source	Power-On Reset (PORESET)	Hard Reset (HRESET)	Soft Reset (SRESET)	
	External only	External or Internal (Software Watchdog or Bus Monitor)	External	JTAG Command: EXTEST, CLAMP, or HIGHZ
Configuration pins sampled (Refer to **Section 2.5.4.1** for details).	Yes	No	No	No
SPLL state reset	Yes	No	No	No
System reset configuration write through the DSI	Yes	No	No	No
System reset configuration write though the system bus	Yes	Yes	No	No
HRESET driven	Yes	Yes	No	No
SIU registers reset	Yes	Yes	No	No
IPBus modules reset (TDM, UART, Timers, DSI, IPBus master, GIC, HS, and GPIO)	Yes	Yes	Yes	Yes
SRESET driven	Yes	Yes	Yes	Depends on command
SC140 extended cores reset	Yes	Yes	Yes	Yes
MQBS reset	Yes	Yes	Yes	Yes

2.5.4.1 Power-On Reset (PORESET) Pin

Asserting PORESET initiates the power-on reset flow. PORESET must be asserted externally for at least 16 CLKIN cycles after V_{DD} and V_{DDH} are both at their nominal levels.

2.5.4.2 Reset Configuration

The MSC8126 has two mechanisms for writing the reset configuration:

- Through the direct slave interface (DSI)
- Through the system bus. When the reset configuration is written through the system bus, the MSC8126 acts as a configuration master or a configuration slave. If configuration slave is selected, but no special configuration word is written, a default configuration word is applied.

Fourteen signal levels (see **Chapter 1** for signal description details) are sampled on PORESET deassertion to define the Reset Configuration Mode and boot and operating conditions:

- RSTCONF
- CNFGS
- DSISYNC
- DSI64
- CHIP_ID[0–3]
- BM[0–2]
- SWTE
- MODCK[1–2]

2.5.4.3 Reset Timing Tables

Table 12 and **Figure 9** describe the reset timing for a reset configuration write through the direct slave interface (DSI) or through the system bus.

Table 12. Timing for a Reset Configuration Write through the DSI or System Bus

No.	Characteristics	Expression	Min	Max	Unit
1	Required external PORESET duration minimum • CLKIN = 20 MHz • CLKIN = 133 MHz (400 MHz core) • CLKIN = 166 MHz (500 MHz core)	16/CLKIN	 800 120 96	 800 — —	 ns ns ns
2	Delay from deassertion of external PORESET to deassertion of internal PORESET • CLKIN = 20 MHz to 166 MHz	1024/CLKIN	6.17	51.2	µs
3	Delay from de-assertion of internal PORESET to SPLL lock • CLKIN = 20 MHz (RDF = 1) • CLKIN = 133 MHz (RDF = 2) (400 MHz core) • CLKIN = 166 MHz (RDF = 2) (500 MHz core)	6400/(CLKIN/RDF) (PLL reference clock-division factor)	 320 96 77	 320 96 77	 µs µs µs
5	Delay from SPLL to HRESET deassertion • REFCLK = 40 MHz to 166 MHz	512/REFCLK	3.08	12.8	µs
6	Delay from SPLL lock to SRESET deassertion • REFCLK = 40 MHz to 166 MHz	515/REFCLK	3.10	12.88	µs
7	Setup time from assertion of RSTCONF, CNFGS, DSISYNC, DSI64, CHIP_ID[0–3], BM[0–2], SWTE, and MODCK[1–2] before deassertion of PORESET		3	—	ns
8	Hold time from deassertion of PORESET to deassertion of RSTCONF, CNFGS, DSISYNC, DSI64, CHIP_ID[0–3], BM[0–2], SWTE, and MODCK[1–2]		5	—	ns
Note:	Timings are not tested, but are guaranteed by design.				

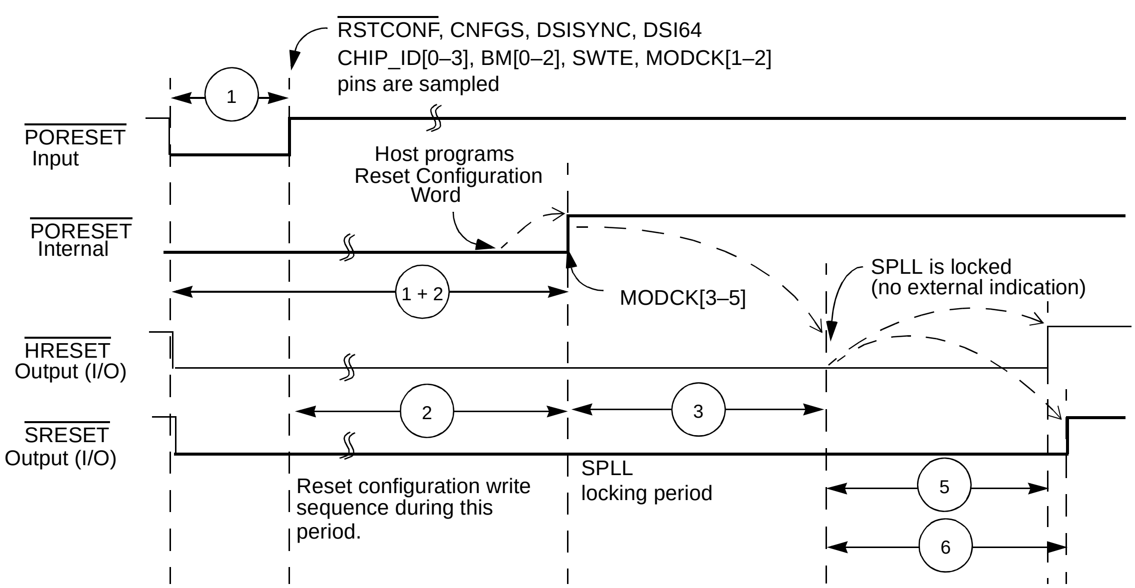


Figure 9. Timing Diagram for a Reset Configuration Write

The UPM machine and GPCM machine outputs change on the internal tick selected by the memory controller configuration. The AC timing specifications are relative to the internal tick. SDRAM machine outputs change only on the REFCLK rising edge.

Table 14. AC Timing for SIU Inputs

No.	Characteristic	Value for Bus Speed in MHz			Units
		Ref = CLKIN		Ref = CLKOUT	
		133	166	133	
10	Hold time for all signals after the 50% level of the REFCLK rising edge	0.5	0.5	0.5	ns
11a	$\overline{ARTRY}$/$\overline{ABB}$ set-up time before the 50% level of the REFCLK rising edge	3.0	3.0	3.0	ns
11b	$\overline{DBG}$/$\overline{DBB}$/$\overline{BG}$/$\overline{BR}$/$\overline{TC}$ set-up time before the 50% level of the REFCLK rising edge	3.3	3.3	3.3	ns
11c	$\overline{AACK}$ set-up time before the 50% level of the REFCLK rising edge	2.9	2.9	2.9	ns
11d	$\overline{TA}$/$\overline{TEA}$/$\overline{PSDVAL}$ set-up time before the 50% level of the REFCLK rising edge • Data-pipeline mode • Non-pipeline mode	 3.4 4.0	 3.4 4.0	 3.4 4.0	 ns ns
12	Data bus set-up time before REFCLK rising edge in Normal mode • Data-pipeline mode • Non-pipeline mode	 1.8 4.0	 1.7 4.0	 1.8 4.0	 ns ns
13[1]	Data bus set-up time before the 50% level of the REFCLK rising edge in ECC and PARITY modes • Data-pipeline mode • Non-pipeline mode	 2.0 7.3	 2.0 7.3	 2.0 7.3	 ns ns
14[1]	DP set-up time before the 50% level of the REFCLK rising edge • Data-pipeline mode • Non-pipeline mode	 2.0 6.1	 2.0 6.1	 2.0 6.1	 ns ns
15a	$\overline{TS}$ and Address bus set-up time before the 50% level of the REFCLK rising edge • Extra cycle mode (SIUBCR[EXDD] = 0) • No extra cycle mode (SIUBCR[EXDD] = 1)	 3.6 5.0	 3.6 5.0	 3.8 5.0	 ns ns
15b	Address attributes: TT/$\overline{TBST}$/TSZ/$\overline{GBL}$ set-up time before the 50% level of the REFCLK rising edge • Extra cycle mode (SIUBCR[EXDD] = 0) • No extra cycle mode (SIUBCR[EXDD] = 1)	 3.5 4.4	 3.5 4.4	 3.5 4.4	 ns ns
16	PUPMWAIT signal set-up time before the 50% level of the REFCLK rising edge	3.7	3.7	3.7	ns
17	$\overline{IRQx}$ setup time before the 50% level; of the REFCLK rising edge[3]	4.0	4.0	4.0	ns
18	$\overline{IRQx}$ minimum pulse width[3]	6.0 + T_{REFCLK}	6.0 + T_{REFCLK}	6.0 + T_{REFCLK}	ns

Notes:
1. Timings specifications 13 and 14 in non-pipeline mode are more restrictive than MSC8102 timings.
2. Values are measured from the 50% TTL transition level relative to the 50% level of the REFCLK rising edge.
3. Guaranteed by design

Table 15. AC Timing for SIU Outputs

No.	Characteristic	Value for Bus Speed in MHz			Units
		Ref = CLKIN		Ref = CLKOUT	
		133	166	133	
30[2]	Minimum delay from the 50% level of the REFCLK for all signals	0.8	0.8	1.0	ns

2.5.6.2 DSI Synchronous Mode

Table 19. DSI Inputs—Synchronous Mode

No.	Characteristic	Expression	Min	Max	Units
120	HCLKIN Cycle Time[1, 2]	HTC	10.0	55.6	ns
121	HCLKIN high Pulse Width	(0.5 ± 0.1) × HTC	4.0	33.3	ns
122	HCLKIN low Pulse Width	(0.5 ± 0.1) × HTC	4.0	33.3	ns
123	HA[11–29] inputs set-up time	—	1.2	—	ns
124	HD[0–63] inputs set-up time	—	0.4	—	ns
125	HCID[0–4] inputs set-up time	—	1.3	—	ns
126	All other inputs set-up time	—	1.2	—	ns
127	All inputs hold time	—	1.5	—	ns

Notes:
1. Values are based on a frequency range of 18–100 MHz.
2. Refer to **Table 7** for HCLKIN frequency limits.

Table 20. DSI Outputs—Synchronous Mode

No.	Characteristic	Min	Max	Units
128	HCLKIN high to HD[0–63] output active	2.0	—	ns
129	HCLKIN high to HD[0–63] output valid	—	6.3	ns
130	HD[0–63] output hold time	1.7	—	ns
131	HCLKIN high to HD[0–63] output high impedance	—	7.6	ns
132	HCLKIN high to $\overline{HTA}$ output active	2.0	—	ns
133	HCLKIN high to $\overline{HTA}$ output valid	—	5.9	ns
134	$\overline{HTA}$ output hold time	1.7	—	ns
135	HCLKIN high to $\overline{HTA}$ high impedance	—	6.3	ns

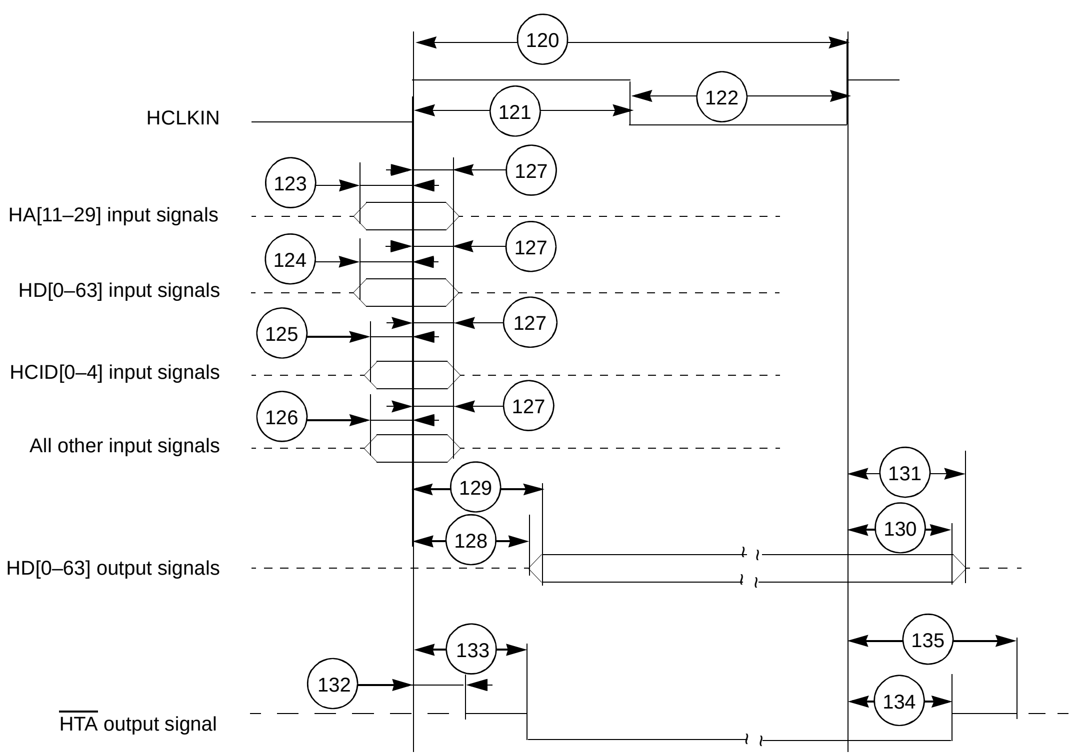


Figure 17. DSI Synchronous Mode Signals Timing Diagram

2.5.7 TDM Timing

Table 21. TDM Timing

No.	Characteristic	Expression	Ref = CLKIN		Units
			Min	Max	
300	TDMxRCLK/TDMxTCLK	TC[1]	16	—	ns
301	TDMxRCLK/TDMxTCLK high pulse width	(0.5 ± 0.1) × TC	7	—	ns
302	TDMxRCLK/TDMxTCLK low pulse width	(0.5 ± 0.1) × TC	7	—	ns
303	TDM receive all input set-up time		1.3	—	ns
304	TDM receive all input hold time		1.0	—	ns
305	TDMxTCLK high to TDMxTDAT/TDMxRCLK output active[2,3]		2.8	—	ns
306	TDMxTCLK high to TDMxTDAT/TDMxRCLK output valid[2,3]		—	8.8	ns
307	All output hold time[5]		2.5	—	ns
308	TDMxTCLK high to TDmXTDAT/TDMxRCLK output high impedance[2,3]		—	10.5	ns
309	TDMxTCLK high to TDMXTSYN output valid[2]		—	8.5	ns
310	TDMxTSYN output hold time[5]		2.5	—	ns

Notes:
1. Values are based on a a maximum frequency of 62.5 MHz. The TDM interface supports any frequency below 62.5 MHz.
2. Values are based on 20 pF capacitive load.
3. When configured as an output, TDMxRCLK acts as a second data link. See the *MSC8126 Reference Manual* for details.
4. CLKOUT synchronization is not supported for cores operating at above 400 MHz.
5. Values are based on 10 pF capacitive load.

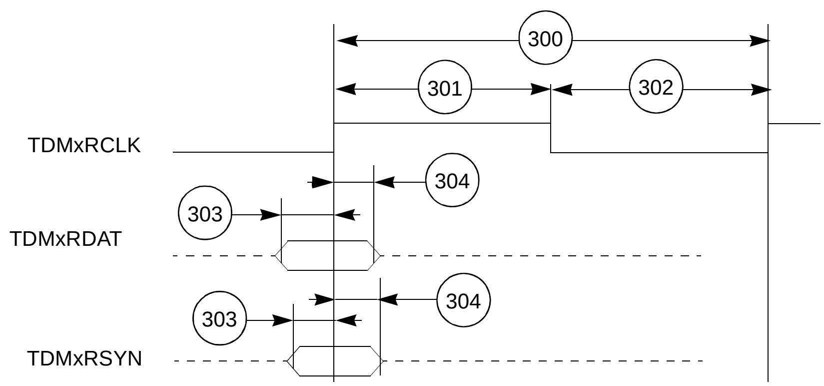


Figure 18. TDM Inputs Signals

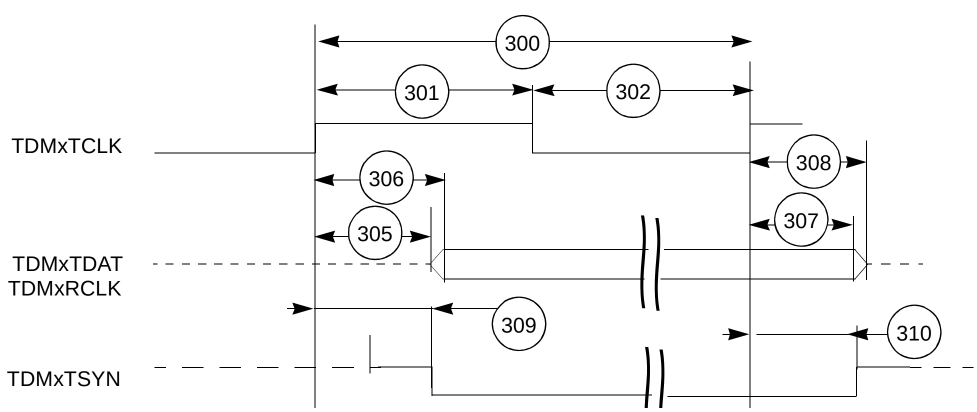


Figure 19. TDM Output Signals

2.5.9 Timer Timing

Table 23. Timer Timing

No.	Characteristics	Ref = CLKIN		Unit
		Min	Max	
500	TIMERx frequency	10.0	—	ns
501	TIMERx Input high period	4.0	—	ns
502	TIMERx Output low period	4.0	—	ns
503	TIMERx Propagations delay from its clock input • 1.1 V core • 1.2 V core	 3.1 2.8	 9.5 8.1	 ns ns

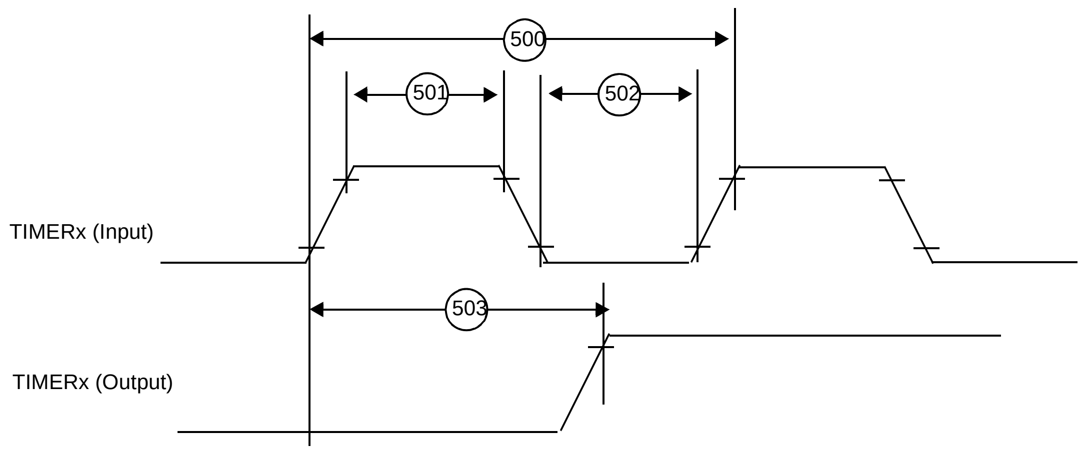


Figure 22. Timer Timing

2.5.10 Ethernet Timing

2.5.10.1 Management Interface Timing

Table 24. Ethernet Controller Management Interface Timing

No.	Characteristics	Min	Max	Unit
801	ETHMDIO to ETHMDC rising edge set-up time	10	—	ns
802	ETHMDC rising edge to ETHMDIO hold time	10	—	ns

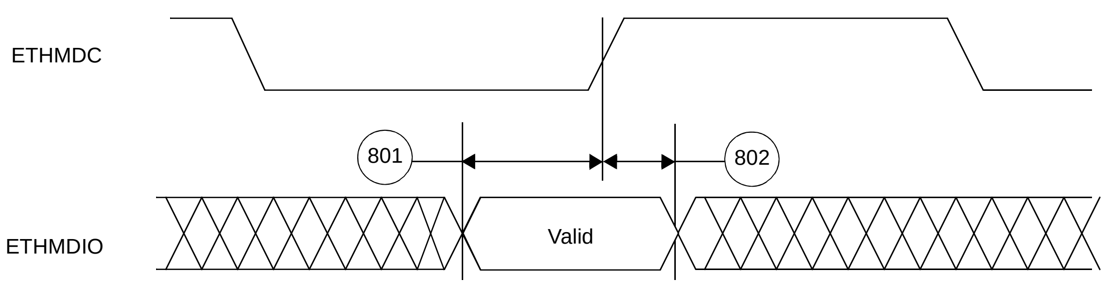


Figure 23. MDIO Timing Relationship to MDC

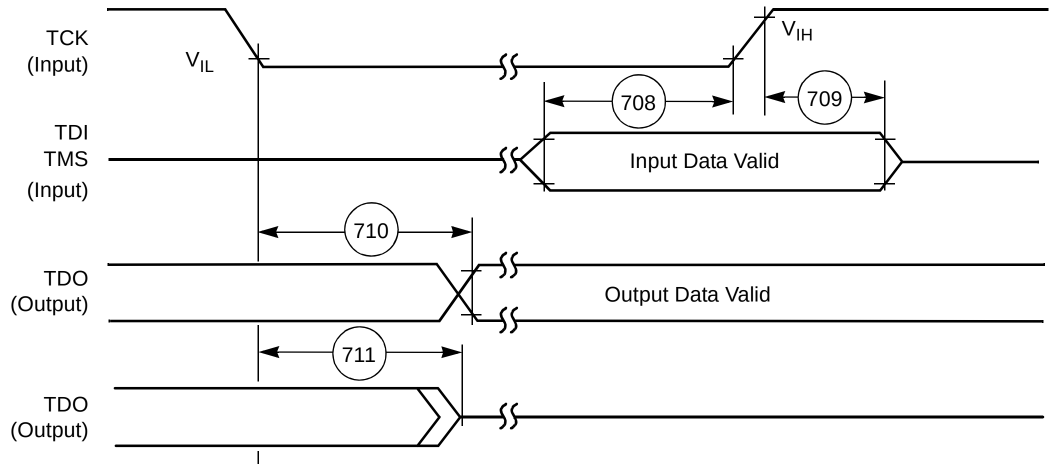


Figure 31. Test Access Port Timing Diagram

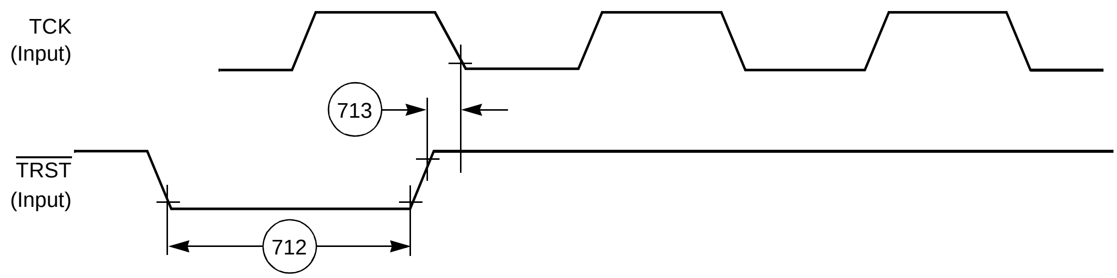


Figure 32. $\overline{\text{TRST}}$ Timing Diagram

3 Hardware Design Considerations

The following sections discuss areas to consider when the MSC8126 device is designed into a system.

3.1 Start-up Sequencing Recommendations

Use the following guidelines for start-up and power-down sequences:

- Assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ before applying power and keep the signals driven low until the power reaches the required minimum power levels. This can be implemented via weak pull-down resistors.
- CLKIN can be held low or allowed to toggle during the beginning of the power-up sequence. However, CLKIN must start toggling before the deassertion of $\overline{\text{PORESET}}$ and after both power supplies have reached nominal voltage levels.
- If possible, bring up V_{DD}/V_{CCSYN} and V_{DDH} together. If it is not possible, raise V_{DD}/V_{CCSYN} first and then bring up V_{DDH}. V_{DDH} should not exceed V_{DD}/V_{CCSYN} until V_{DD}/V_{CCSYN} reaches its nominal voltage level. Similarly, bring both voltage levels down together. If that is not possible reverse the power-up sequence, with V_{DDH} going down first and then V_{DD}/V_{CCSYN}.

Note: This recommended power sequencing for the MSC8126 is different from the MSC8102. See **Section 2.5.2** for start-up timing specifications.

External voltage applied to any input line must not exceed the I/O supply V_{DDH} by more than 0.8 V at any time, including during power-up. Some designs require pull-up voltages applied to selected input lines during power-up for configuration purposes. This is an acceptable exception to the rule. However, each such input can draw up to 80 mA per input pin per device in the system during start-up.

During the power-up sequence, if V_{DD} rises before V_{DDH} (see **Figure 6**), current can pass from the V_{DD} supply through the device ESD protection circuits to the V_{DDH} supply. The ESD protection diode can allow this to occur when V_{DD} exceeds V_{DDH} by more than 0.8 V. Design the power supply to prevent or minimize this effect using one of the following optional methods:

- Never allow V_{DD} to exceed V_{DDH} + 0.8V.
- Design the V_{DDH} supply to prevent reverse current flow by adding a minimum 10 Ω resistor to GND to limit the current. Such a design yields an initial V_{DDH} level of V_{DD} – 0.8 V before it is enabled.

After power-up, V_{DDH} must not exceed V_{DD}/V_{CCSYN} by more than 2.6 V.

3.2 Power Supply Design Considerations

When used as a drop-in replacement in MSC8102 applications or when implementing a new design, use the guidelines described in *Migrating Designs from the MSC8102 to the MSC8122* (AN2716) and the *MSC8126 Design Checklist* (AN3374 for optimal system performance. *MSC8122 and MSC8126 Power Circuit Design Recommendations and Examples* (AN2937) provides detailed design information. See **Section 2.5.2** for start-up timing specifications.

Figure 33 shows the recommended power decoupling circuit for the core power supply. The voltage regulator and the decoupling capacitors should supply the required device current without any drop in voltage on the device pins. The voltage on the package pins should not drop below the minimum specified voltage level even for a very short spikes. This can be achieved by using the following guidelines:

- For the core supply, use a voltage regulator rated at 1.2 V with nominal rating of at least 3 A. This rating does not reflect actual average current draw, but is recommended because it resists changes imposed by transient spikes and has better voltage recovery time than supplies with lower current ratings.

- Decouple the supply using low-ESR capacitors mounted as close as possible to the socket. **Figure 33** shows three capacitors in parallel to reduce the resistance. Three capacitors is a recommended minimum number. If possible, mount at least one of the capacitors directly below the MSC8126 device.

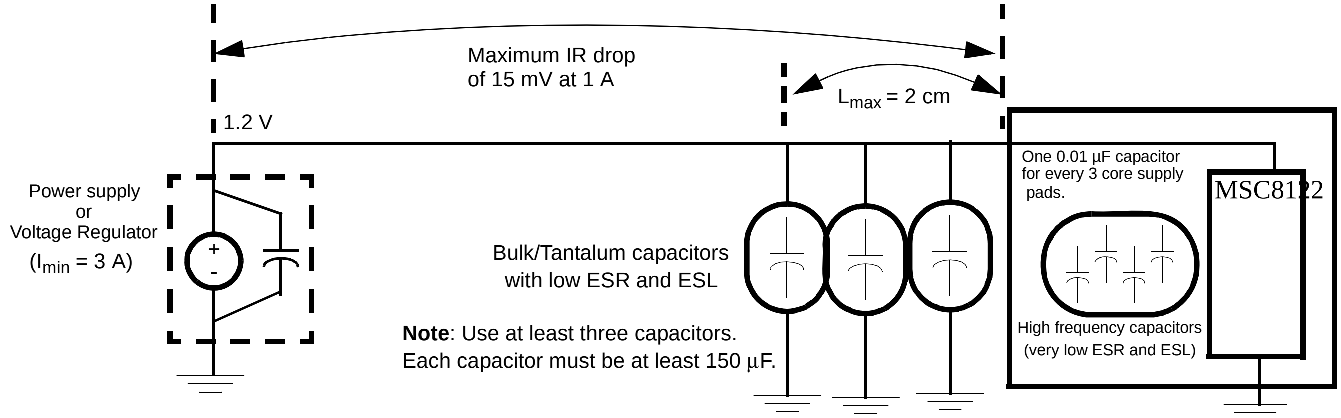


Figure 33. Core Power Supply Decoupling

Each V_{CC} and V_{DD} pin on the MSC8126 device should have a low-impedance path to the board power supply. Similarly, each GND pin should have a low-impedance path to the ground plane. The power supply pins drive distinct groups of logic on the chip. The V_{CC} power supply should have at least four 0.1 µF by-pass capacitors to ground located as closely as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC}, V_{DD}, and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MSC8126 have fast rise and fall times. PCB trace interconnection length should be minimized to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PCB trace lengths of six inches are recommended. For the DSI control signals in synchronous mode, ensure that the layout supports the DSI AC timing requirements and minimizes any signal crosstalk. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PCB traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC}, V_{DD}, and GND circuits. Pull up all unused inputs or signals that will be inputs during reset.

Special care should be taken to minimize the noise levels on the PLL supply pins. There is one pair of PLL supply pins: V_{CCSYN}-GND_{SYN}. To ensure internal clock stability, filter the power to the V_{CCSYN} input with a circuit similar to the one in **Figure 34**. For optimal noise filtering, place the circuit as close as possible to V_{CCSYN}. The 0.01-µF capacitor should be closest to V_{CCSYN}, followed by the 10-µF capacitor, the 10-nH inductor, and finally the 10-Ω resistor to V_{DD}. These traces should be kept short and direct. Provide an extremely low impedance path to the ground plane for GND_{SYN}. Bypass GND_{SYN} to V_{CCSYN} by a 0.01-µF capacitor located as close as possible to the chip package. For best results, place this capacitor on the backside of the PCB aligned with the depopulated void on the MSC8126 located in the square defined by positions, L11, L12, L13, M11, M12, M13, N11, N12, and N13.

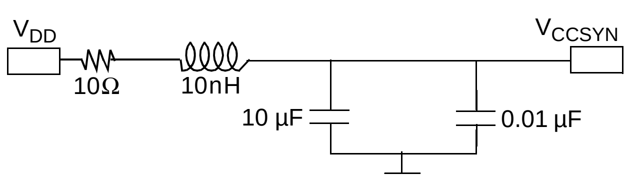


Figure 34. V_{CCSYN} Bypass

3.3 Connectivity Guidelines

Unused output pins can be disconnected, and unused input pins should be connected to the non-active value, via resistors to V_{DDH} or GND, except for the following:

- If the DSI is unused (DDR[DSIDIS] is set), HCS and HBCS must pulled up and all the rest of the DSI signals can be disconnected.
- When the DSI uses synchronous mode, HTA must be pulled up. In asynchronous mode, HTA should be pulled either up or down, depending on design requirements.
- HDST can be disconnected if the DSI is in big-endian mode, or if the DSI is in little-endian mode and the DCR[DSRFA] bit is set.
- When the DSI is in 64-bit data bus mode and DCR[BEM] is cleared, pull up HWBS[1–3]/HDBS[1–3]/HWBE[1–3]/HDBE[1–3] and HWBS[4–7]/HDBS[4–7]/HWBE[4–7]/HDBE[4–7]/PWE[4–7]/PSDDQM[4–7]/PBS[4–7].
- When the DSI is in 32-bit data bus mode and DCR[BEM] is cleared, HWBS[1–3]/HDBS[1–3]/HWBE[1–3]/HDBE[1–3] must be pulled up.
- When the DSI is in asynchronous mode, HBRST and HCLKIN should either be disconnected or pulled up.
- When the DSI uses sliding window address mode (DCR[SLDWA] = 1), the external HA[11–13] signals must be connected (tied) to the correct voltage levels so that the host can perform the first access to the DCR. After reset, the DSI expects full address mode (DCR[SLDWA] = 0). The DCR address in the DSI memory map is 0x1BE000, which requires the following connections:
  - — HA11 must be pulled high (1)
  - — HA12 must be pulled high (1)
  - — HA13 must be pulled low (0)
- The following signals must be pulled up: HRESET, SRESET, ARTRY, TA, TEA, PSDVAL, and AACK.
- In single-master mode (BCR[EBM] = 0) with internal arbitration (PPC_ACR[EARB] = 0):
  - — BG, DBG, and TS can be left unconnected.
  - — EXT_BG[2–3], EXT_DBG[2–3], and GBL can be left unconnected if they are multiplexed to the system bus functionality. For any other functionality, connect the signal lines based on the multiplexed functionality.
  - — BR must be pulled up.
  - — EXT_BR[2–3] must be pulled up if multiplexed to the system bus functionality.
- If there is an external bus master (BCR[EBM] = 1):
  - — BR, BG, DBG, and TS must be pulled up.
  - — EXT_BR[2–3], EXT_BG[2–3], and EXT_DBG[2–3] must be pulled up if multiplexed to the system bus functionality.
- In single-master mode, ABB and DBB can be selected as IRQ inputs and be connected to the non-active value. In other modes, they must be pulled up.

Note: The MSC8126 does not support DLL-enabled mode. For the following two clock schemes, ensure that the DLL is disabled (that is, the DLLDIS bit in the Hard Reset Configuration Word is set).

- If no system synchronization is required (for example, the design does not use SDRAM), you can use any of the available clock modes.
- In the CLKIN synchronization mode, use the following connections:
  - — Connect the oscillator output through a buffer to CLKIN.
  - — Connect the CLKIN buffer output to the slave device (for example, SDRAM) making sure that the delay path between the clock buffer to the MSC8126 and the SDRAM is equal (that is, has a skew less than 100 ps).
  - — Valid clock modes in this scheme are: 0, 7, 15, 19, 21, 23, 28, 29, 30, and 31.
- In CLKOUT synchronization mode (for 1.2 V devices), CLKOUT is the main clock to SDRAM. Use the following connections:
  - — Connect the oscillator output through a buffer to CLKIN.
  - — Connect CLKOUT through a zero-delay buffer to the slave device (for example, SDRAM) using the following guidelines:
    - – The maximum delay between the slave and CLKOUT must not exceed 0.7 ns.

5 Package Information

Notes:
1. All dimensions in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M–1994.
3. Features are symmetrical about the package center lines unless dimensioned otherwise.
4. Maximum solder ball diameter measured parallel to Datum A.
5. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
6. Parallelism measurement shall exclude any effect of mark on top surface of package.
7. Capacitors may not be present on all devices.
8. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
9. FC CBGA (Ceramic) package code: 5238.
FC PBGA (Plastic) package code: 5263.
10. Pin 1 indicator can be in the form of number 1 marking or an "L" shape marking.

Figure 35. MSC8126 Mechanical Information, 431-pin FC-PBGA Package

6 Product Documentation

- *MSC8126 Technical Data Sheet* (MSC8126). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8126 device.
- *MSC8126 Reference Manual* (MSC8126RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes*. Cover various programming topics related to the StarCore DSP core and the MSC8126 device.
- *SC140 DSP Core Reference Manual*. Covers the SC140 core architecture, control registers, clock registers, program control, and instruction set.

7 Revision History

Table 31 provides a revision history for this data sheet.

Table 31. Document Revision History

Revision	Date	Description
0	May 2004	• Initial release.
1	Jun. 2004	• Updated timing number 32b. • Updated DSI timing specifications.
2	Sep 2004	• New orderable parts added with other core voltage and temperature options. • Updated thermal characteristics. • In Table 2-14, removed references to 30 pF. • Design guidelines and layout recommendations updated.
3	Nov. 2004	• Added 500 MHz core and 166 MHz bus speed options. • Definitions of GPIO[27–28] updated. • Bus, TDM, and GPIO timing updated. I^2C timing changed to GPIO timing. • GPIO[27–28] connections updated. MWBEn replaced with correct name HWBEn. • Design guidelines update.
4	Jan. 2005	• Package type changed to FC-PBGA for all frequencies. • Low-voltage 300 MHz power changed to 1.1 V. • $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ definitions updated. • Undershoot and overshoot values added for V_{DDH}. • RMII timing updated. • Design guidelines updated and reorganized.
5	May 2005	• Multiple AC timing specifications updated.
6	May 2005	• Multiple AC timing specifications updated.
7	Jul. 2005	• Multiple AC timing specifications updated.
8	Jul. 2005	• AC specification table layout modified.
9	Sep. 2005	• ETHTX_EN type and $\overline{\text{TRST}}$ description updated. • Package drawing updated. • Clock specifications updated. • Start-up sequence updated.
10	Oct 2005	• V_{DDH} + 10% changed to V_{DDH} + 8% in **Figure 2-1**. • V_{DDH} +20% changed to V_{DDH} + 17% in **Figure 2-1**.
11	Apr 2006	• Reset timing updated to reflect actual values in **Table 2-11**.
12	Oct. 2006	• Added new timings 17 and 18 for IRQ set time and pulse width in **Table 2-13**
13	Dec. 2007	• Converted to new data sheet format. • Added PLL supply current to **Table 5** in **Section 2.4**. • Modified **Figure 5** in **Section 2.4** to make it clear that the time limits for undershoot referred to values below –0.3 V and not GND. • Added cross-references between **Sections 2.5.2** and **Section 3.1** and **3.2**. • Added power-sequence guidelines to **Sections 2.5.2**. • Added CLKIN jitter characteristic specifications to Table 9. • Added additional guidelines to prevent reverse current to **Section 3.1**. • Added connectivity guidelines for DSI in sliding windows mode to **Section 3.3**.
14	May 2008	• Changed V_{IL} maximum and reference value to 0.8 V in **Table 5**.
15	Dec 2008	• Clarified the wording of note 2 in **Table 15** on p. 24.

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