


## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Obsolete |
| Type | SC140 Core |
| Interface | DSI, Ethernet, RS-232 |
| Clock Rate | 400MHz |
| Non-Volatile Memory | External |
| On-Chip RAM | 1.436MB |
| Voltage - I/O | 3.30V |
| Voltage - Core | 1.20V |
| Operating Temperature | -40°C ~ 105°C (TJ) |
| Mounting Type | Surface Mount |
| Package / Case | 431-BFBGA, FCBGA |
| Supplier Device Package | 431-FCPBGA (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8126tmp6400 |

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# 1 Pin Assignments

This section includes diagrams of the MSC8126 package ball grid array layouts and pinout allocation tables.

## 1.1 FC-PBGA Ball Layout Diagrams

Top and bottom views of the FC-PBGA package are shown in **Figure 3** and **Figure 4** with their ball location index numbers.

Bottom View

| | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B | GND | $V_{DD}$ | $V_{DD}$ | GPIO0 | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | $\overline{\text{NMI}}$ OUT | GND | GND | $V_{DD}$ | |
| C | GPIO6 | GPIO5 | GPIO3 | GPIO7 | GPIO1 | GPIO2 | GPIO30 | GND | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | HCID1 | GPIO28 | $\overline{\text{S}}$ RESET | TDO | $V_{DD}$ | GND |
| D | GPIO8 | GND | $V_{DDH}$ | GPIO4 | $V_{DDH}$ | GPIO29 | GPIO31 | $V_{DD}$ | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | HCID3 | HCID2 | $V_{DDH}$ | GND | EE1 | EE0 | TDI |
| E | GPIO12 | GPIO10 | GPIO13 | GPIO9 | GND | GND | $V_{DD}$ | GND | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | HCID0 | GPIO27 | $\overline{\text{HRESET}}$ | TMS | $\overline{\text{TRST}}$ | TCK |
| F | GPIO19 | GPIO14 | GPIO11 | GPIO16 | GPIO18 | GPIO20 | ETHTX_CLK | ETHRX_CLK | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | GND | HA22 | HA29 | $\overline{\text{NMI}}$ | $\overline{\text{RST}}$ CONF | $\overline{\text{PO}}$ RESET |
| G | GPIO22 | GPIO17 | GND | GPIO15 | $\overline{\text{BCTL0}}$ | $\overline{\text{CS1}}$ | $V_{DD}$ | ETHCRS | $\overline{\text{INT}}$ OUT | $V_{DD}$ | $\overline{\text{ABB}}$ | BM0 | BADDR31 | $V_{DD}$ | $V_{DD}$ | $\overline{\text{PWE0}}$ | HA17 | HA23 | HA25 | HA27 | HA24 |
| H | A31 | $V_{DDH}$ | $V_{DD}$ | GPIO21 | GPIO24 | $\overline{\text{CS4}}$ | TT4 | $V_{DD}$ | $\overline{\text{HTA}}$ | $\overline{\text{DBB}}$ | $\overline{\text{AACK}}$ | $\overline{\text{ARTRY}}$ | BM1 | $V_{DD}$ | $\overline{\text{PGTA}}$ | $\overline{\text{PSD}}$ CAS | TEST | HA19 | $V_{DD}$ | HA28 | HA20 |
| J | A30 | GPIO25 | GND | GPIO23 | BCTL1 | PSDA10 | TT3 | $V_{DD}$ | GND | $V_{DD}$ | $\overline{\text{DBG}}$ | BM2 | CLKIN | $V_{DD}$ | BADDR27 | PSDA MUX | GND | HA13 | $V_{DD}$ | HA26 | HA18 |
| K | A28 | A29 | A26 | GND | $\overline{\text{CS2}}$ | ALE | TT2 | $V_{DD}$ | CLKOUT | GND | GND | GND | GND | Res. | BADDR30 | $\overline{\text{POE}}$ | $\overline{\text{PWE1}}$ | $\overline{\text{PWE3}}$ | HA16 | HA21 | HA15 |
| L | A22 | A25 | A27 | $V_{DDH}$ | $\overline{\text{CS3}}$ | GND | GND | $V_{DDH}$ | GND | | | | GND | GND | BADDR29 | BADDR28 | $V_{DDH}$ | $V_{DDH}$ | HA11 | HA14 | HA12 |
| M | A21 | A24 | $V_{DDH}$ | GND | $V_{DDH}$ | $V_{DDH}$ | $\overline{\text{HB}}$ RST | $V_{DDH}$ | GND | | MSC8126 | | GND | $V_{DDH}$ | $V_{DD}$ | $V_{DDH}$ | GND | GND | $V_{DDH}$ | HD31 | HD28 |
| N | A20 | A23 | GPIO26 | $\overline{\text{PSDWE}}$ | $\overline{\text{CS0}}$ | $\overline{\text{HCS}}$ | $\overline{\text{BG}}$ | $\overline{\text{HRDS}}$ | GND | | | | GND | $\overline{\text{HBCS}}$ | $\overline{\text{HWBS}}$ 0 | $V_{DDH}$ | $\overline{\text{PWE2}}$ | HD24 | HD29 | HD30 | HD26 |
| P | A19 | GND | $V_{DDH}$ | DP0 | $\overline{\text{PSD}}$ VAL | $\overline{\text{TEA}}$ | $\overline{\text{BR}}$ | $\overline{\text{TA}}$ | GND | GND | $V_{CCSYN}$ | $GND_{SYN}$ | GND | HCLKIN | $\overline{\text{HWBS}}$ 1 | $\overline{\text{HWBS}}$ 2 | $\overline{\text{HWBS}}$ 3 | HD23 | HD25 | HD27 | HD20 |
| R | A16 | A18 | A17 | DP2 | $\overline{\text{TS}}$ | DP3 | DP6 | DP7 | TT0 | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $\overline{\text{GBL}}$ | TSZ3 | TSZ1 | $\overline{\text{HWBS}}$ 4 | $\overline{\text{HWBS}}$ 6 | HD22 | GND | $V_{DDH}$ | HD18 |
| T | A14 | A15 | GND | D30 | DP1 | DP4 | DP5 | D23 | D21 | TT1 | D16 | $V_{DD}$ | $\overline{\text{TBST}}$ | TSZ2 | TSZ0 | $\overline{\text{HWBS}}$ 5 | $\overline{\text{HWBS}}$ 7 | HD0 | HD1 | HD21 | HD17 |
| U | A13 | A12 | $V_{DDH}$ | D31 | D28 | D26 | D25 | D22 | D19 | D17 | D15 | D14 | D11 | D9 | D8 | D6 | D3 | D2 | HD2 | HD19 | HD16 |
| V | A11 | A10 | A9 | A8 | D29 | D27 | D24 | GND | D20 | D18 | D13 | D12 | D10 | D7 | D5 | D4 | D1 | D0 | GND | $V_{DDH}$ | HD3 |
| W | A6 | A7 | GND | GND | HD32 | $V_{DDH}$ | HD33 | $V_{DDH}$ | HD40 | GND | $V_{DDH}$ | HDST0 | HDST1 | GND | $V_{DDH}$ | $V_{DDH}$ | GND | GND | HD4 | HD5 | HD6 |
| Y | A5 | A4 | $V_{DDH}$ | HD34 | HD37 | GND | $V_{DDH}$ | GND | HD43 | $V_{DDH}$ | GND | HD51 | $V_{DDH}$ | GND | HD58 | HD60 | $V_{DD}$ | HD9 | $V_{DDH}$ | HD15 | HD7 |
| AA | A3 | A2 | A0 | HD35 | HD38 | HD42 | GND | HD46 | $V_{DDH}$ | GND | $V_{DDH}$ | HD52 | HD54 | $V_{DDH}$ | GND | HD59 | HD63 | HD10 | HD12 | HD14 | $V_{DD}$ |
| AB | $V_{DD}$ | A1 | HD36 | HD39 | HD41 | HD44 | HD45 | HD47 | HD48 | HD49 | HD50 | HD53 | HD55 | HD56 | HD57 | HD61 | HD62 | HD8 | HD11 | HD13 | GND |

**Figure 4. MSC8126 Package, Bottom View**

**Table 1. MSC8126 Signal Listing by Ball Designator (continued)**

| Des. | Signal Name | Des. | Signal Name |
|---|---|---|---|
| J3 | HA26 | K18 | $\overline{\text{CS2}}$ |
| J4 | $V_{DD}$ | K19 | GND |
| J5 | HA13 | K20 | A26 |
| J6 | GND | K21 | A29 |
| J7 | PSDAMUX/PGPL5 | K22 | A28 |
| J8 | BADDR27 | L2 | HA12 |
| J9 | $V_{DD}$ | L3 | HA14 |
| J10 | CLKIN | L4 | HA11 |
| J11 | BM2/TC2/BNKSEL2 | L5 | $V_{DDH}$ |
| J12 | $\overline{\text{DBG}}$ | L6 | $V_{DDH}$ |
| J13 | $V_{DD}$ | L7 | BADDR28 |
| J14 | GND | L8 | $\overline{\text{IRQ5}}$/BADDR29 |
| J15 | $V_{DD}$ | L9 | GND |
| J16 | TT3/$\overline{\text{CS6}}$ | L10 | GND |
| J17 | PSDA10/PGPL0 | L14 | GND |
| J18 | $\overline{\text{BCTL1}}$/$\overline{\text{CS5}}$ | L15 | $V_{DDH}$ |
| J19 | GPIO23/TDM0TDAT/$\overline{\text{IRQ13}}$ | L16 | GND |
| J20 | GND | L17 | GND |
| J21 | GPIO25/TDM0RCLK/$\overline{\text{IRQ15}}$ | L18 | $\overline{\text{CS3}}$ |
| J22 | A30 | L19 | $V_{DDH}$ |
| K2 | HA15 | L20 | A27 |
| K3 | HA21 | L21 | A25 |
| K4 | HA16 | L22 | A22 |
| K5 | $\overline{\text{PWE3}}$/$\overline{\text{PSDDQM3}}$/$\overline{\text{PBS3}}$ | M2 | HD28 |
| K6 | $\overline{\text{PWE1}}$/$\overline{\text{PSDDQM1}}$/$\overline{\text{PBS1}}$ | M3 | HD31 |
| K7 | $\overline{\text{POE}}$/$\overline{\text{PSDRAS}}$/PGPL2 | M4 | $V_{DDH}$ |
| K8 | $\overline{\text{IRQ2}}$/BADDR30 | M5 | GND |
| K9 | Reserved | M6 | GND |
| K10 | GND | M7 | $V_{DDH}$ |
| K11 | GND | M8 | $V_{DD}$ |
| K12 | GND | M9 | $V_{DDH}$ |
| K13 | GND | M10 | GND |
| K14 | CLKOUT | M14 | GND |
| M15 | $V_{DDH}$ | P12 | $V_{CCSYN}$ |
| M16 | $\overline{\text{HBRST}}$ | P13 | GND |
| M17 | $V_{DDH}$ | P14 | GND |
| M18 | $V_{DDH}$ | P15 | $\overline{\text{TA}}$ |
| M19 | GND | P16 | $\overline{\text{BR}}$ |
| M20 | $V_{DDH}$ | P17 | $\overline{\text{TEA}}$ |

**Table 1. MSC8126 Signal Listing by Ball Designator (continued)**

| Des. | Signal Name | Des. | Signal Name |
|---|---|---|---|
| M21 | A24 | P18 | PSDVAL |
| M22 | A21 | P19 | DP0/DREQ1/EXT_BR2 |
| N2 | HD26 | P20 | $V_{DDH}$ |
| N3 | HD30 | P21 | GND |
| N4 | HD29 | P22 | A19 |
| N5 | HD24 | R2 | HD18 |
| N6 | PWE2/PSDDQM2/PBS2 | R3 | $V_{DDH}$ |
| N7 | $V_{DDH}$ | R4 | GND |
| N8 | HWBS0/HDBS0/HWBE0/HDBE0 | R5 | HD22 |
| N9 | HBCS | R6 | HWBS6/HDBS6/HWBE6/HDBE6/PWE6/PSDDQM6/PBS6 |
| N10 | GND | R7 | HWBS4/HDBS4/HWBE4/HDBE4/PWE4/PSDDQM4/PBS4 |
| N14 | GND | R8 | TSZ1 |
| N15 | HRDS/HRW/HRDE | R9 | TSZ3 |
| N16 | BG | R10 | IRQ1/GBL |
| N17 | HCS | R11 | $V_{DD}$ |
| N18 | CS0 | R12 | $V_{DD}$ |
| N19 | PSDWE/PGPL1 | R13 | $V_{DD}$ |
| N20 | GPIO26/TDM0RDAT | R14 | TT0/HA7 |
| N21 | A23 | R15 | IRQ7/DP7/DREQ4 |
| N22 | A20 | R16 | IRQ6/DP6/DREQ3 |
| P2 | HD20 | R17 | IRQ3/DP3/DREQ2/EXT_BR3 |
| P3 | HD27 | R18 | TS |
| P4 | HD25 | R19 | IRQ2/DP2/DACK2/EXT_DBG2 |
| P5 | HD23 | R20 | A17 |
| P6 | HWBS3/HDBS3/HWBE3/HDBE3 | R21 | A18 |
| P7 | HWBS2/HDBS2/HWBE2/HDBE2 | R22 | A16 |
| P8 | HWBS1/HDBS1/HWBE1/HDBE1 | T2 | HD17 |
| P9 | HCLKIN | T3 | HD21 |
| P10 | GND | T4 | HD1/DSISYNC |
| P11 | $GND_{SYN}$ | T5 | HD0/SWTE |
| T6 | HWBS7/HDBS7/HWBE7/HDBE7/PWE7/PSDDQM7/PBS7 | U21 | A12 |
| T7 | HWBS5/HDBS5/HWBE5/HDBE5/PWE5/PSDDQM5/PBS5 | U22 | A13 |
| T8 | TSZ0 | V2 | HD3/MODCK1 |
| T9 | TSZ2 | V3 | $V_{DDH}$ |
| T10 | TBST | V4 | GND |
| T11 | $V_{DD}$ | V5 | D0 |
| T12 | D16 | V6 | D1 |
| T13 | TT1 | V7 | D4 |
| T14 | D21 | V8 | D5 |

### Table 1. MSC8126 Signal Listing by Ball Designator (continued)

| Des. | Signal Name | Des. | Signal Name |
|---|---|---|---|
| T15 | D23 | V9 | D7 |
| T16 | $\overline{\text{IRQ5}}$/DP5/$\overline{\text{DACK4}}$/$\overline{\text{EXT\_BG3}}$ | V10 | D10 |
| T17 | $\overline{\text{IRQ4}}$/DP4/$\overline{\text{DACK3}}$/$\overline{\text{EXT\_DBG3}}$ | V11 | D12 |
| T18 | $\overline{\text{IRQ1}}$/DP1/$\overline{\text{DACK1}}$/$\overline{\text{EXT\_BG2}}$ | V12 | D13 |
| T19 | D30 | V13 | D18 |
| T20 | GND | V14 | D20 |
| T21 | A15 | V15 | GND |
| T22 | A14 | V16 | D24 |
| U2 | HD16 | V17 | D27 |
| U3 | HD19 | V18 | D29 |
| U4 | HD2/DSI64 | V19 | A8 |
| U5 | D2 | V20 | A9 |
| U6 | D3 | V21 | A10 |
| U7 | D6 | V22 | A11 |
| U8 | D8 | W2 | HD6 |
| U9 | D9 | W3 | HD5/CNFGS |
| U10 | D11 | W4 | HD4/MODCK2 |
| U11 | D14 | W5 | GND |
| U12 | D15 | W6 | GND |
| U13 | D17 | W7 | $V_{DDH}$ |
| U14 | D19 | W8 | $V_{DDH}$ |
| U15 | D22 | W9 | GND |
| U16 | D25 | W10 | HDST1/HA10 |
| U17 | D26 | W11 | HDST0/HA9 |
| U18 | D28 | W12 | $V_{DDH}$ |
| U19 | D31 | W13 | GND |
| U20 | $V_{DDH}$ | W14 | HD40/D40/ETHRXD0 |
| W15 | $V_{DDH}$ | AA9 | $V_{DDH}$ |
| W16 | HD33/D33/reserved | AA10 | HD54/D54/ETHTX_EN |
| W17 | $V_{DDH}$ | AA11 | HD52/D52 |
| W18 | HD32/D32/reserved | AA12 | $V_{DDH}$ |
| W19 | GND | AA13 | GND |
| W20 | GND | AA14 | $V_{DDH}$ |
| W21 | A7 | AA15 | HD46/D46/ETHTXT0 |
| W22 | A6 | AA16 | GND |
| Y2 | HD7 | AA17 | HD42/D42/ETHRXD2/reserved |
| Y3 | HD15 | AA18 | HD38/D38/reserved |
| Y4 | $V_{DDH}$ | AA19 | HD35/D35/reserved |
| Y5 | HD9 | AA20 | A0 |

## 2.2 Recommended Operating Conditions

**Table 3** lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

**Table 3. Recommended Operating Conditions**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Core and PLL supply voltage:<br>• Standard<br>— 400 MHz<br>— 500 MHz<br>• Reduced (300 and 400 MHz) | $V_{DD}$<br>$V_{CCSYN}$ | <br><br>1.14 to 1.26<br>1.16 to 1.24<br>1.07 to 1.13 | <br><br>V<br>V<br>V |
| I/O supply voltage | $V_{DDH}$ | 3.135 to 3.465 | V |
| Input voltage | $V_{IN}$ | –0.2 to $V_{DDH}$+0.2 | V |
| Operating temperature range:<br>• Standard<br>• Extended | <br>$T_J$<br>$T_J$ | <br>0 to 90<br>–40 to 105 | <br>°C<br>°C |

## 2.3 Thermal Characteristics

**Table 4** describes thermal characteristics of the MSC8126 for the FC-PBGA packages.

**Table 4. Thermal Characteristics for the MSC8126**

| Characteristic | Symbol | FC-PBGA 20 × 20 mm[5] | | Unit |
|---|---|---|---|---|
| | | Natural Convection | 200 ft/min (1 m/s) airflow | |
| Junction-to-ambient[1, 2] | $R_{\theta JA}$ | 26 | 21 | °C/W |
| Junction-to-ambient, four-layer board[1, 3] | $R_{\theta JA}$ | 19 | 15 | °C/W |
| Junction-to-board (bottom)[4] | $R_{\theta JB}$ | 9 | | °C/W |
| Junction-to-case[5] | $R_{\theta JC}$ | 0.9 | | °C/W |
| Junction-to-package-top[6] | $\Psi_{JT}$ | 1 | | °C/W |

**Notes:**
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

**Section 3.5**, *Thermal Considerations* provides a detailed explanation of these characteristics.

In all cases, the power-up sequence must follow the guidelines shown in **Figure 8**.

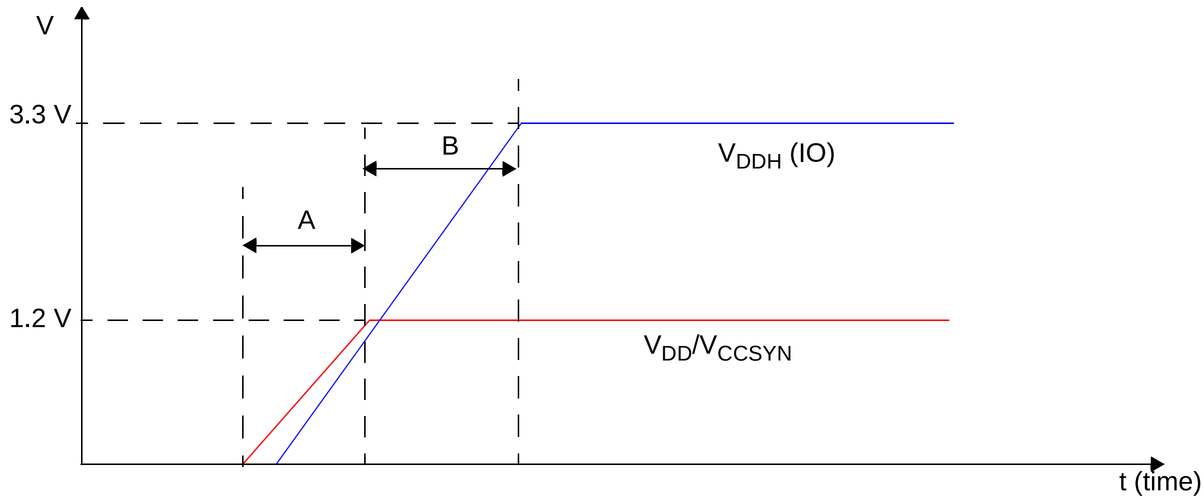



**Figure 8. Power-Up Sequence for $V_{DDH}$ and $V_{DD}/V_{CCSYN}$**

The following rules apply:

1. During time interval A, $V_{DDH}$ should always be equal to or less than the $V_{DD}/V_{CCSYN}$ voltage level. The duration of interval A should be kept below 10 ms.
2. The duration of timing interval B should be kept as small as possible and less than 10 ms.

### 2.5.3 Clock and Timing Signals

The following sections include a description of clock signal characteristics. **Table 7** shows the maximum frequency values for internal (Core, Reference, Bus, and DSI) and external (CLKIN and CLKOUT) clocks. The user must ensure that maximum frequency values are not exceeded.

**Table 7. Maximum Frequencies**

| Characteristic | Maximum in MHz |
|---|---|
| Core frequency | 400/500 |
| Reference frequency (REFCLK) | 133/166 |
| Internal bus frequency (BLCK) | 133/166 |
| DSI clock frequency (HCLKIN) | HCLKIN ≤ (min{100 MHz, CLKOUT}) |
| External clock frequency (CLKIN or CLKOUT) | 133/166 |

**Table 8. Clock Frequencies**

| Characteristics | Symbol | 400 MHz Device | | 500 MHz Device | |
|---|---|---|---|---|---|
| | | Min | Max | Min | Max |
| CLKIN frequency | $F_{CLKIN}$ | 20 | 133.3 | 20 | 166.7 |
| BCLK frequency | $F_{BCLK}$ | 40 | 133.3 | 40 | 166.7 |
| Reference clock (REFCLK) frequency | $F_{REFCLK}$ | 40 | 133.3 | 40 | 166.7 |
| Output clock (CLKOUT) frequency | $F_{CLKOUT}$ | 40 | 133.3 | 40 | 166.7 |
| SC140 core clock frequency | $F_{CORE}$ | 200 | 400 | 200 | 500 |
| **Note:** The rise and fall time of external clocks should be 5 ns maximum | | | | | |

**Table 9. System Clock Parameters**

| Characteristic | Min | Max | Unit |
|---|---|---|---|
| Phase jitter between BCLK and CLKIN | — | 0.3 | ns |
| CLKIN frequency | 20 | see **Table 8** | MHz |
| CLKIN slope | — | 3 | ns |
| PLL input clock (after predivider) | 20 | 100 | MHz |
| PLL output frequency (VCO output)<br>• 400 MHz core<br>• 500 MHz core | 800 | <br>1600<br>2000 | MHz<br>MHz<br>MHz |
| CLKOUT frequency jitter[1] | — | 200 | ps |
| CLKOUT phase jitter[1] with CLKIN phase jitter of ±100 ps | — | 500 | ps |
| **Notes:** **1.** Peak-to-peak.<br>**2.** Not tested. Guaranteed by design. | | | |

## 2.5.4 Reset Timing

The MSC8126 has several inputs to the reset logic:

- Power-on reset ($\overline{\text{PORESET}}$)
- External hard reset ($\overline{\text{HRESET}}$)
- External soft reset ($\overline{\text{SRESET}}$)
- Software watchdog reset
- Bus monitor reset
- Host reset command through JTAG

All MSC8126 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 10** describes the reset sources.

**Table 10. Reset Sources**

| Name | Direction | Description |
|---|---|---|
| Power-on reset ($\overline{\text{PORESET}}$) | Input | Initiates the power-on reset flow that resets the MSC8126 and configures various attributes of the MSC8126. On $\overline{\text{PORESET}}$, the entire MSC8126 device is reset. SPLL states is reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the SC140 extended cores are reset, and system configuration is sampled. The clock mode (MODCK bits), reset configuration mode, boot mode, Chip ID, and use of either a DSI 64 bits port or a System Bus 64 bits port are configured only when $\overline{\text{PORESET}}$ is asserted. |
| External hard reset ($\overline{\text{HRESET}}$) | Input/ Output | Initiates the hard reset flow that configures various attributes of the MSC8126. While $\overline{\text{HRESET}}$ is asserted, $\overline{\text{SRESET}}$ is also asserted. $\overline{\text{HRESET}}$ is an open-drain pin. Upon hard reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the SC140 extended cores are reset, and system configuration is sampled. The most configurable features are reconfigured. These features are defined in the 32-bit hard reset configuration word described in *Hard Reset Configuration Word* section of the *Reset* chapter in the *MSC8126 Reference Manual*. |
| External soft reset ($\overline{\text{SRESET}}$) | Input/ Output | Initiates the soft reset flow. The MSC8126 detects an external assertion of $\overline{\text{SRESET}}$ only if it occurs while the MSC8126 is not asserting reset. $\overline{\text{SRESET}}$ is an open-drain pin. Upon soft reset, $\overline{\text{SRESET}}$ is driven, the SC140 extended cores are reset, and system configuration is maintained. |
| Software watchdog reset | Internal | When the MSC8126 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence. |
| Bus monitor reset | Internal | When the MSC8126 bus monitor count reaches zero, a bus monitor hard reset is asserted. The enabled bus monitor event then generates an internal hard reset sequence. |
| Host reset command through the TAP | Internal | When a host reset command is written through the Test Access Port (TAP), the TAP logic asserts the soft reset signal and an internal soft reset sequence is generated. |

**Table 11** summarizes the reset actions that occur as a result of the different reset sources.

## 2.5.5 System Bus Access Timing

### 2.5.5.1 Core Data Transfers

Generally, all MSC8126 bus and system output signals are driven from the rising edge of the reference clock (REFCLK). The REFCLK is the CLKIN signal. Memory controller signals, however, trigger on four points within a REFCLK cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge of REFCLK (and T3 at the falling edge), but the spacing of T2 and T4 depends on the PLL clock ratio selected, as **Table 13** shows.

**Table 13. Tick Spacing for Memory Controller Signals**

| BCLK/SC140 clock | Tick Spacing (T1 Occurs at the Rising Edge of REFCLK) | | |
|---|---|---|---|
| | **T2** | **T3** | **T4** |
| 1:4, 1:6, 1:8, 1:10 | 1/4 REFCLK | 1/2 REFCLK | 3/4 REFCLK |
| 1:3 | 1/6 REFCLK | 1/2 REFCLK | 4/6 REFCLK |
| 1:5 | 2/10 REFCLK | 1/2 REFCLK | 7/10 REFCLK |

**Figure 10** is a graphical representation of **Table 13**.

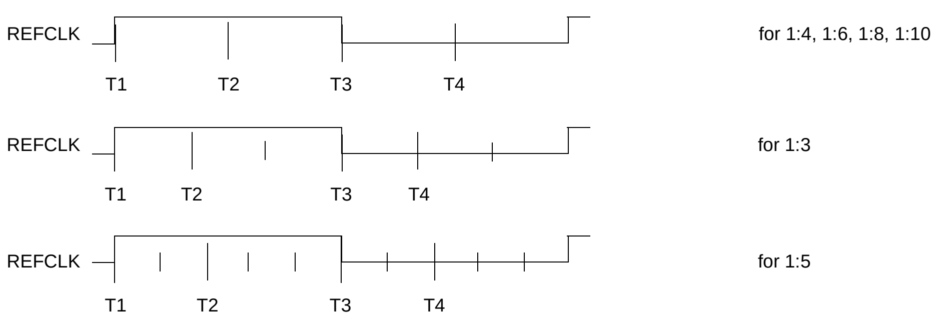



**Figure 10. Internal Tick Spacing for Memory Controller Signals**

**Table 15. AC Timing for SIU Outputs (continued)**

| No. | Characteristic | Value for Bus Speed in MHz | | | Units |
|---|---|---|---|---|---|
| | | Ref = CLKIN | | Ref = CLKOUT | |
| | | 133 | 166 | 133 | |
| 31 | $\overline{\text{PSDVAL}}$/$\overline{\text{TEA}}$/$\overline{\text{TA}}$ max delay from the 50% level of the REFCLK rising edge | 4.9 | 4.9 | 5.8 | ns |
| 32a | Address bus max delay from the 50% level of the REFCLK rising edge<br>• Multi-master mode (SIUBCR[EBM] = 1)<br>• Single-master mode (SIUBCR[EBM] = 0) | <br>5.5<br>4.2 | <br>5.5<br>3.9 | <br>6.4<br>5.1 | <br>ns<br>ns |
| 32b | Address attributes: TT[0–1]/$\overline{\text{TBST}}$/TSZ/$\overline{\text{GBL}}$ max delay from the 50% level of the REFCLK rising edge | 5.1 | 5.1 | 6.0 | ns |
| 32c | Address attributes: TT[2–4]/TC max delay from the 50% level of the REFCLK rising edge | 5.7 | 5.7 | 6.6 | ns |
| 32d | BADDR max delay from the 50% level of the REFCLK rising edge | 4.2 | 4.2 | 5.1 | ns |
| 33a | Data bus max delay from the 50% level of the REFCLK rising edge<br>• Data-pipeline mode<br>• Non-pipeline mode | <br>3.9<br>6.1 | <br>3.7<br>6.1 | <br>4.8<br>7.0 | <br>ns<br>ns |
| 33b | DP max delay from the 50% level of the REFCLK rising edge<br>• Data-pipeline mode<br>• Non-pipeline mode | <br>5.3<br>6.5 | <br>5.3<br>6.5 | <br>6.2<br>7.4 | <br>ns<br>ns |
| 34 | Memory controller signals/ALE/$\overline{\text{CS[0–4]}}$ max delay from the 50% level of the REFCLK rising edge | 4.2 | 3.9 | 5.1 | ns |
| 35a | $\overline{\text{DBG}}$/$\overline{\text{BG}}$/$\overline{\text{BR}}$/$\overline{\text{DBB}}$ max delay from the 50% level of the REFCLK rising edge | 4.7 | 4.7 | 5.6 | ns |
| 35b | $\overline{\text{AACK}}$/$\overline{\text{ABB}}$/$\overline{\text{TS}}$/$\overline{\text{CS[5–7]}}$ max delay from the 50% level of the REFCLK rising edge | 4.5 | 4.5 | 5.4 | ns |

**Notes:**

1. Values are measured from the 50% level of the REFCLK rising edge to the 50% signal level and assume a 20 pF load except where otherwise specified.
2. Except for specification 30, which is specified for a 10 pF load, all timings in this table are specified for a 20 pF load. Decreasing the load results in a timing decrease at the rate of 0.3 ns per 5 pF decrease in load. Increasing the load results in a timing increase at the rate of 0.15 ns per 5 pF increase in load.
3. The maximum bus frequency depends on the mode:
4. In 60x-compatible mode connected to another MSC8126 device, the frequency is determined by adding the input and output longest timing values, which results in the total delay for 20 pF output capacitance. You must also account for other influences that can affect timing, such as on-board clock skews, on-board noise delays, and so on.
   • In single-master mode, the frequency depends on the timing of the devices connected to the MSC8126.
   • To achieve maximum performance on the bus in single-master mode, disable the $\overline{\text{DBB}}$ signal by writing a 1 to the SIUMCR[BDD] bit. See the SIU chapter in the *MSC8122 Reference Manual* for details.

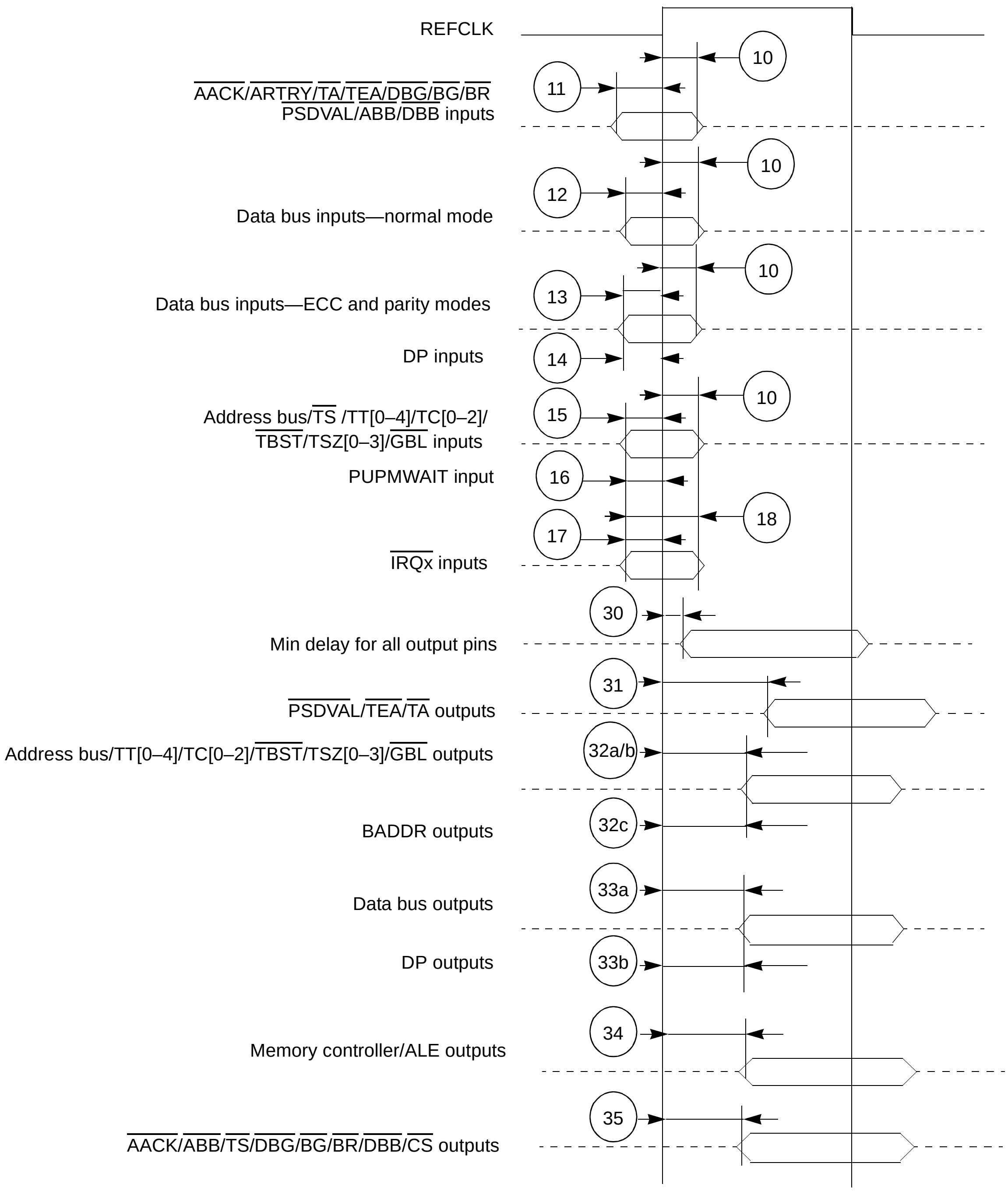



**Figure 11. SIU Timing Diagram**

### 2.5.5.3 DMA Data Transfers

**Table 17** describes the DMA signal timing.

**Table 17. DMA Signals**

| No. | Characteristic | Ref = CLKIN Min | Ref = CLKIN Max | Ref = CLKOUT (1.2 V only) Min | Ref = CLKOUT (1.2 V only) Max | Units |
|---|---|---|---|---|---|---|
| 37 | DREQ set-up time before the 50% level of the falling edge of REFCLK | 5.0 | — | 5.0 | — | ns |
| 38 | DREQ hold time after the 50% level of the falling edge of REFCLK | 0.5 | — | 0.5 | — | ns |
| 39 | $\overline{\text{DONE}}$ set-up time before the 50% level of the rising edge of REFCLK | 5.0 | — | 5.0 | — | ns |
| 40 | $\overline{\text{DONE}}$ hold time after the 50% level of the rising edge of REFCLK | 0.5 | — | 0.5 | — | ns |
| 41 | $\overline{\text{DACK}}$/$\overline{\text{DRACK}}$/$\overline{\text{DONE}}$ delay after the 50% level of the REFCLK rising edge | 0.5 | 7.5 | 0.5 | 8.4 | ns |

The DREQ signal is synchronized with REFCLK. To achieve fast response, a synchronized peripheral should assert DREQ according to the timings in **Table 17**. **Figure 13** shows synchronous peripheral interaction.

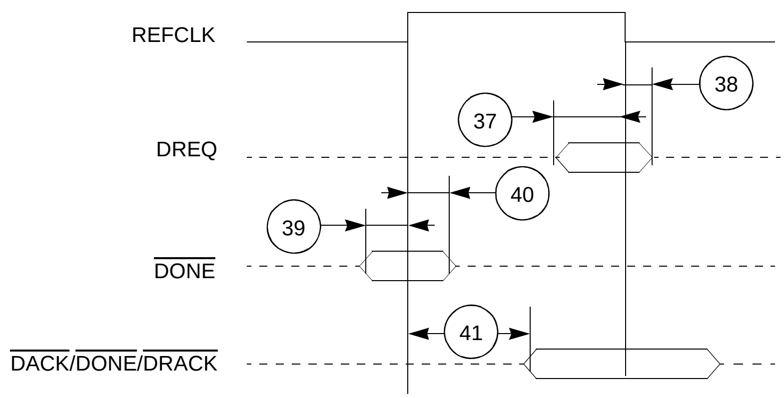
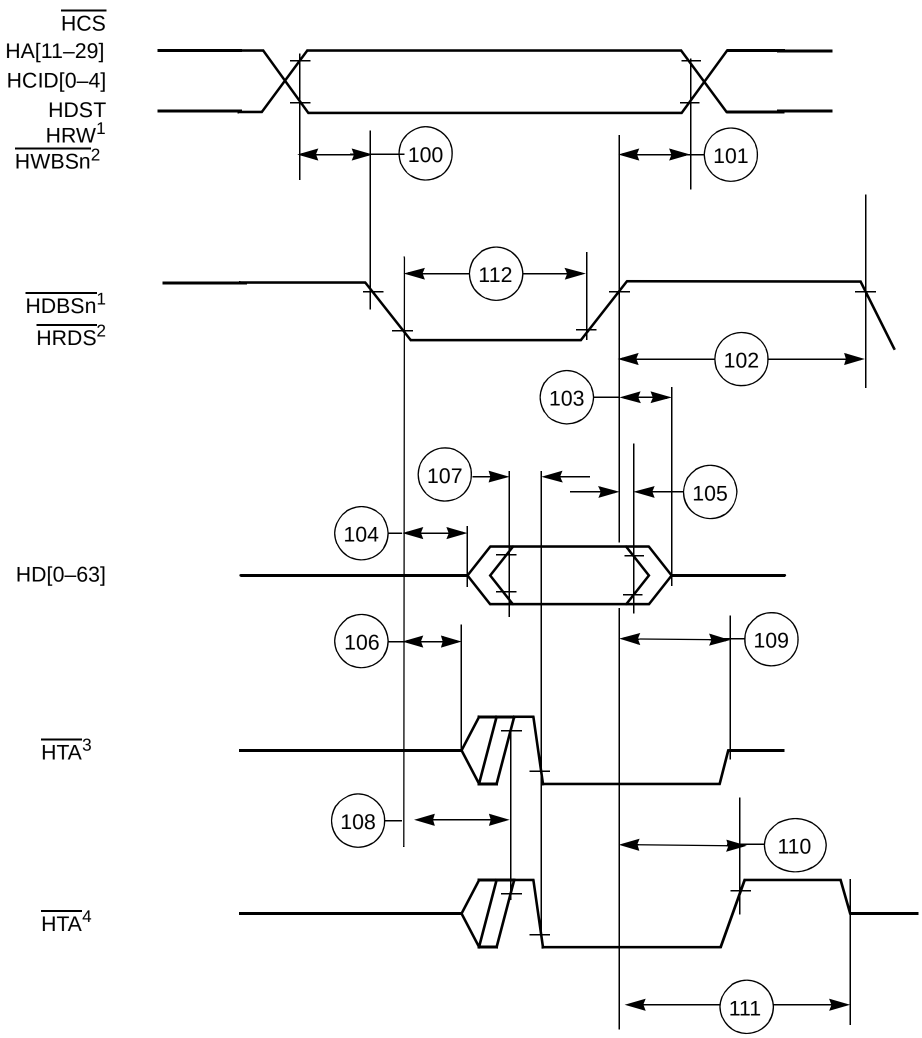



**Figure 13. DMA Signals**

**Figure 14** shows DSI asynchronous read signals timing.




**Notes:**
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.
3. HTA released at logic 0 (DCR[HTAAD] = 0) at end of access; used with pull-down implementation.
4. HTA released at logic 1 (DCR[HTAAD] = 1) at end of access; used with pull-up implementation.

**Figure 14. Asynchronous Single- and Dual-Strobe Modes Read Timing Diagram**

### 2.5.6.2 DSI Synchronous Mode

**Table 19. DSI Inputs—Synchronous Mode**

| No. | Characteristic | Expression | Min | Max | Units |
|---|---|---|---|---|---|
| 120 | HCLKIN Cycle Time[1, 2] | HTC | 10.0 | 55.6 | ns |
| 121 | HCLKIN high Pulse Width | (0.5 ± 0.1) × HTC | 4.0 | 33.3 | ns |
| 122 | HCLKIN low Pulse Width | (0.5 ± 0.1) × HTC | 4.0 | 33.3 | ns |
| 123 | HA[11–29] inputs set-up time | — | 1.2 | — | ns |
| 124 | HD[0–63] inputs set-up time | — | 0.4 | — | ns |
| 125 | HCID[0–4] inputs set-up time | — | 1.3 | — | ns |
| 126 | All other inputs set-up time | — | 1.2 | — | ns |
| 127 | All inputs hold time | — | 1.5 | — | ns |

**Notes:**
1. Values are based on a frequency range of 18–100 MHz.
2. Refer to **Table 7** for HCLKIN frequency limits.

**Table 20. DSI Outputs—Synchronous Mode**

| No. | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| 128 | HCLKIN high to HD[0–63] output active | 2.0 | — | ns |
| 129 | HCLKIN high to HD[0–63] output valid | — | 6.3 | ns |
| 130 | HD[0–63] output hold time | 1.7 | — | ns |
| 131 | HCLKIN high to HD[0–63] output high impedance | — | 7.6 | ns |
| 132 | HCLKIN high to $\overline{\text{HTA}}$ output active | 2.0 | — | ns |
| 133 | HCLKIN high to $\overline{\text{HTA}}$ output valid | — | 5.9 | ns |
| 134 | $\overline{\text{HTA}}$ output hold time | 1.7 | — | ns |
| 135 | HCLKIN high to $\overline{\text{HTA}}$ high impedance | — | 6.3 | ns |

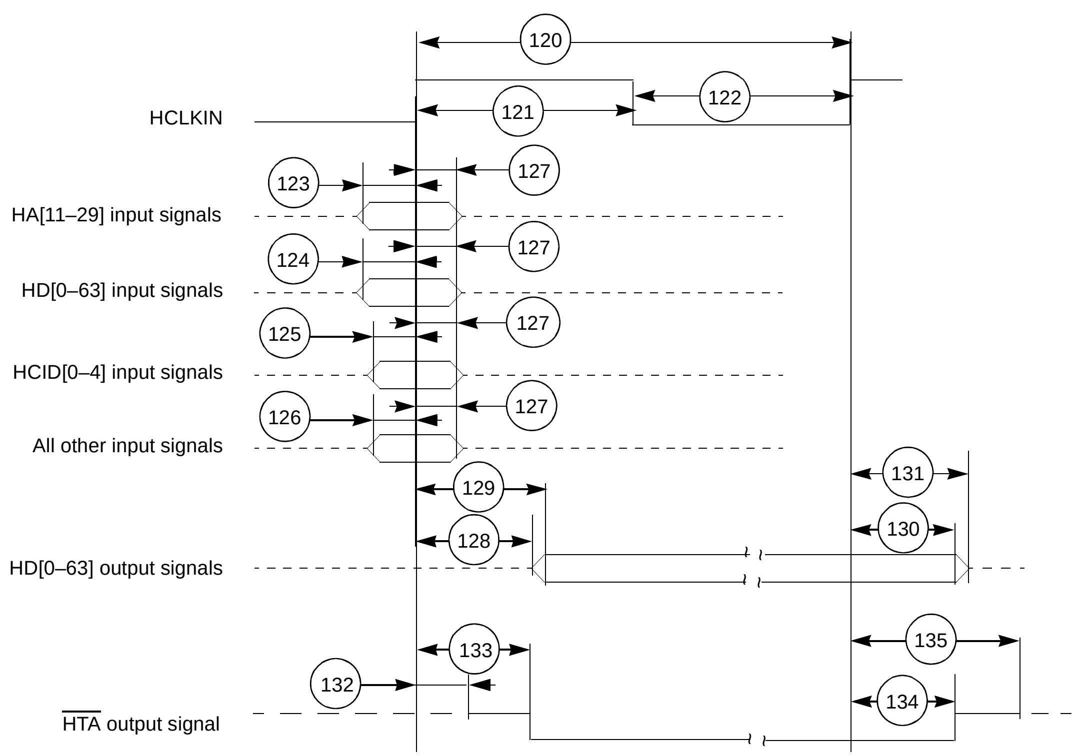



**Figure 17. DSI Synchronous Mode Signals Timing Diagram**

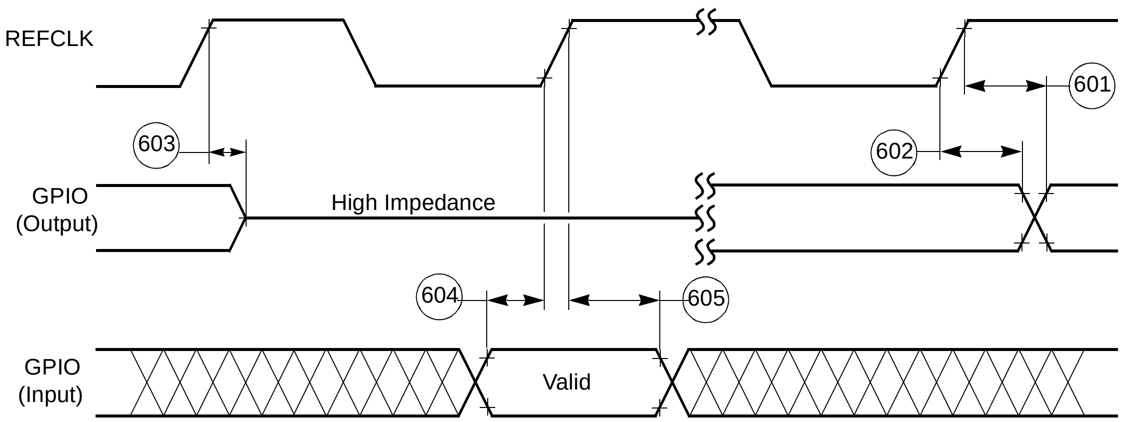



**Figure 27. GPIO Timing**

## 2.5.12 EE Signals

**Table 29. EE Pin Timing**

| Number | Characteristics | Type | Min |
|---|---|---|---|
| 65 | EE0 (input) | Asynchronous | 4 core clock periods |
| 66 | EE1 (output) | Synchronous to Core clock | 1 core clock period |

**Notes:** **1.** The core clock is the SC140 core clock. The ratio between the core clock and CLKOUT is configured during power-on-reset.
**2.** Refer to **Table 1-4** on page 1-6 for details on EE pin functionality.

**Figure 28** shows the signal behavior of the EE pins.

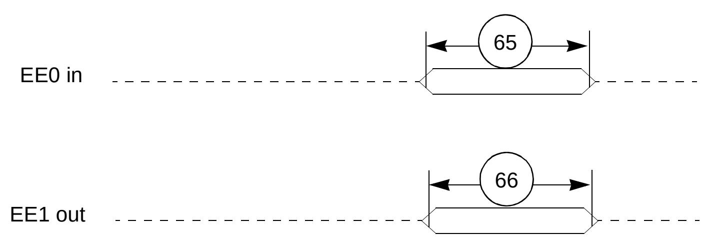



**Figure 28. EE Pin Timing**

## 2.5.13 JTAG Signals

**Table 30. JTAG Timing**

| No. | Characteristics | All frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 700 | TCK frequency of operation ($1/(T_C \times 4)$; maximum 25 MHz) | 0.0 | 25 | MHz |
| 701 | TCK cycle time | 40.0 | — | ns |
| 702 | TCK clock pulse width measured at $V_M$ = 1.6 V<br>• High<br>• Low | <br>20.0<br>16.0 | <br>—<br>— | <br>ns<br>ns |
| 703 | TCK rise and fall times | 0.0 | 3.0 | ns |

## 3.5 Thermal Considerations

An estimation of the chip-junction temperature, $T_J$, in °C can be obtained from the following:

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \text{Eqn. 1}$$

where

$T_A$ = ambient temperature near the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$P_D = P_{INT} + P_{I/O}$ = power dissipation in the package (W)
$P_{INT} = I_{DD} \times V_{DD}$ = internal power dissipation (W)
$P_{I/O}$ = power dissipated from device on output pins (W)

The power dissipation values for the MSC8126 are listed in **Table 2-3**. The ambient temperature for the device is the air temperature in the immediate vicinity that would cool the device. The junction-to-ambient thermal resistances are JEDEC standard values that provide a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. The value that more closely approximates a specific application depends on the power dissipated by other components on the printed circuit board (PCB). The value obtained using a single layer board is appropriate for tightly packed PCB configurations. The value obtained using a board with internal planes is more appropriate for boards with low power dissipation (less than 0.02 W/cm$^2$ with natural convection) and well separated components. Based on an estimation of junction temperature using this technique, determine whether a more detailed thermal analysis is required. Standard thermal management techniques can be used to maintain the device thermal junction temperature below its maximum. If $T_J$ appears to be too high, either lower the ambient temperature or the power dissipation of the chip. You can verify the junction temperature by measuring the case temperature using a small diameter thermocouple (40 gauge is recommended) or an infrared temperature sensor on a spot on the device case that is painted black. The MSC8126 device case surface is too shiny (low emissivity) to yield an accurate infrared temperature measurement. Use the following equation to determine $T_J$:

$$T_J = T_T + (\theta_{JA} \times P_D) \qquad \text{Eqn. 2}$$

where

$T_T$ = thermocouple (or infrared) temperature on top of the package (°C)
$\theta_{JA}$ = thermal characterization parameter (°C/W)
$P_D$ = power dissipation in the package (W)

**Note:** See *MSC8102, MSC8122, and MSC8126 Thermal Management Design Guidelines* (AN2601/D).

# 4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

| Part | Package Type | Spheres | Core Voltage | Operating Temperature | Core Frequency (MHz) | Order Number |
|---|---|---|---|---|---|---|
| MSC8126 | Flip Chip Plastic Ball Grid Array (FC-PBGA) | Lead-free | 1.2 V | –40° to 105°C | 400 | MSC8126TVT6400 |
| | | Lead-bearing | | | | MSC8126TMP6400 |
| | | Lead-free | | 0° to 90°C | 500 | MSC8126VT8000 |
| | | Lead-bearing | | | | MSC8126MP8000 |

# 7 Revision History

Table 31 provides a revision history for this data sheet.

**Table 31. Document Revision History**

| Revision | Date | Description |
|---|---|---|
| 0 | May 2004 | • Initial release. |
| 1 | Jun. 2004 | • Updated timing number 32b.<br>• Updated DSI timing specifications. |
| 2 | Sep 2004 | • New orderable parts added with other core voltage and temperature options.<br>• Updated thermal characteristics.<br>• In Table 2-14, removed references to 30 pF.<br>• Design guidelines and layout recommendations updated. |
| 3 | Nov. 2004 | • Added 500 MHz core and 166 MHz bus speed options.<br>• Definitions of GPIO[27–28] updated.<br>• Bus, TDM, and GPIO timing updated. $I^2C$ timing changed to GPIO timing.<br>• GPIO[27–28] connections updated. MWBEn replaced with correct name HWBEn.<br>• Design guidelines update. |
| 4 | Jan. 2005 | • Package type changed to FC-PBGA for all frequencies.<br>• Low-voltage 300 MHz power changed to 1.1 V.<br>• $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ definitions updated.<br>• Undershoot and overshoot values added for $V_{DDH}$.<br>• RMII timing updated.<br>• Design guidelines updated and reorganized. |
| 5 | May 2005 | • Multiple AC timing specifications updated. |
| 6 | May 2005 | • Multiple AC timing specifications updated. |
| 7 | Jul. 2005 | • Multiple AC timing specifications updated. |
| 8 | Jul. 2005 | • AC specification table layout modified. |
| 9 | Sep. 2005 | • ETHTX_EN type and $\overline{\text{TRST}}$ description updated.<br>• Package drawing updated.<br>• Clock specifications updated.<br>• Start-up sequence updated. |
| 10 | Oct 2005 | • $V_{DDH}$ + 10% changed to $V_{DDH}$ + 8% in **Figure 2-1**.<br>• $V_{DDH}$ +20% changed to $V_{DDH}$ + 17% in **Figure 2-1**. |
| 11 | Apr 2006 | • Reset timing updated to reflect actual values in **Table 2-11**. |
| 12 | Oct. 2006 | • Added new timings 17 and 18 for IRQ set time and pulse width in **Table 2-13** |
| 13 | Dec. 2007 | • Converted to new data sheet format.<br>• Added PLL supply current to **Table 5** in **Section 2.4**.<br>• Modified **Figure 5** in **Section 2.4** to make it clear that the time limits for undershoot referred to values below –0.3 V and not GND.<br>• Added cross-references between **Sections 2.5.2** and **Section 3.1** and **3.2**.<br>• Added power-sequence guidelines to **Sections 2.5.2**.<br>• Added CLKIN jitter characteristic specifications to Table 9.<br>• Added additional guidelines to prevent reverse current to **Section 3.1**.<br>• Added connectivity guidelines for DSI in sliding windows mode to **Section 3.3**. |
| 14 | May 2008 | • Changed $V_{IL}$ maximum and reference value to 0.8 V in **Table 5**. |
| 15 | Dec 2008 | • Clarified the wording of note 2 in **Table 15** on p. 24. |

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