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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	13
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 6x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1006dasp-x0

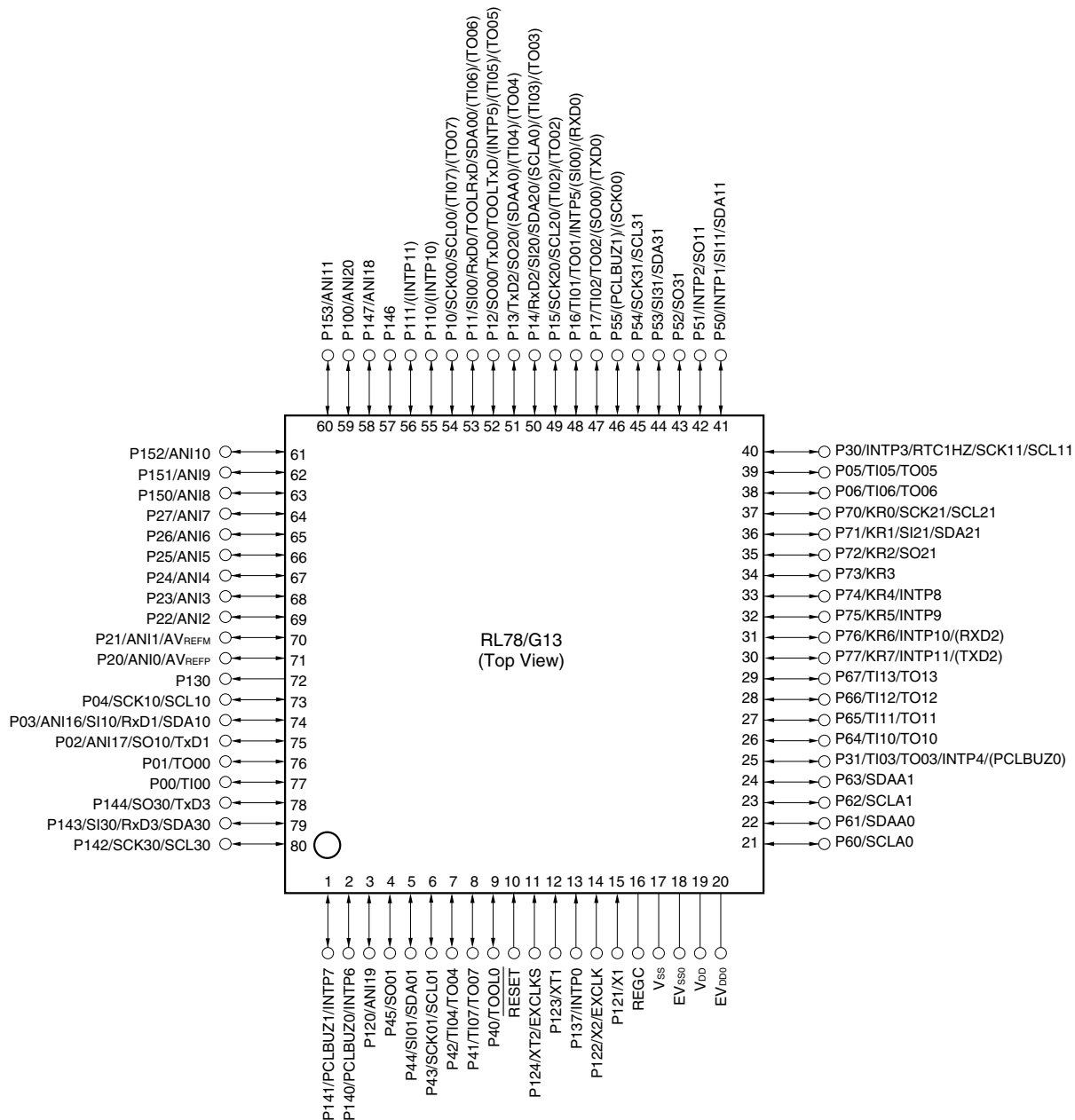
(7/12)

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

R01DS0131EJ0330 Rev.3.30
Mar 31, 2016

1.3.12 80-pin products

- 80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)

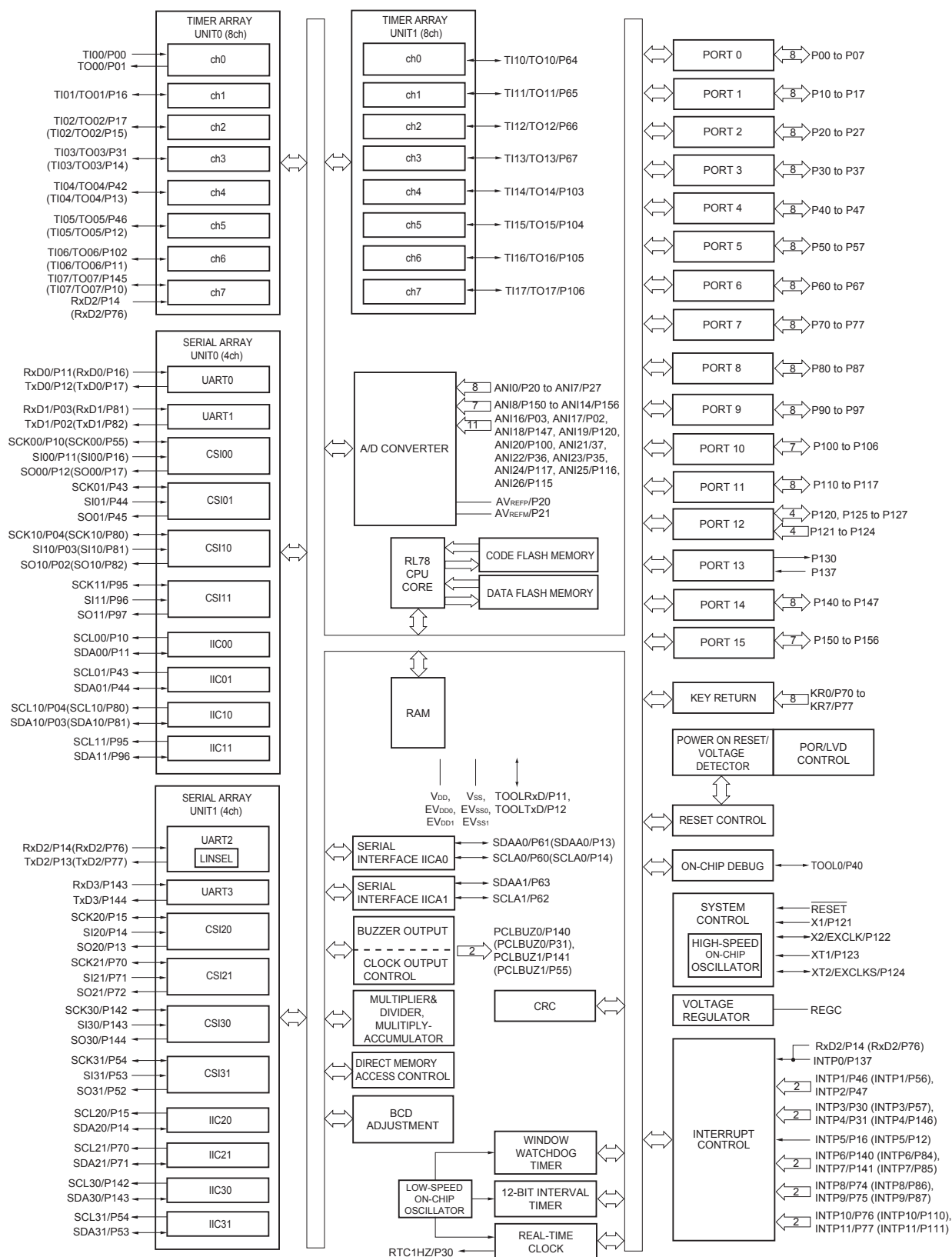


- Cautions**
1. Make EV_{SS0} pin the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.
3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.14 128-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

2.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS0} = 0 V) (1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit		
Supply current ^{Note 1}	I _{DD1}	Operating mode	HS (high-speed main) mode ^{Note 5}	f _{IH} = 32 MHz ^{Note 3}	Basic operation	V _{DD} = 5.0 V		2.1		mA	
						V _{DD} = 3.0 V		2.1		mA	
					Normal operation	V _{DD} = 5.0 V		4.6	7.0	mA	
						V _{DD} = 3.0 V		4.6	7.0	mA	
				f _{IH} = 24 MHz ^{Note 3}	Normal operation	V _{DD} = 5.0 V		3.7	5.5	mA	
						V _{DD} = 3.0 V		3.7	5.5	mA	
				f _{IH} = 16 MHz ^{Note 3}	Normal operation	V _{DD} = 5.0 V		2.7	4.0	mA	
						V _{DD} = 3.0 V		2.7	4.0	mA	
				LS (low-speed main) mode ^{Note 5}	f _{IH} = 8 MHz ^{Note 3}	Normal operation	V _{DD} = 3.0 V		1.2	1.8	mA
							V _{DD} = 2.0 V		1.2	1.8	mA
				LV (low-voltage main) mode ^{Note 5}	f _{IH} = 4 MHz ^{Note 3}	Normal operation	V _{DD} = 3.0 V		1.2	1.7	mA
							V _{DD} = 2.0 V		1.2	1.7	mA
			HS (high-speed main) mode ^{Note 5}	f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 5.0 V	Normal operation	Square wave input		3.0	4.6	mA	
						Resonator connection		3.2	4.8	mA	
					Normal operation	Square wave input		3.0	4.6	mA	
						Resonator connection		3.2	4.8	mA	
					f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 5.0 V	Normal operation	Square wave input		1.9	2.7	mA
							Resonator connection		1.9	2.7	mA
				f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input		1.9	2.7	mA	
						Resonator connection		1.9	2.7	mA	
				LS (low-speed main) mode ^{Note 5}	f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input		1.1	1.7	mA
							Resonator connection		1.1	1.7	mA
					f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 2.0 V	Normal operation	Square wave input		1.1	1.7	mA
							Resonator connection		1.1	1.7	mA
			Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 4} T _A = −40°C	Normal operation	Square wave input		4.1	4.9	μA	
						Resonator connection		4.2	5.0	μA	
				f _{SUB} = 32.768 kHz ^{Note 4} T _A = +25°C	Normal operation	Square wave input		4.1	4.9	μA	
						Resonator connection		4.2	5.0	μA	
				f _{SUB} = 32.768 kHz ^{Note 4} T _A = +50°C	Normal operation	Square wave input		4.2	5.5	μA	
						Resonator connection		4.3	5.6	μA	
				f _{SUB} = 32.768 kHz ^{Note 4} T _A = +70°C	Normal operation	Square wave input		4.3	6.3	μA	
						Resonator connection		4.4	6.4	μA	
				f _{SUB} = 32.768 kHz ^{Note 4} T _A = +85°C	Normal operation	Square wave input		4.6	7.7	μA	
						Resonator connection		4.7	7.8	μA	

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 32 MHz
 - $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 16 MHz
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 8 MHz
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 4 MHz

- Remarks**
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH}: High-speed on-chip oscillator clock frequency
 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products**(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS0} = 0 V) (2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I _{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f _{IH} = 32 MHz ^{Note 4}	V _{DD} = 5.0 V		0.54	1.63	mA	
					V _{DD} = 3.0 V		0.54	1.63	mA	
				f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 5.0 V		0.44	1.28	mA	
					V _{DD} = 3.0 V		0.44	1.28	mA	
				f _{IH} = 16 MHz ^{Note 4}	V _{DD} = 5.0 V		0.40	1.00	mA	
					V _{DD} = 3.0 V		0.40	1.00	mA	
				LS (low-speed main) mode Note 7	f _{IH} = 8 MHz ^{Note 4}	V _{DD} = 3.0 V		260	530	μA
						V _{DD} = 2.0 V		260	530	μA
				LV (low-voltage main) mode Note 7	f _{IH} = 4 MHz ^{Note 4}	V _{DD} = 3.0 V		420	640	μA
						V _{DD} = 2.0 V		420	640	μA
			HS (high-speed main) mode Note 7	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.28	1.00	mA	
					Resonator connection		0.45	1.17	mA	
				f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.28	1.00	mA	
					Resonator connection		0.45	1.17	mA	
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.19	0.60	mA	
					Resonator connection		0.26	0.67	mA	
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.19	0.60	mA	
					Resonator connection		0.26	0.67	mA	
			LS (low-speed main) mode Note 7	f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		95	330	μA	
					Resonator connection		145	380	μA	
				f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 2.0 V	Square wave input		95	330	μA	
					Resonator connection		145	380	μA	
			Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 5} T _A = −40°C	Square wave input		0.25	0.57	μA	
					Resonator connection		0.44	0.76	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +25°C	Square wave input		0.30	0.57	μA	
					Resonator connection		0.49	0.76	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +50°C	Square wave input		0.37	1.17	μA	
					Resonator connection		0.56	1.36	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +70°C	Square wave input		0.53	1.97	μA	
					Resonator connection		0.72	2.16	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +85°C	Square wave input		0.82	3.37	μA	
					Resonator connection		1.01	3.56	μA	
	I _{DD3} ^{Note 6}	STOP mode ^{Note 8}	T _A = −40°C					0.18	0.50	μA
			T _A = +25°C					0.23	0.50	μA
			T _A = +50°C					0.30	1.10	μA
			T _A = +70°C					0.46	1.90	μA
			T _A = +85°C					0.75	3.30	μA

(Notes and Remarks are listed on the next page.)

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I _{DD1}	Operating mode	HS (high-speed main) mode Note 5	f _{IH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.3		mA
						V _{DD} = 3.0 V		2.3		mA
					Normal operation	V _{DD} = 5.0 V		5.2	8.5	mA
						V _{DD} = 3.0 V		5.2	8.5	mA
				f _{IH} = 24 MHz Note 3	Normal operation	V _{DD} = 5.0 V		4.1	6.6	mA
						V _{DD} = 3.0 V		4.1	6.6	mA
				f _{IH} = 16 MHz Note 3	Normal operation	V _{DD} = 5.0 V		3.0	4.7	mA
						V _{DD} = 3.0 V		3.0	4.7	mA
			LS (low-speed main) mode Note 5	f _{IH} = 8 MHz Note 3	Normal operation	V _{DD} = 3.0 V		1.3	2.1	mA
						V _{DD} = 2.0 V		1.3	2.1	mA
			LV (low-voltage main) mode Note 5	f _{IH} = 4 MHz Note 3	Normal operation	V _{DD} = 3.0 V		1.3	1.8	mA
						V _{DD} = 2.0 V		1.3	1.8	mA
			HS (high-speed main) mode Note 5	f _{MX} = 20 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		3.4	5.5	mA
						Resonator connection		3.6	5.7	mA
				f _{MX} = 20 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		3.4	5.5	mA
						Resonator connection		3.6	5.7	mA
				f _{MX} = 10 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		2.1	3.2	mA
						Resonator connection		2.1	3.2	mA
				f _{MX} = 10 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		2.1	3.2	mA
						Resonator connection		2.1	3.2	mA
			LS (low-speed main) mode Note 5	f _{MX} = 8 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.2	2.0	mA
				f _{MX} = 8 MHz Note 2, V _{DD} = 2.0 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.2	2.0	mA
			Subsystem clock operation	f _{SUB} = 32.768 kHz Note 4 T _A = -40°C	Normal operation	Square wave input		4.8	5.9	μA
						Resonator connection		4.9	6.0	μA
				f _{SUB} = 32.768 kHz Note 4 T _A = +25°C	Normal operation	Square wave input		4.9	5.9	μA
						Resonator connection		5.0	6.0	μA
				f _{SUB} = 32.768 kHz Note 4 T _A = +50°C	Normal operation	Square wave input		5.0	7.6	μA
						Resonator connection		5.1	7.7	μA
				f _{SUB} = 32.768 kHz Note 4 T _A = +70°C	Normal operation	Square wave input		5.2	9.3	μA
						Resonator connection		5.3	9.4	μA
				f _{SUB} = 32.768 kHz Note 4 T _A = +85°C	Normal operation	Square wave input		5.7	13.3	μA
						Resonator connection		5.8	13.4	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 32 MHz
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 16 MHz
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 8 MHz
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 4 MHz

- Remarks**
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH}: High-speed on-chip oscillator clock frequency
 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2)

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK2}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} +2 0		1/f _{MCK} +30		1/f _{MCK} +30		ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} +3 0		1/f _{MCK} +30		1/f _{MCK} +30		ns
		1.7 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} +4 0		1/f _{MCK} +40		1/f _{MCK} +40		ns
		1.6 V ≤ EV _{DD0} ≤ 5.5 V		—		1/f _{MCK} +40		1/f _{MCK} +40		ns
Slp hold time (from SCKp↑) ^{Note 2}	t _{KSI2}	1.8 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} +3 1		1/f _{MCK} +31		1/f _{MCK} +31		ns
		1.7 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} + 250		1/f _{MCK} + 250		1/f _{MCK} + 250		ns
		1.6 V ≤ EV _{DD0} ≤ 5.5 V		—		1/f _{MCK} + 250		1/f _{MCK} + 250		ns
Delay time from SCKp↓ to SOp output ^{Note 3}	t _{KSO2}	C = 30 pF ^{Note 4}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		2/f _{MCK} + 44		2/f _{MCK} + 110		2/f _{MCK} + 110	ns
			2.4 V ≤ EV _{DD0} ≤ 5.5 V		2/f _{MCK} + 75		2/f _{MCK} + 110		2/f _{MCK} + 110	ns
			1.8 V ≤ EV _{DD0} ≤ 5.5 V		2/f _{MCK} + 110		2/f _{MCK} + 110		2/f _{MCK} + 110	ns
			1.7 V ≤ EV _{DD0} ≤ 5.5 V		2/f _{MCK} + 220		2/f _{MCK} + 220		2/f _{MCK} + 220	ns
			1.6 V ≤ EV _{DD0} ≤ 5.5 V		—		2/f _{MCK} + 220		2/f _{MCK} + 220	ns

- Notes**
1. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp setup time becomes “to SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 2. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp hold time becomes “from SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 3. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The delay time to SOp output becomes “from SCKp↑” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 4. C is the load capacitance of the SOp output lines.
 5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)
 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$) (2/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, I_{OL} ^{Note 1}	I_{OL1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147			8.5 ^{Note 2}	mA
		Per pin for P60 to P63			15.0 ^{Note 2}	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty $\leq 70\%$ ^{Note 3})	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		40.0	mA
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$		15.0	mA
			$2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$		9.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty $\leq 70\%$ ^{Note 3})	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		40.0	mA
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$		35.0	mA
			$2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$		20.0	mA
		Total of all pins (When duty $\leq 70\%$ ^{Note 3})			80.0	mA
	I_{OL2}	Per pin for P20 to P27, P150 to P156			0.4 ^{Note 2}	mA
		Total of all pins (When duty $\leq 70\%$ ^{Note 3})	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		5.0	mA

- Notes**
- Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0} , EV_{SS1} and V_{SS} pin.
 - Do not exceed the total current value.
 - Specification under conditions where the duty factor $\leq 70\%$.
The output current value that has changed to the duty factor $> 70\%$ the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to $n\%$).
 - Total output current of pins = $(I_{OL} \times 0.7)/(n \times 0.01)$
 <Example> Where $n = 80\%$ and $I_{OL} = 10.0\text{ mA}$
 Total output current of pins = $(10.0 \times 0.7)/(80 \times 0.01) \cong 8.7\text{ mA}$
 However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD0} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I _{DD1}	Operating mode	HS (high-speed main) mode Note 5	f _{IH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.1		mA
						V _{DD} = 3.0 V		2.1		mA
					Normal operation	V _{DD} = 5.0 V		4.6	7.5	mA
						V _{DD} = 3.0 V		4.6	7.5	mA
				f _{IH} = 24 MHz Note 3	Normal operation	V _{DD} = 5.0 V		3.7	5.8	mA
						V _{DD} = 3.0 V		3.7	5.8	mA
				f _{IH} = 16 MHz Note 3	Normal operation	V _{DD} = 5.0 V		2.7	4.2	mA
						V _{DD} = 3.0 V		2.7	4.2	mA
			HS (high-speed main) mode Note 5	f _{MX} = 20 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	mA
				f _{MX} = 20 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	mA
				f _{MX} = 10 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	mA
				f _{MX} = 10 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	mA
		Subsystem clock operation	f _{SUB} = 32.768 kHz Note 4 T _A = −40°C	Normal operation	Square wave input		4.1	4.9	μA	
					Resonator connection		4.2	5.0	μA	
			f _{SUB} = 32.768 kHz Note 4 T _A = +25°C	Normal operation	Square wave input		4.1	4.9	μA	
					Resonator connection		4.2	5.0	μA	
			f _{SUB} = 32.768 kHz Note 4 T _A = +50°C	Normal operation	Square wave input		4.2	5.5	μA	
					Resonator connection		4.3	5.6	μA	
			f _{SUB} = 32.768 kHz Note 4 T _A = +70°C	Normal operation	Square wave input		4.3	6.3	μA	
					Resonator connection		4.4	6.4	μA	
			f _{SUB} = 32.768 kHz Note 4 T _A = +85°C	Normal operation	Square wave input		4.6	7.7	μA	
					Resonator connection		4.7	7.8	μA	
			f _{SUB} = 32.768 kHz Note 4 T _A = +105°C	Normal operation	Square wave input		6.9	19.7	μA	
					Resonator connection		7.0	19.8	μA	

(Notes and Remarks are listed on the next page.)

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(TA = -40 to +105°C, $2.4\text{ V} \leq V_{DD0} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = V_{SS0} = 0\text{ V}$) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I _{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f _{IH} = 32 MHz ^{Note 4}	V _{DD} = 5.0 V		0.54	2.90	mA	
					V _{DD} = 3.0 V		0.54	2.90	mA	
				f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 5.0 V		0.44	2.30	mA	
					V _{DD} = 3.0 V		0.44	2.30	mA	
				f _{IH} = 16 MHz ^{Note 4}	V _{DD} = 5.0 V		0.40	1.70	mA	
					V _{DD} = 3.0 V		0.40	1.70	mA	
			HS (high-speed main) mode Note 7	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.28	1.90	mA	
					Resonator connection		0.45	2.00	mA	
				f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.28	1.90	mA	
					Resonator connection		0.45	2.00	mA	
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.19	1.02	mA	
					Resonator connection		0.26	1.10	mA	
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.19	1.02	mA	
					Resonator connection		0.26	1.10	mA	
		Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 5} T _A = −40°C	Square wave input		0.25	0.57	μA		
				Resonator connection		0.44	0.76	μA		
			f _{SUB} = 32.768 kHz ^{Note 5} T _A = +25°C	Square wave input		0.30	0.57	μA		
				Resonator connection		0.49	0.76	μA		
			f _{SUB} = 32.768 kHz ^{Note 5} T _A = +50°C	Square wave input		0.37	1.17	μA		
				Resonator connection		0.56	1.36	μA		
			f _{SUB} = 32.768 kHz ^{Note 5} T _A = +70°C	Square wave input		0.53	1.97	μA		
				Resonator connection		0.72	2.16	μA		
			f _{SUB} = 32.768 kHz ^{Note 5} T _A = +85°C	Square wave input		0.82	3.37	μA		
				Resonator connection		1.01	3.56	μA		
		f _{SUB} = 32.768 kHz ^{Note 5} T _A = +105°C	Square wave input		3.01	15.37	μA			
			Resonator connection		3.20	15.56	μA			
	I _{DD3} ^{Note 6}	STOP mode ^{Note 8}	T _A = −40°C					0.18	0.50	μA
			T _A = +25°C					0.23	0.50	μA
			T _A = +50°C					0.30	1.10	μA
			T _A = +70°C					0.46	1.90	μA
			T _A = +85°C					0.75	3.30	μA
			T _A = +105°C					2.94	15.30	μA

(Notes and Remarks are listed on the next page.)

6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter is in operation.
7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.
8. Current flowing only during data flash rewrite.
9. Current flowing only during self programming.
10. For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode** in the RL78/G13 User's Manual.

- Remarks**
1. f_{IL} : Low-speed on-chip oscillator clock frequency
 2. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 3. f_{CLK} : CPU/peripheral hardware clock frequency
 4. Temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit	
			MIN.	MAX.		
Transfer rate		Reception	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		f _{MCK} /12 ^{Note 1}	bps
			Theoretical value of the maximum transfer rate f _{CLK} = 32 MHz, f _{MCK} = f _{CLK}		2.6	Mbps
			2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		f _{MCK} /12 ^{Note 1}	bps
			Theoretical value of the maximum transfer rate f _{CLK} = 32 MHz, f _{MCK} = f _{CLK}		2.6	Mbps
			2.4 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		f _{MCK} /12 ^{Notes 1,2}	bps
			Theoretical value of the maximum transfer rate f _{CLK} = 32 MHz, f _{MCK} = f _{CLK}		2.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

- 2.** The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$.
 $2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$: MAX. 1.3 Mbps

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

Remarks 1. $V_b[V]$: Communication line voltage**2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)**3.** f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

5. The smaller maximum transfer rate derived by using $f_{MCK}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

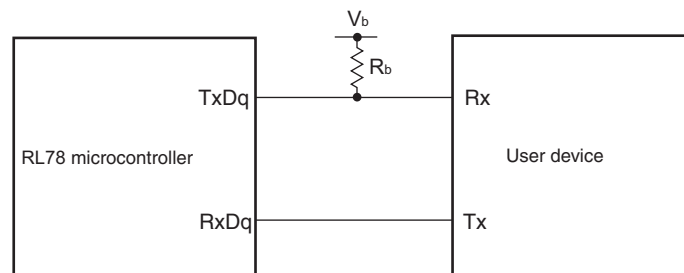
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

6. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 5 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (-) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (-) = AV_{REFM}
ANI0 to ANI14	Refer to 3.6.1 (1).	Refer to 3.6.1 (3).	Refer to 3.6.1 (4).
ANI16 to ANI26	Refer to 3.6.1 (2).		
Internal reference voltage Temperature sensor output voltage	Refer to 3.6.1 (1).		—

(1) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

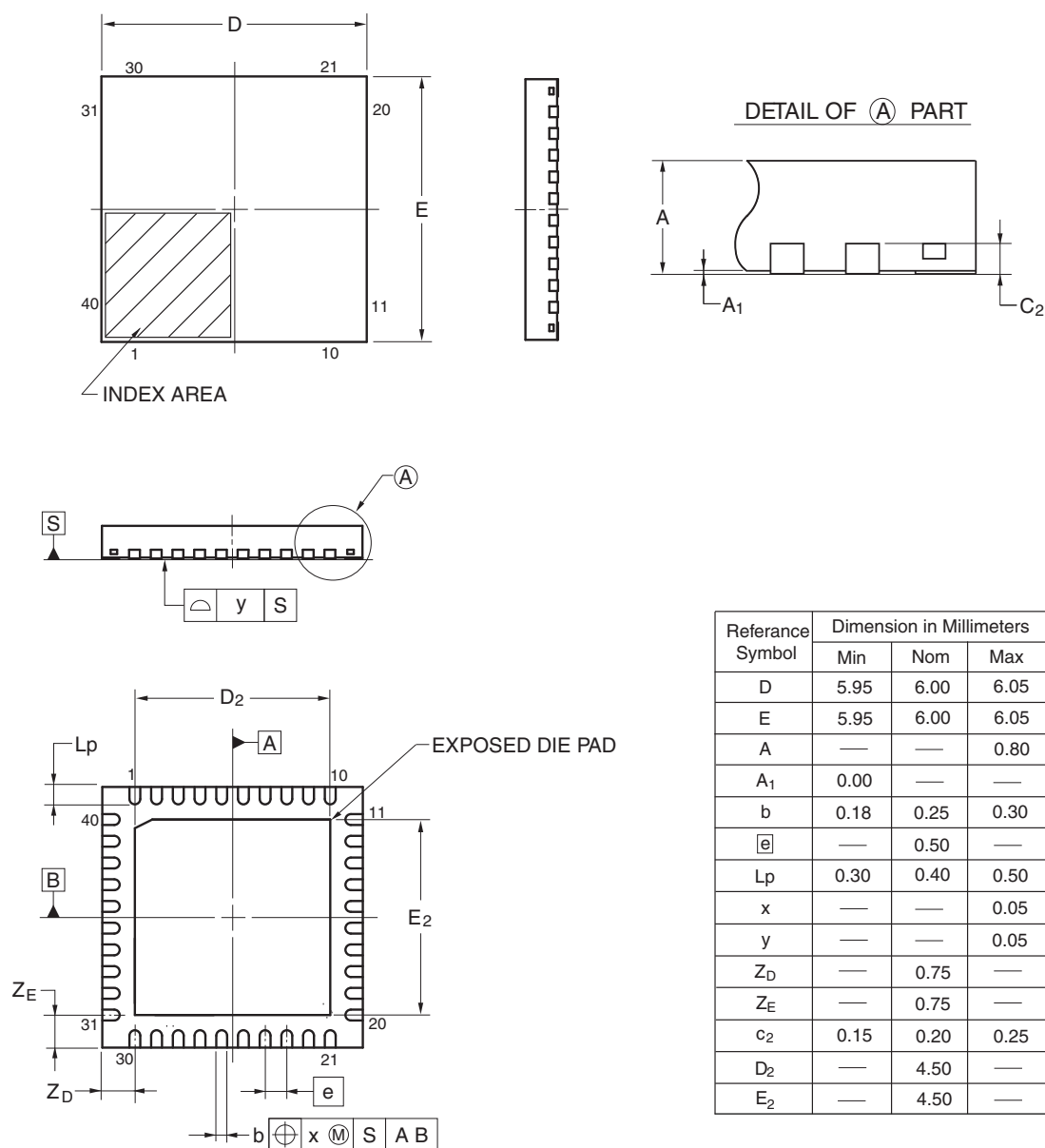
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		1.2	± 3.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2 to ANI14	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	E_{ZS}	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 0.25	%FSR
Full-scale error ^{Notes 1, 2}	E_{FS}	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 0.25	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 2.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 1.5	LSB
Analog input voltage	V_{AIN}	ANI2 to ANI14		0		AV_{REFP}	V
		Internal reference voltage output ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{BGR} ^{Note 4}			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{TMPS25} ^{Note 4}			V

(Notes are listed on the next page.)

4.7 40-pin Products

R5F100EAANA, R5F100ECANA, R5F100EDANA, R5F100EEANA, R5F100EFANA, R5F100EGANA, R5F100EHANA
 R5F101EAANA, R5F101ECANA, R5F101EDANA, R5F101EEANA, R5F101EFANA, R5F101EGANA, R5F101EHANA
 R5F100EADNA, R5F100ECDNA, R5F100EDDNA, R5F100EEDNA, R5F100EFDNA, R5F100EGDNA,
 R5F100EHDNA
 R5F101EADNA, R5F101ECDNA, R5F101EDDNA, R5F101EEDNA, R5F101EFDNA, R5F101EGDNA,
 R5F101EHDNA
 R5F100EAGNA, R5F100ECGNA, R5F100EDGNA, R5F100EEGNA, R5F100EFGNA, R5F100EGGNA,
 R5F100EHGNA

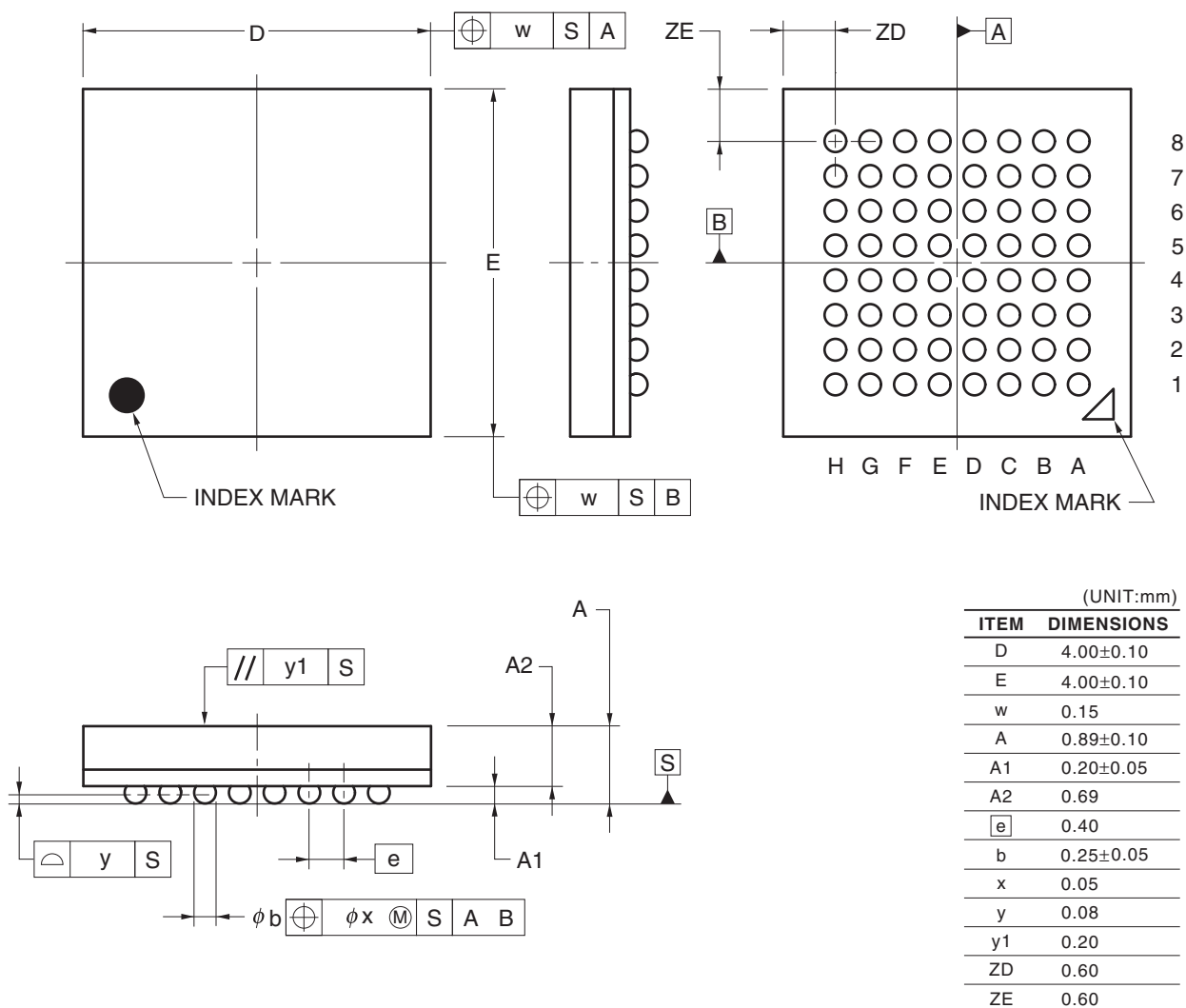
JEITA Package code	RENESAS code	Previous code	MASS (TYP.) [g]
P-HWQFN40-6x6-0.50	PWQN0040KC-A	P40K8-50-4B4-5	0.09



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R5F100LCABG, R5F100LDABG, R5F100LEABG, R5F100LFABG, R5F100LGABG, R5F100LHABG,
 R5F100LJABG
 R5F101LCABG, R5F101LDABG, R5F101LEABG, R5F101LFABG, R5F101LGABG, R5F101LHABG,
 R5F101LJABG
 R5F100LCGBG, R5F100LDGBG, R5F100LEGBG, R5F100LFGBG, R5F100LGGBG, R5F100LHGBG,
 R5F100LJGBG

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-VFBGA64-4x4-0.40	PVBG0064LA-A	P64F1-40-AA2-2	0.03



Revision History	RL78/G13 Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	Feb 29, 2012	-	First Edition issued
2.00	Oct 12, 2012	7	Figure 1-1. Part Number, Memory Size, and Package of RL78/G13: Pin count corrected.
		25	1.4 Pin Identification: Description of pins INTP0 to INTP11 corrected.
		40, 42, 44	1.6 Outline of Functions: Descriptions of Subsystem clock, Low-speed on-chip oscillator, and General-purpose register corrected.
		41, 43, 45	1.6 Outline of Functions: Lists of Descriptions changed.
		59, 63, 67	Descriptions of Note 8 in a table corrected.
		68	(4) Common to RL78/G13 all products: Descriptions of Notes corrected.
		69	2.4 AC Characteristics: Symbol of external system clock frequency corrected.
		96 to 98	2.6.1 A/D converter characteristics: Notes of overall error corrected.
		100	2.6.2 Temperature sensor characteristics: Parameter name corrected.
		104	2.8 Flash Memory Programming Characteristics: Incorrect descriptions corrected.
		116	3.10 52-pin products: Package drawings of 52-pin products corrected.
		120	3.12 80-pin products: Package drawings of 80-pin products corrected.
3.00	Aug 02, 2013	1	Modification of 1.1 Features
		3	Modification of 1.2 List of Part Numbers
		4 to 15	Modification of Table 1-1. List of Ordering Part Numbers, note, and caution
		16 to 32	Modification of package type in 1.3.1 to 1.3.14
		33	Modification of description in 1.4 Pin Identification
		48, 50, 52	Modification of caution, table, and note in 1.6 Outline of Functions
		55	Modification of description in table of Absolute Maximum Ratings ($T_A = 25^{\circ}\text{C}$)
		57	Modification of table, note, caution, and remark in 2.2.1 X1, XT1 oscillator characteristics
		57	Modification of table in 2.2.2 On-chip oscillator characteristics
		58	Modification of note 3 of table (1/5) in 2.3.1 Pin characteristics
		59	Modification of note 3 of table (2/5) in 2.3.1 Pin characteristics
		63	Modification of table in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products
		64	Modification of notes 1 and 4 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products
		65	Modification of table in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products
		66	Modification of notes 1, 5, and 6 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products
		68	Modification of notes 1 and 4 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products
		70	Modification of notes 1, 5, and 6 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products
		72	Modification of notes 1 and 4 in (3) Flash ROM: 384 to 512 KB of 44- to 100-pin products
		74	Modification of notes 1, 5, and 6 in (3) Flash ROM: 384 to 512 KB of 44- to 100-pin products
		75	Modification of (4) Peripheral Functions (Common to all products)
		77	Modification of table in 2.4 AC Characteristics
		78, 79	Addition of Minimum Instruction Execution Time during Main System Clock Operation
		80	Modification of figures of AC Timing Test Points and External System Clock Timing

Rev.	Date	Description	
		Page	Summary
3.00	Aug 02, 2013	163	Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I ² C mode) (1/2)
		164, 165	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I ² C mode) (2/2)
		166	Modification of table in 3.5.2 Serial interface IICA
		166	Modification of IICA serial transfer timing
		167	Addition of table in 3.6.1 A/D converter characteristics
		167, 168	Modification of table and notes 3 and 4 in 3.6.1 (1)
		169	Modification of description in 3.6.1 (2)
		170	Modification of description and note 3 in 3.6.1 (3)
		171	Modification of description and notes 3 and 4 in 3.6.1 (4)
		172	Modification of table and note in 3.6.3 POR circuit characteristics
		173	Modification of table of LVD Detection Voltage of Interrupt & Reset Mode
		173	Modification from Supply Voltage Rise Time to 3.6.5 Power supply voltage rising slope characteristics
		174	Modification of 3.9 Dedicated Flash Memory Programmer Communication (UART)
		175	Modification of table, figure, and remark in 3.10 Timing Specs for Switching Flash Memory Programming Modes
3.10	Nov 15, 2013	123	Caution 4 added.
		125	Note for operating ambient temperature in 3.1 Absolute Maximum Ratings deleted.
3.30	Mar 31, 2016		Modification of the position of the index mark in 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch) of 1.3.3 25-pin products
			Modification of power supply voltage in 1.6 Outline of Functions [20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products]
			Modification of power supply voltage in 1.6 Outline of Functions [40-pin, 44-pin, 48-pin, 52-pin, 64-pin products]
			Modification of power supply voltage in 1.6 Outline of Functions [80-pin, 100-pin, 128-pin products]
			$\overline{\text{ACK}}$ corrected to ACK
			$\overline{\text{ACK}}$ corrected to ACK

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