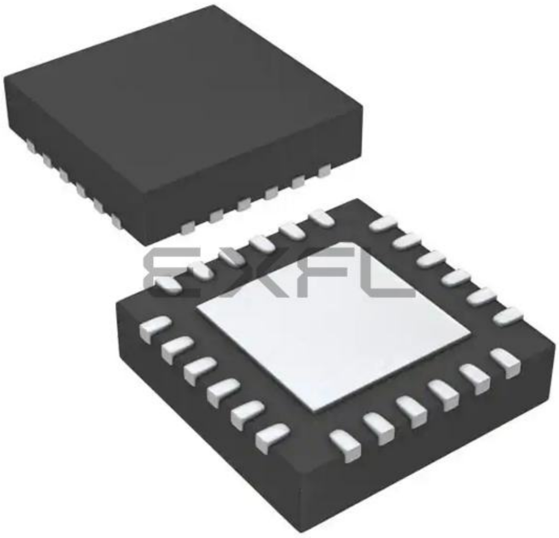
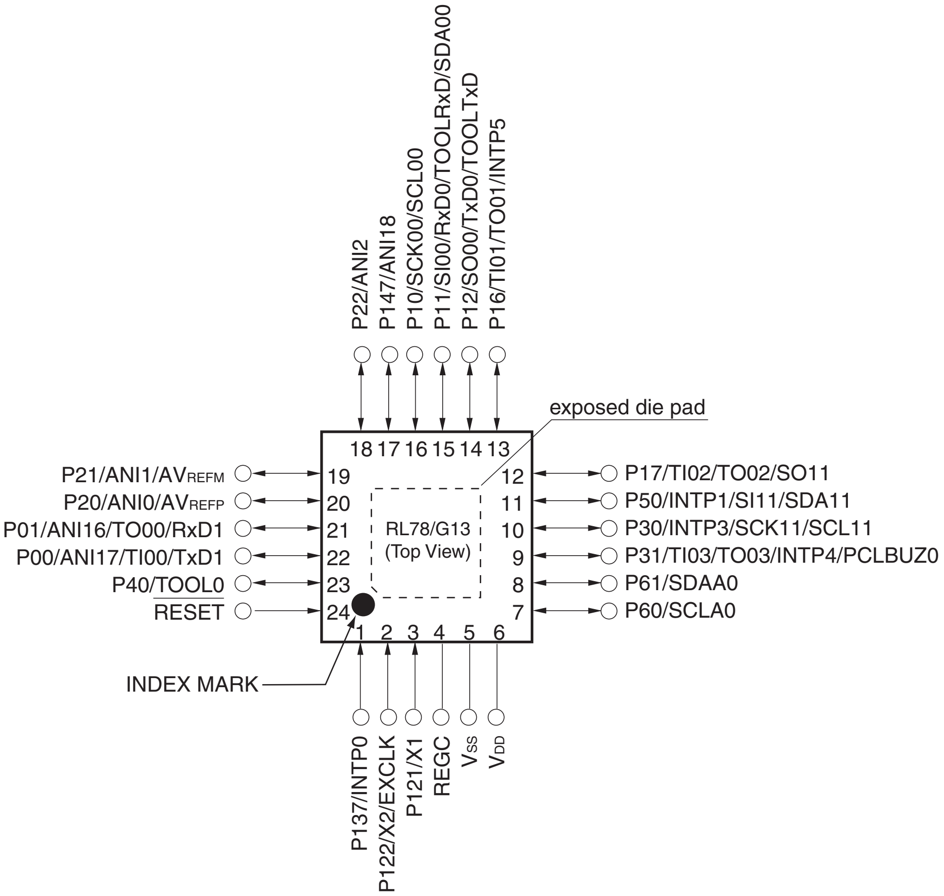


| **Details** | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 15 |
| Program Memory Size | 48KB (48K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 3K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 6x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 24-WFQFN Exposed Pad |
| Supplier Device Package | 24-HWQFN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1007dana-w0 |

### 1.3.2 24-pin products

- 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)

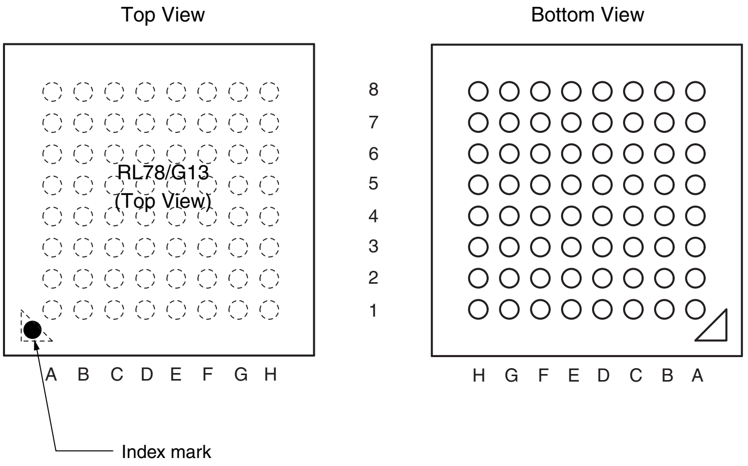


**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** It is recommended to connect an exposed die pad to $V_{SS}$.

- 64-pin plastic VFBGA (4 × 4 mm, 0.4 mm pitch)



| Pin No. | Name | Pin No. | Name | Pin No. | Name | Pin No. | Name |
|---|---|---|---|---|---|---|---|
| A1 | P05/TI05/TO05 | C1 | P51/INTP2/SO11 | E1 | P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04) | G1 | P146 |
| A2 | P30/INTP3/RTC1HZ/SCK11/SCL11 | C2 | P71/KR1/SI21/SDA21 | E2 | P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03) | G2 | P25/ANI5 |
| A3 | P70/KR0/SCK21/SCL21 | C3 | P74/KR4/INTP8/SI01/SDA01 | E3 | P15/SCK20/SCL20/(TI02)/(TO02) | G3 | P24/ANI4 |
| A4 | P75/KR5/INTP9/SCK01/SCL01 | C4 | P52/(INTP10) | E4 | P16/TI01/TO01/INTP5/(SI00)/(RxD0) | G4 | P22/ANI2 |
| A5 | P77/KR7/INTP11/(TxD2) | C5 | P53/(INTP11) | E5 | P03/ANI16/SI10/RxD1/SDA10 | G5 | P130 |
| A6 | P61/SDAA0 | C6 | P63 | E6 | P41/TI07/TO07 | G6 | P02/ANI17/SO10/TxD1 |
| A7 | P60/SCLA0 | C7 | $V_{SS}$ | E7 | $\overline{\text{RESET}}$ | G7 | P00/TI00 |
| A8 | $EV_{DD0}$ | C8 | P121/X1 | E8 | P137/INTP0 | G8 | P124/XT2/EXCLKS |
| B1 | P50/INTP1/SI11/SDA11 | D1 | P55/(PCLBUZ1)/(SCK00) | F1 | P10/SCK00/SCL00/(TI07)/(TO07) | H1 | P147/ANI18 |
| B2 | P72/KR2/SO21 | D2 | P06/TI06/TO06 | F2 | P11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06) | H2 | P27/ANI7 |
| B3 | P73/KR3/SO01 | D3 | P17/TI02/TO02/(SO00)/(TxD0) | F3 | P12/SO00/TxD0/TOOLTxD/(INTP5)/(TI05)/(TO05) | H3 | P26/ANI6 |
| B4 | P76/KR6/INTP10/(RxD2) | D4 | P54 | F4 | P21/ANI1/$AV_{REFM}$ | H4 | P23/ANI3 |
| B5 | P31/TI03/TO03/INTP4/(PCLBUZ0) | D5 | P42/TI04/TO04 | F5 | P04/SCK10/SCL10 | H5 | P20/ANI0/$AV_{REFP}$ |
| B6 | P62 | D6 | P40/TOOL0 | F6 | P43 | H6 | P141/PCLBUZ1/INTP7 |
| B7 | $V_{DD}$ | D7 | REGC | F7 | P01/TO00 | H7 | P140/PCLBUZ0/INTP6 |
| B8 | $EV_{SS0}$ | D8 | P122/X2/EXCLK | F8 | P123/XT1 | H8 | P120/ANI19 |

**Cautions 1. Make $EV_{SS0}$ pin the same potential as $V_{SS}$ pin.**

**2. Make $V_{DD}$ pin the potential that is higher than $EV_{DD0}$ pin.**

**3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 $\mu$F).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the $V_{DD}$ and $EV_{DD0}$ pins and connect the $V_{SS}$ and $EV_{SS0}$ pins to separate ground lines.

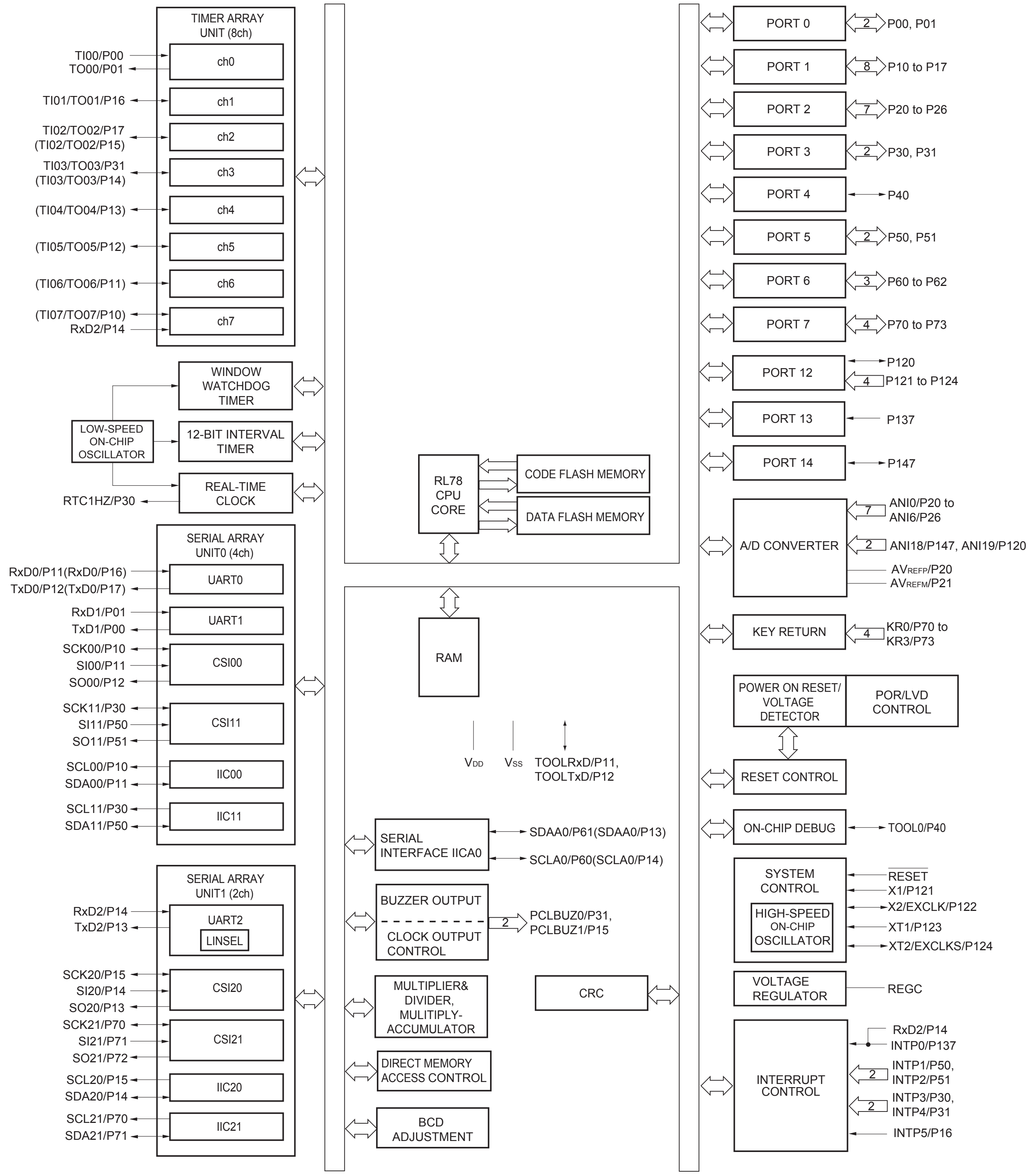
**3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.4 Pin Identification

| | |
|---|---|
| ANI0 to ANI14,<br>ANI16 to ANI26: | Analog input |
| $\text{AV}_{\text{REFM}}$: | A/D converter reference potential (– side) input |
| $\text{AV}_{\text{REFP}}$: | A/D converter reference potential (+ side) input |
| $\text{EV}_{\text{DD0}}$, $\text{EV}_{\text{DD1}}$: | Power supply for port |
| $\text{EV}_{\text{SS0}}$, $\text{EV}_{\text{SS1}}$: | Ground for port |
| EXCLK: | External clock input (Main system clock) |
| EXCLKS: | External clock input (Subsystem clock) |
| INTP0 to INTP11: | Interrupt request from peripheral |
| KR0 to KR7: | Key return |
| P00 to P07: | Port 0 |
| P10 to P17: | Port 1 |
| P20 to P27: | Port 2 |
| P30 to P37: | Port 3 |
| P40 to P47: | Port 4 |
| P50 to P57: | Port 5 |
| P60 to P67: | Port 6 |
| P70 to P77: | Port 7 |
| P80 to P87: | Port 8 |
| P90 to P97: | Port 9 |
| P100 to P106: | Port 10 |
| P110 to P117: | Port 11 |
| P120 to P127: | Port 12 |
| P130, P137: | Port 13 |
| P140 to P147: | Port 14 |
| P150 to P156: | Port 15 |
| PCLBUZ0, PCLBUZ1: | Programmable clock output/buzzer output |

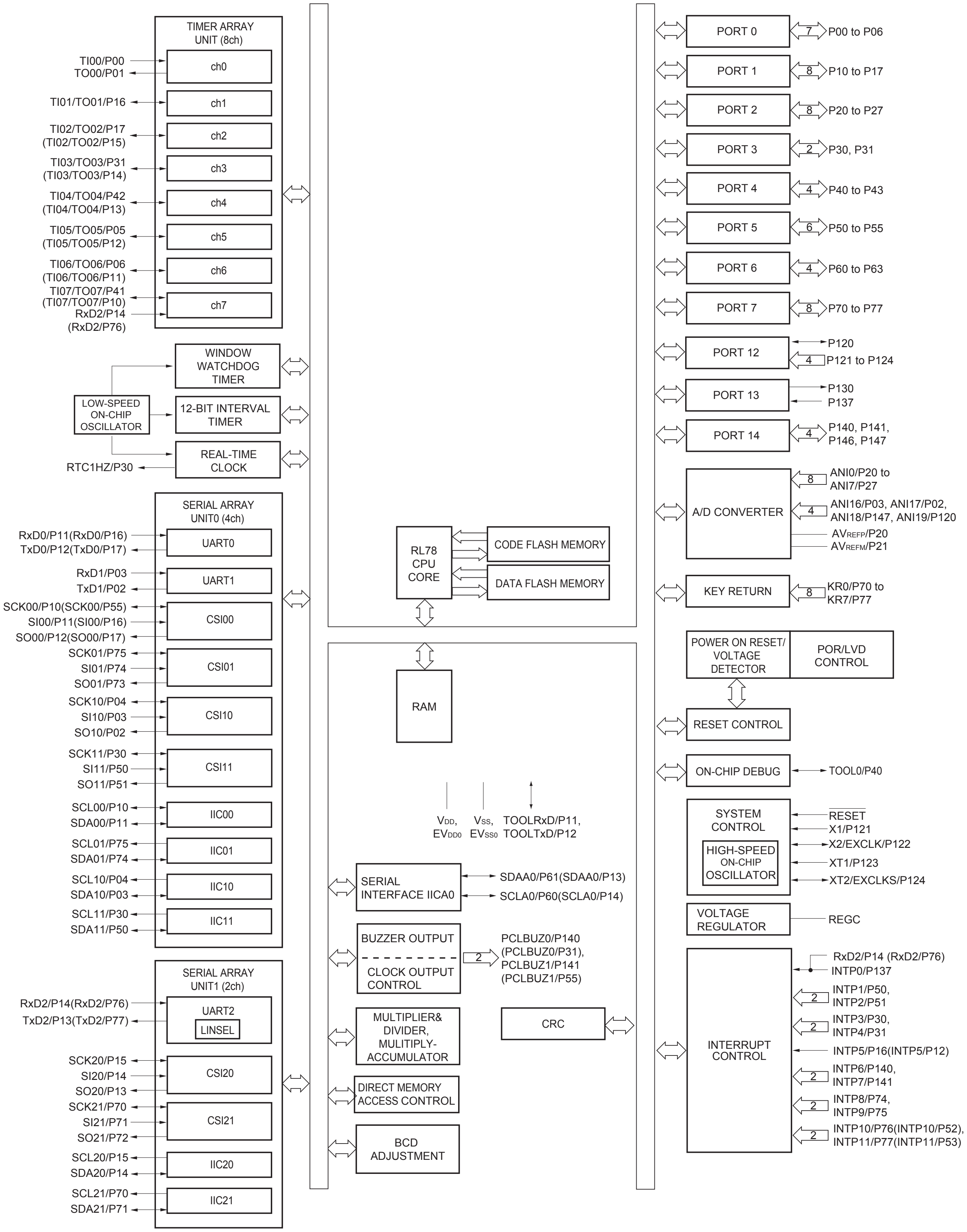
| | |
|---|---|
| REGC: | Regulator capacitance |
| $\overline{\text{RESET}}$: | Reset |
| RTC1HZ: | Real-time clock correction clock (1 Hz) output |
| RxD0 to RxD3: | Receive data |
| SCK00, SCK01, SCK10,<br>SCK11, SCK20, SCK21,<br>SCLA0, SCLA1: | Serial clock input/output |
| SCLA0, SCLA1, SCL00,<br>SCL01, SCL10, SCL11,<br>SCL20,SCL21, SCL30,<br>SCL31: | Serial clock output |
| SDAA0, SDAA1, SDA00,<br>SDA01,SDA10, SDA11,<br>SDA20,SDA21, SDA30,<br>SDA31: | Serial data input/output |
| SI00, SI01, SI10, SI11,<br>SI20, SI21, SI30, SI31: | Serial data input |
| SO00, SO01, SO10,<br>SO11, SO20, SO21,<br>SO30, SO31: | Serial data output |
| TI00 to TI07,<br>TI10 to TI17: | Timer input |
| TO00 to TO07,<br>TO10 to TO17: | Timer output |
| TOOL0: | Data input/output for tool |
| TOOLRxD, TOOLTxD: | Data input/output for external device |
| TxD0 to TxD3: | Transmit data |
| $\text{V}_{\text{DD}}$: | Power supply |
| $\text{V}_{\text{SS}}$: | Ground |
| X1, X2: | Crystal oscillator (main system clock) |
| XT1, XT2: | Crystal oscillator (subsystem clock) |

### 1.5.7 40-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.5.11 64-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 2.1 Absolute Maximum Ratings

### Absolute Maximum Ratings ($T_A$ = 25°C) (1/2)

| Parameter | Symbols | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | −0.5 to +6.5 | V |
| | $EV_{DD0}$, $EV_{DD1}$ | $EV_{DD0} = EV_{DD1}$ | −0.5 to +6.5 | V |
| | $EV_{SS0}$, $EV_{SS1}$ | $EV_{SS0} = EV_{SS1}$ | −0.5 to +0.3 | V |
| REGC pin input voltage | $V_{IREGC}$ | REGC | −0.3 to +2.8<br>and −0.3 to $V_{DD}$ +0.3 Note 1 | V |
| Input voltage | $V_{I1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | −0.3 to $EV_{DD0}$ +0.3<br>and −0.3 to $V_{DD}$ +0.3 Note 2 | V |
| | $V_{I2}$ | P60 to P63 (N-ch open-drain) | −0.3 to +6.5 | V |
| | $V_{I3}$ | P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | −0.3 to $V_{DD}$ +0.3 Note 2 | V |
| Output voltage | $V_{O1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | −0.3 to $EV_{DD0}$ +0.3<br>and −0.3 to $V_{DD}$ +0.3 Note 2 | V |
| | $V_{O2}$ | P20 to P27, P150 to P156 | −0.3 to $V_{DD}$ +0.3 Note 2 | V |
| Analog input voltage | $V_{AI1}$ | ANI16 to ANI26 | −0.3 to $EV_{DD0}$ +0.3<br>and −0.3 to $AV_{REF}(+)$ +0.3 Notes 2, 3 | V |
| | $V_{AI2}$ | ANI0 to ANI14 | −0.3 to $V_{DD}$ +0.3<br>and −0.3 to $AV_{REF}(+)$ +0.3 Notes 2, 3 | V |

**Notes 1.** Connect the REGC pin to Vss via a capacitor (0.47 to 1 $\mu$F). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**2.** Must be 6.5 V or lower.

**3.** Do not exceed $AV_{REF}(+)$ + 0.3 V in case of A/D conversion target pin.

**Caution** **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**2.** $AV_{REF}(+)$ : + side reference voltage of the A/D converter.

**3.** $V_{SS}$ : Reference voltage

**Notes 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**4.** When high-speed system clock and subsystem clock are stopped.

**5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

| | |
|---|---|
| HS (high-speed main) mode: | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz |
| | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz |
| LS (low-speed main) mode: | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz |
| LV (low-voltage main) mode: | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz |

**8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current . However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**4.** When high-speed system clock and subsystem clock are stopped.

**5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: $2.7\ V \le V_{DD} \le 5.5\ V$@1 MHz to 32 MHz
$2.4\ V \le V_{DD} \le 5.5\ V$@1 MHz to 16 MHz
LS (low-speed main) mode: $1.8\ V \le V_{DD} \le 5.5\ V$ @1 MHz to 8 MHz
LV (low-voltage main) mode: $1.6\ V \le V_{DD} \le 5.5\ V$@1 MHz to 4 MHz

**8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

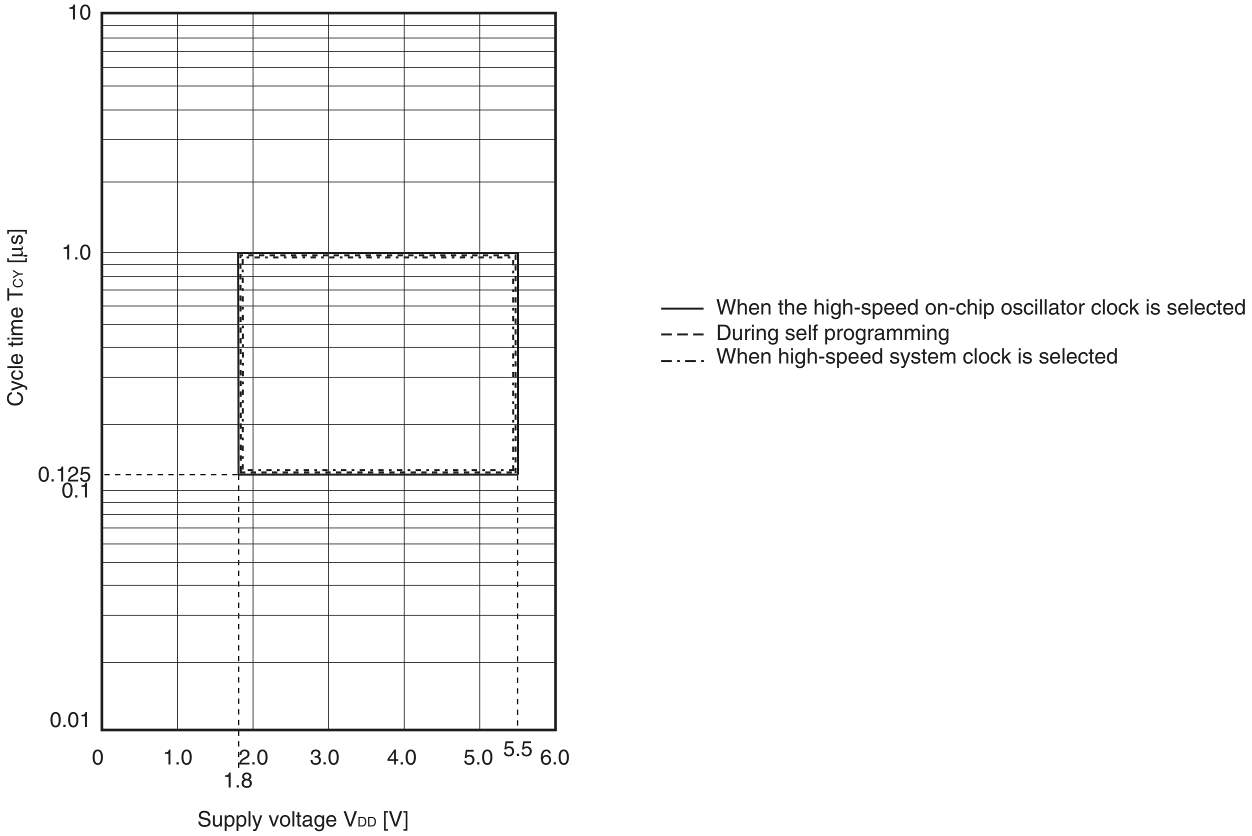
**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

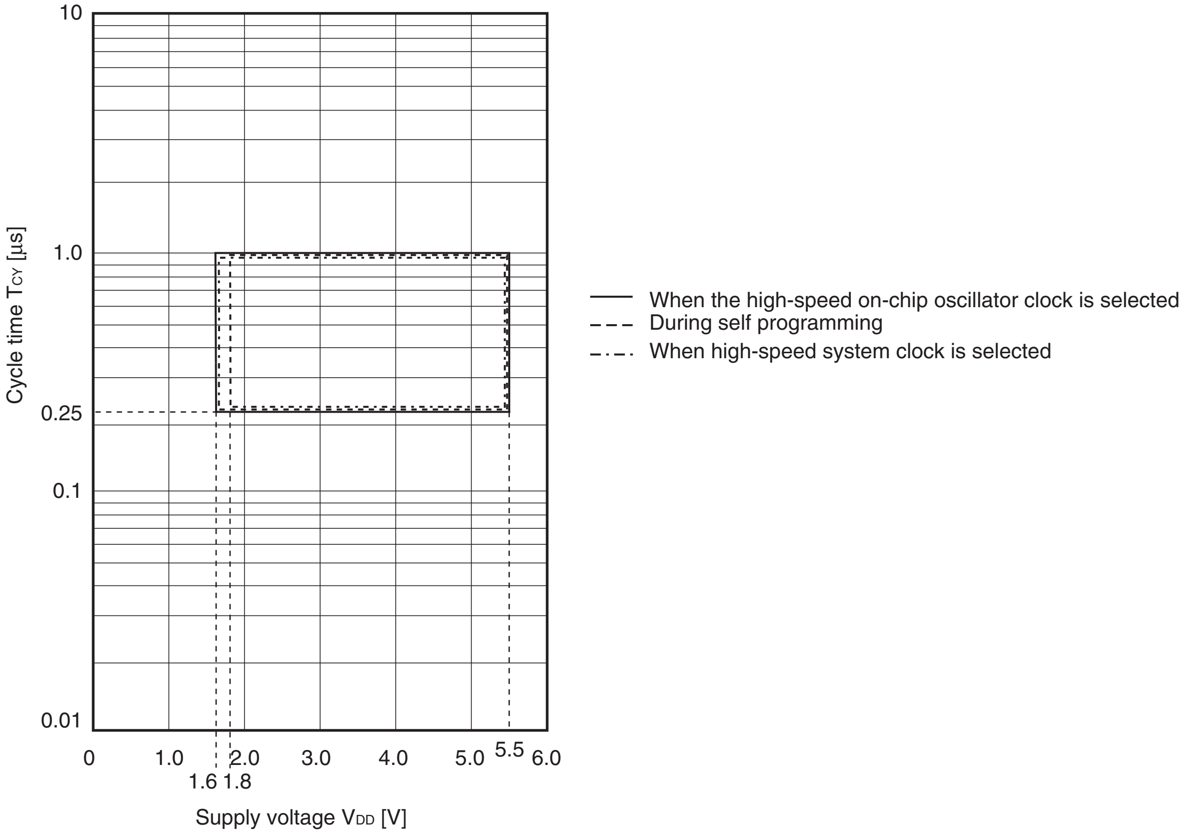
**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

$T_{CY}$ vs $V_{DD}$ (LS (low-speed main) mode)



$T_{CY}$ vs $V_{DD}$ (LV (low-voltage main) mode)



### (3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output) ($T_A$ = −40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 4/$f_{CLK}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 125 | | 500 | | 1000 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | 500 | | 1000 | | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 500 | | 500 | | 1000 | | ns |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1000 | | 1000 | | 1000 | | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 1000 | | 1000 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 12 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 18 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 38 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 – 100 | | $t_{KCY1}$/2 – 100 | | $t_{KCY1}$/2 – 100 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | $t_{KCY1}$/2 – 100 | | $t_{KCY1}$/2 – 100 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 44 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 44 | | 110 | | 110 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 75 | | 110 | | 110 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 110 | | 110 | | 110 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 220 | | 220 | | 220 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 220 | | 220 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 19 | | 19 | | 19 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 19 | | 19 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V<br>C = 30 pF Note 4 | | | 25 | | 25 | | 25 | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V<br>C = 30 pF Note 4 | | | — | | 25 | | 25 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

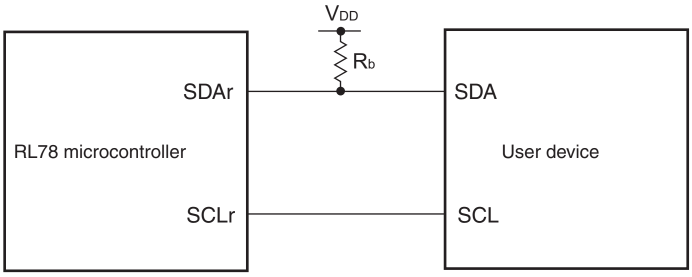
**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

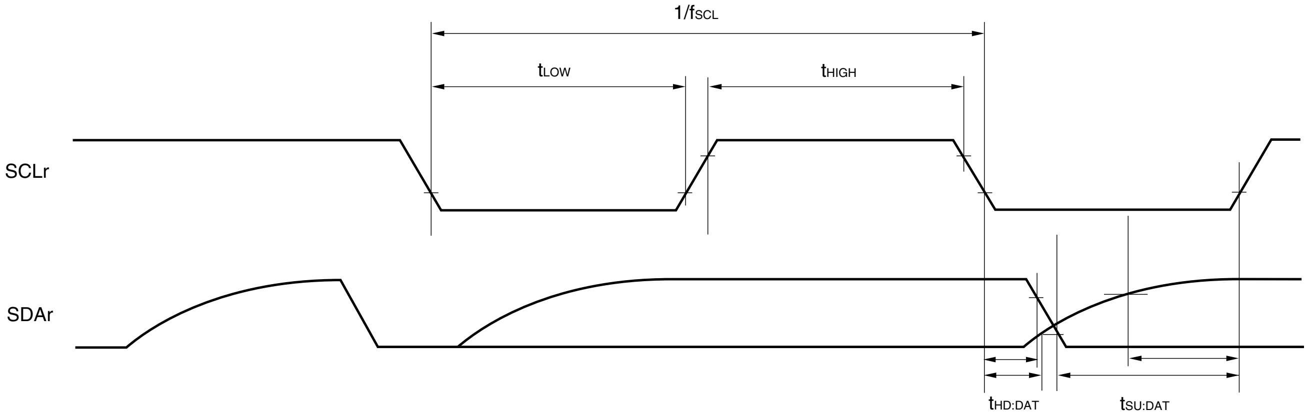
**4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Simplified $I^2C$ mode mode connection diagram (during communication at same potential)**



**Simplified $I^2C$ mode serial transfer timing (during communication at same potential)**



**Remarks 1.** $R_b$[Ω]:Communication line (SDAr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance

**2.** r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14), h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)

**3.** $f_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),

n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)

**($T_A = -40$ to $+85°C$, $1.8\ V \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\ V$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\ V$)**

| Parameter | Symbol | Conditions | | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate | | Reception | $4.0\ V \leq EV_{DD0} \leq 5.5\ V$,<br>$2.7\ V \leq V_b \leq 4.0\ V$ | | | $f_{MCK}/6$ Note 1 | | $f_{MCK}/6$ Note 1 | | $f_{MCK}/6$ Note 1 | bps |
| | | | | Theoretical value of the maximum transfer rate<br>$f_{MCK} = f_{CLK}$ Note 4 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | | $2.7\ V \leq EV_{DD0} < 4.0\ V$,<br>$2.3\ V \leq V_b \leq 2.7\ V$ | | | $f_{MCK}/6$ Note 1 | | $f_{MCK}/6$ Note 1 | | $f_{MCK}/6$ Note 1 | bps |
| | | | | Theoretical value of the maximum transfer rate<br>$f_{MCK} = f_{CLK}$ Note 4 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | | $1.8\ V \leq EV_{DD0} < 3.3\ V$,<br>$1.6\ V \leq V_b \leq 2.0\ V$ | | | $f_{MCK}/6$ Notes 1 to 3 | | $f_{MCK}/6$ Notes 1, 2 | | $f_{MCK}/6$ Notes 1, 2 | bps |
| | | | | Theoretical value of the maximum transfer rate<br>$f_{MCK} = f_{CLK}$ Note 4 | | 5.3 | | 1.3 | | 0.6 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**2.** Use it with $EV_{DD0} \geq V_b$.

**3.** The following conditions are required for low voltage interface when $E_{VDD0} < V_{DD}$.
$2.4\ V \leq EV_{DD0} < 2.7\ V$ : MAX. 2.6 Mbps
$1.8\ V \leq EV_{DD0} < 2.4\ V$ : MAX. 1.3 Mbps

**4.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:

| | |
|---|---|
| HS (high-speed main) mode: | 32 MHz ($2.7\ V \leq V_{DD} \leq 5.5\ V$) |
| | 16 MHz ($2.4\ V \leq V_{DD} \leq 5.5\ V$) |
| LS (low-speed main) mode: | 8 MHz ($1.8\ V \leq V_{DD} \leq 5.5\ V$) |
| LV (low-voltage main) mode: | 4 MHz ($1.6\ V \leq V_{DD} \leq 5.5\ V$) |

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (When 20- to 52-pin products)/$EV_{DD}$ tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remarks 1.** $V_b$[V]: Communication line voltage

**2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

**3.** $f_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

**4.** UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

### (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

**($T_A$ = −40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp high-/low-level width | $t_{KH2}$,<br>$t_{KL2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V | $t_{KCY2}/2 - 12$ | | $t_{KCY2}/2 - 50$ | | $t_{KCY2}/2 - 50$ | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V,<br>2.3 V ≤ $V_b$ ≤ 2.7 V | $t_{KCY2}/2 - 18$ | | $t_{KCY2}/2 - 50$ | | $t_{KCY2}/2 - 50$ | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V,<br>1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | $t_{KCY2}/2 - 50$ | | $t_{KCY2}/2 - 50$ | | $t_{KCY2}/2 - 50$ | | ns |
| SIp setup time (to SCKp↑) Note 3 | $t_{SIK2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V | $1/f_{MCK} + 20$ | | $1/f_{MCK} + 30$ | | $1/f_{MCK} + 30$ | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V,<br>2.3 V ≤ $V_b$ ≤ 2.7 V | $1/f_{MCK} + 20$ | | $1/f_{MCK} + 30$ | | $1/f_{MCK} + 30$ | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V,<br>1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | $1/f_{MCK} + 30$ | | $1/f_{MCK} + 30$ | | $1/f_{MCK} + 30$ | | ns |
| SIp hold time (from SCKp↑) Note 4 | $t_{KSI2}$ | | $1/f_{MCK} + 31$ | | $1/f_{MCK} + 31$ | | $1/f_{MCK} + 31$ | | ns |
| Delay time from SCKp↓ to SOp output Note 5 | $t_{KSO2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $2/f_{MCK} + 120$ | | $2/f_{MCK} + 573$ | | $2/f_{MCK} + 573$ | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V,<br>$C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $2/f_{MCK} + 214$ | | $2/f_{MCK} + 573$ | | $2/f_{MCK} + 573$ | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V,<br>1.6 V ≤ $V_b$ ≤ 2.0 V Note 2,<br>$C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $2/f_{MCK} + 573$ | | $2/f_{MCK} + 573$ | | $2/f_{MCK} + 573$ | ns |

**Notes**
1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps
2. Use it with $EV_{DD0}$ ≥ $V_b$.
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution** **Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

### LVD Detection Voltage of Interrupt & Reset Mode

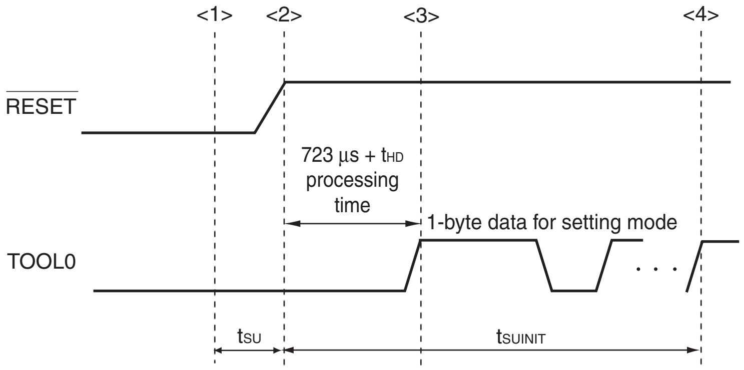
**($T_A$ = –40 to +85°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Interrupt and reset mode | $V_{LVDA0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 0, 0, falling reset voltage | | | 1.60 | 1.63 | 1.66 | V |
| | $V_{LVDA1}$ | | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 1.74 | 1.77 | 1.81 | V |
| | | | | Falling interrupt voltage | 1.70 | 1.73 | 1.77 | V |
| | $V_{LVDA2}$ | | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 1.84 | 1.88 | 1.91 | V |
| | | | | Falling interrupt voltage | 1.80 | 1.84 | 1.87 | V |
| | $V_{LVDA3}$ | | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVDB0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 0, 1, falling reset voltage | | | 1.80 | 1.84 | 1.87 | V |
| | $V_{LVDB1}$ | | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 1.94 | 1.98 | 2.02 | V |
| | | | | Falling interrupt voltage | 1.90 | 1.94 | 1.98 | V |
| | $V_{LVDB2}$ | | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 2.05 | 2.09 | 2.13 | V |
| | | | | Falling interrupt voltage | 2.00 | 2.04 | 2.08 | V |
| | $V_{LVDB3}$ | | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 3.07 | 3.13 | 3.19 | V |
| | | | | Falling interrupt voltage | 3.00 | 3.06 | 3.12 | V |
| | $V_{LVDC0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 0, falling reset voltage | | | 2.40 | 2.45 | 2.50 | V |
| | $V_{LVDC1}$ | | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 2.56 | 2.61 | 2.66 | V |
| | | | | Falling interrupt voltage | 2.50 | 2.55 | 2.60 | V |
| | $V_{LVDC2}$ | | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 2.66 | 2.71 | 2.76 | V |
| | | | | Falling interrupt voltage | 2.60 | 2.65 | 2.70 | V |
| | $V_{LVDC3}$ | | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 3.68 | 3.75 | 3.82 | V |
| | | | | Falling interrupt voltage | 3.60 | 3.67 | 3.74 | V |
| | $V_{LVDD0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 1, falling reset voltage | | | 2.70 | 2.75 | 2.81 | V |
| | $V_{LVDD1}$ | | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVDD2}$ | | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 2.96 | 3.02 | 3.08 | V |
| | | | | Falling interrupt voltage | 2.90 | 2.96 | 3.02 | V |
| | $V_{LVDD3}$ | | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 3.98 | 4.06 | 4.14 | V |
| | | | | Falling interrupt voltage | 3.90 | 3.98 | 4.06 | V |

## 2.10 Timing of Entry to Flash Memory Programming Modes

**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Time to complete the communication for the initial setting after the external reset is released | $t_{SUINIT}$ | POR and LVD reset must be released before the external reset is released. | | | 100 | ms |
| Time to release the external reset after the TOOL0 pin is set to the low level | $t_{SU}$ | POR and LVD reset must be released before the external reset is released. | 10 | | | μs |
| Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory) | $t_{HD}$ | POR and LVD reset must be released before the external reset is released. | 1 | | | ms |



<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** $t_{SUINIT}$: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

$t_{SU}$: Time to release the external reset after the TOOL0 pin is set to the low level

$t_{HD}$: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

**Absolute Maximum Ratings ($T_A$ = 25°C) (2/2)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Output current, high | $I_{OH1}$ | Per pin | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | −40 | mA |
| | | Total of all pins<br>−170 mA | P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 | −70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 | −100 | mA |
| | $I_{OH2}$ | Per pin | P20 to P27, P150 to P156 | −0.5 | mA |
| | | Total of all pins | | −2 | mA |
| Output current, low | $I_{OL1}$ | Per pin | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 40 | mA |
| | | Total of all pins<br>170 mA | P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 | 70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 | 100 | mA |
| | $I_{OL2}$ | Per pin | P20 to P27, P150 to P156 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | $T_A$ | In normal operation mode | | −40 to +105 | °C |
| | | In flash memory programming mode | | | |
| Storage temperature | $T_{stg}$ | | | −65 to +150 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = −40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low[Note 1] | $I_{OL1}$ | Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | | | | 8.5 [Note 2] | mA |
| | | Per pin for P60 to P63 | | | | 15.0 [Note 2] | mA |
| | | Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70% [Note 3]) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 40.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 15.0 | mA |
| | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | | | 9.0 | mA |
| | | Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70% [Note 3]) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 40.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 35.0 | mA |
| | | | 2,4 V ≤ $EV_{DD0}$ < 2.7 V | | | 20.0 | mA |
| | | Total of all pins (When duty ≤ 70% [Note 3]) | | | | 80.0 | mA |
| | $I_{OL2}$ | Per pin for P20 to P27, P150 to P156 | | | | 0.4 [Note 2] | mA |
| | | Total of all pins (When duty ≤ 70%[Note 3]) | 2,4 V ≤ $V_{DD}$ ≤ 5.5 V | | | 5.0 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the $EV_{SS0}$, $EV_{SS1}$ and $V_{SS}$ pin.

**2.** Do not exceed the total current value.

**3.** Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OL}$ = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $V_{BGR}$[Note 3], Reference voltage (–) = $AV_{REFM}$[Note 4] = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | 8 | | bit |
| Conversion time | $t_{CONV}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error[Notes 1, 2] | $E_{ZS}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| Integral linearity error[Note 1] | ILE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Differential linearity error[Note 1] | DLE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±1.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $V_{BGR}$[Note 3] | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

**4.** When reference voltage (–) = $V_{SS}$, the MAX. values are as follows.
Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = $AV_{REFM}$.
Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = $AV_{REFM}$.
Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = $AV_{REFM}$.

## 3.6.2 Temperature sensor/internal reference voltage characteristics

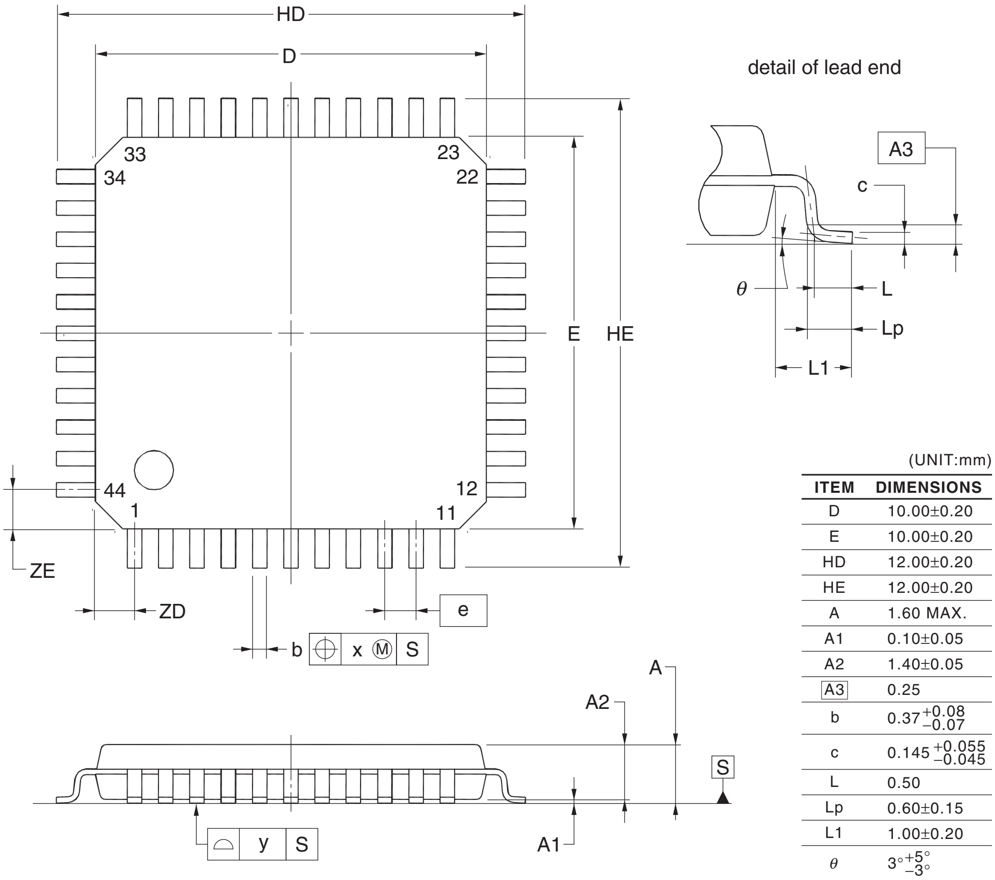
**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor that depends on the temperature | | –3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 5 | | | μs |

## 4.8 44-pin Products

R5F100FAAFP, R5F100FCAFP, R5F100FDAFP, R5F100FEAFP, R5F100FFAFP, R5F100FGAFP,
R5F100FHAFP, R5F100FJAFP, R5F100FKAFP, R5F100FLAFP
R5F101FAAFP, R5F101FCAFP, R5F101FDAFP, R5F101FEAFP, R5F101FFAFP, R5F101FGAFP,
R5F101FHAFP, R5F101FJAFP, R5F101FKAFP, R5F101FLAFP
R5F100FADFP, R5F100FCDFP, R5F100FDDFP, R5F100FEDFP, R5F100FFDFP, R5F100FGDFP,
R5F100FHDFP, R5F100FJDFP, R5F100FKDFP, R5F100FLDFP
R5F101FADFP, R5F101FCDFP, R5F101FDDFP, R5F101FEDFP, R5F101FFDFP, R5F101FGDFP,
R5F101FHDFP, R5F101FJDFP, R5F101FKDFP, R5F101FLDFP
R5F100FAGFP, R5F100FCGFP, R5F100FDGFP, R5F100FEGFP, R5F100FFGFP, R5F100FGGFP,
R5F100FHGFP, R5F100FJGFP

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP44-10x10-0.80 | PLQP0044GC-A | P44GB-80-UES-2 | 0.36 |



(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 10.00±0.20 |
| E | 10.00±0.20 |
| HD | 12.00±0.20 |
| HE | 12.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | $0.37^{+0.08}_{-0.07}$ |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3°^{+5°}_{-3°}$ |
| e | 0.80 |
| x | 0.20 |
| y | 0.10 |
| ZD | 1.00 |
| ZE | 1.00 |

**NOTE**
Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

| Rev. | Date | Description | |
|---|---|---|---|
| | | **Page** | **Summary** |
| 1.00 | Feb 29, 2012 | - | First Edition issued |
| 2.00 | Oct 12, 2012 | 7 | Figure 1-1. Part Number, Memory Size, and Package of RL78/G13: Pin count corrected. |
| | | 25 | 1.4 Pin Identification: Description of pins INTP0 to INTP11 corrected. |
| | | 40, 42, 44 | 1.6 Outline of Functions: Descriptions of Subsystem clock, Low-speed on-chip oscillator, and General-purpose register corrected. |
| | | 41, 43, 45 | 1.6 Outline of Functions: Lists of Descriptions changed. |
| | | 59, 63, 67 | Descriptions of Note 8 in a table corrected. |
| | | 68 | (4) Common to RL78/G13 all products: Descriptions of Notes corrected. |
| | | 69 | 2.4 AC Characteristics: Symbol of external system clock frequency corrected. |
| | | 96 to 98 | 2.6.1 A/D converter characteristics: Notes of overall error corrected. |
| | | 100 | 2.6.2 Temperature sensor characteristics: Parameter name corrected. |
| | | 104 | 2.8 Flash Memory Programming Characteristics: Incorrect descriptions corrected. |
| | | 116 | 3.10 52-pin products: Package drawings of 52-pin products corrected. |
| | | 120 | 3.12 80-pin products: Package drawings of 80-pin products corrected. |
| 3.00 | Aug 02, 2013 | 1 | Modification of 1.1 Features |
| | | 3 | Modification of 1.2 List of Part Numbers |
| | | 4 to 15 | Modification of Table 1-1. List of Ordering Part Numbers, note, and caution |
| | | 16 to 32 | Modification of package type in 1.3.1 to 1.3.14 |
| | | 33 | Modification of description in 1.4 Pin Identification |
| | | 48, 50, 52 | Modification of caution, table, and note in 1.6 Outline of Functions |
| | | 55 | Modification of description in table of Absolute Maximum Ratings ($T_A$ = 25°C) |
| | | 57 | Modification of table, note, caution, and remark in 2.2.1 X1, XT1 oscillator characteristics |
| | | 57 | Modification of table in 2.2.2 On-chip oscillator characteristics |
| | | 58 | Modification of note 3 of table (1/5) in 2.3.1 Pin characteristics |
| | | 59 | Modification of note 3 of table (2/5) in 2.3.1 Pin characteristics |
| | | 63 | Modification of table in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products |
| | | 64 | Modification of notes 1 and 4 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products |
| | | 65 | Modification of table in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products |
| | | 66 | Modification of notes 1, 5, and 6 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products |
| | | 68 | Modification of notes 1 and 4 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products |
| | | 70 | Modification of notes 1, 5, and 6 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products |
| | | 72 | Modification of notes 1 and 4 in (3) Flash ROM: 384 to 512 KB of 44- to 100-pin products |
| | | 74 | Modification of notes 1, 5, and 6 in (3) Flash ROM: 384 to 512 KB of 44- to 100-pin products |
| | | 75 | Modification of (4) Peripheral Functions (Common to all products) |
| | | 77 | Modification of table in 2.4 AC Characteristics |
| | | 78, 79 | Addition of Minimum Instruction Execution Time during Main System Clock Operation |
| | | 80 | Modification of figures of AC Timing Test Points and External System Clock Timing |