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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	15
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 6x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WQFN Exposed Pad
Supplier Device Package	24-HWQFN (4x4)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1007eana-u0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1007eana-u0</a>

## 1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/G13



- Notes**
1. Products only for "A: Consumer applications ( $T_A = -40$  to  $+85^\circ\text{C}$ )", and "G: Industrial applications ( $T_A = -40$  to  $+105^\circ\text{C}$ )"
  2. Products only for "A: Consumer applications ( $T_A = -40$  to  $+85^\circ\text{C}$ )", and "D: Industrial applications ( $T_A = -40$  to  $+85^\circ\text{C}$ )"

Table 1-1. List of Ordering Part Numbers

(12/12)

Pin count	Package	Data flash	Fields of Application <sup>Note</sup>	Ordering Part Number
128 pins	128-pin plastic LFQFP (14 × 20 mm, 0.5 mm pitch)	Mounted	A	R5F100SHAFB#V0, R5F100SJAFB#V0, R5F100SKAFB#V0, R5F100SLAFB#V0 R5F100SHAFB#X0, R5F100SJAFB#X0, R5F100SKAFB#X0, R5F100SLAFB#X0
			D	R5F100SHDFB#V0, R5F100SJDFB#V0, R5F100SKDFB#V0, R5F100SLDFB#V0 R5F100SHDFB#X0, R5F100SJDFB#X0, R5F100SKDFB#X0, R5F100SLDFB#X0
		Not mounted	A	R5F101SHAFB#V0, R5F101SJAFB#V0, R5F101SKAFB#V0, R5F101SLAFB#V0 R5F101SHAFB#X0, R5F101SJAFB#X0, R5F101SKAFB#X0, R5F101SLAFB#X0
			D	R5F101SHDFB#V0, R5F101SJDFB#V0, R5F101SKDFB#V0, R5F101SLDFB#V0 R5F101SHDFB#X0, R5F101SJDFB#X0, R5F101SKDFB#X0, R5F101SLDFB#X0

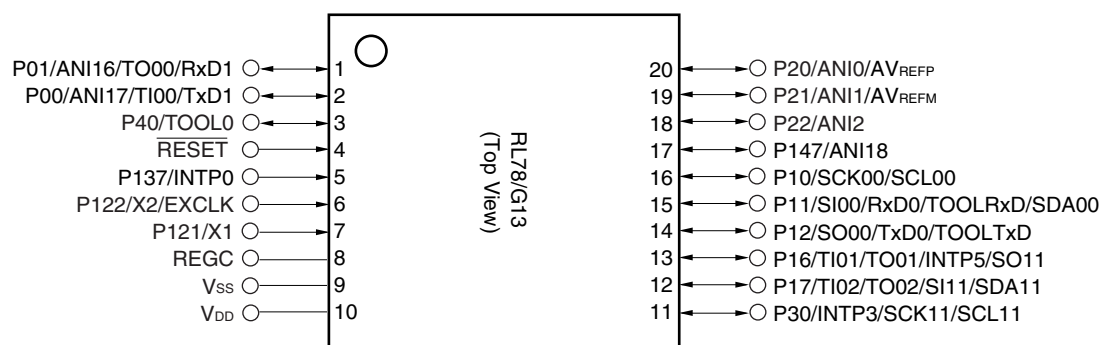
**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

**Caution** The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

### 1.3 Pin Configuration (Top View)

#### 1.3.1 20-pin products

- 20-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)

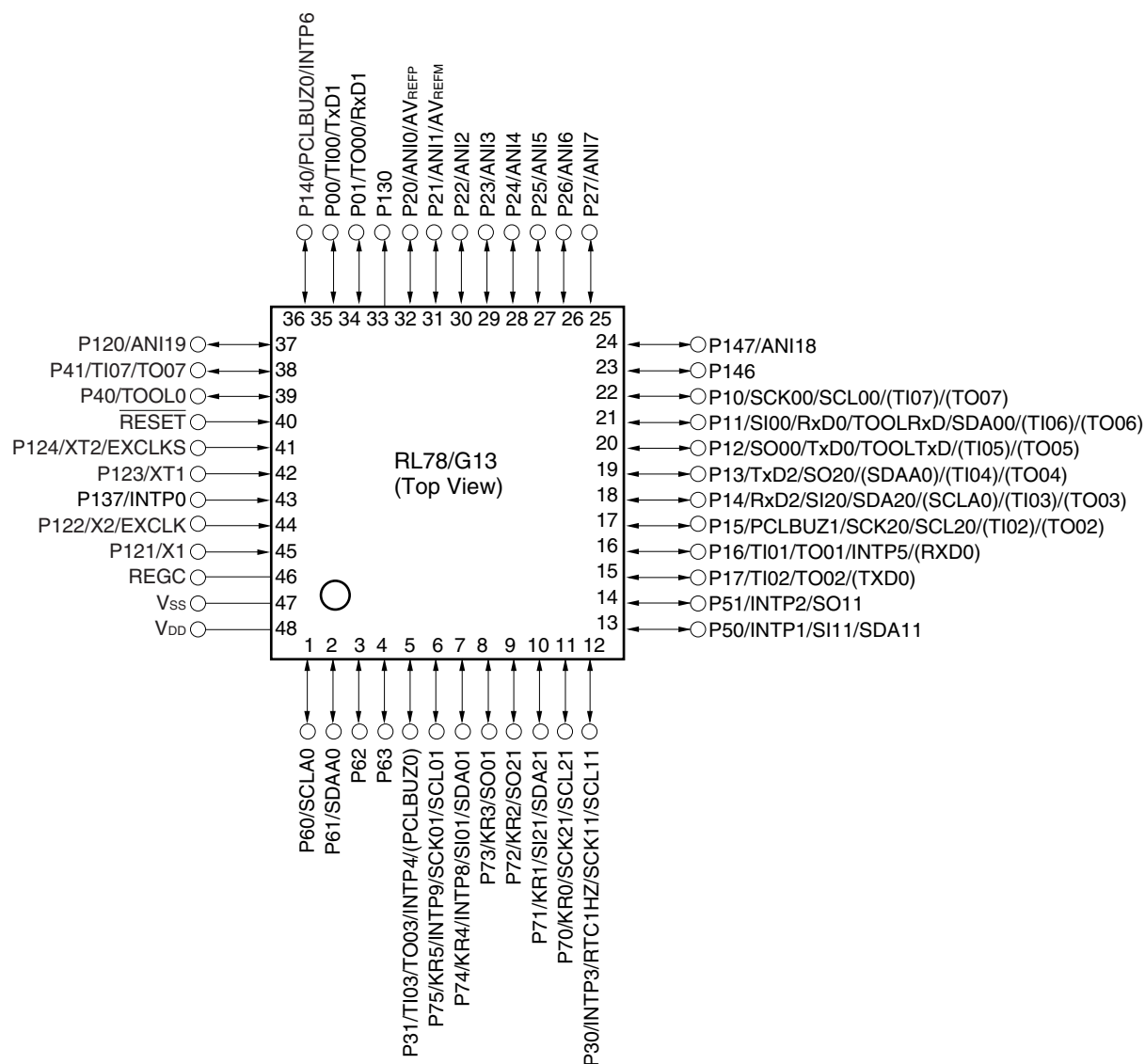


**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F).

**Remark** For pin identification, see 1.4 Pin Identification.

## 1.3.9 48-pin products

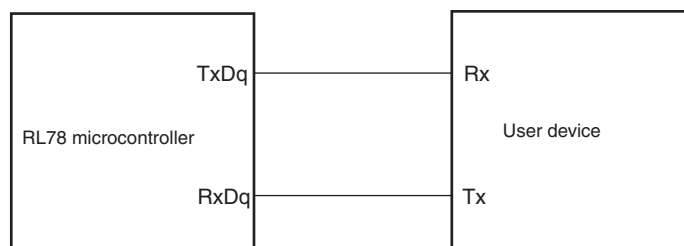
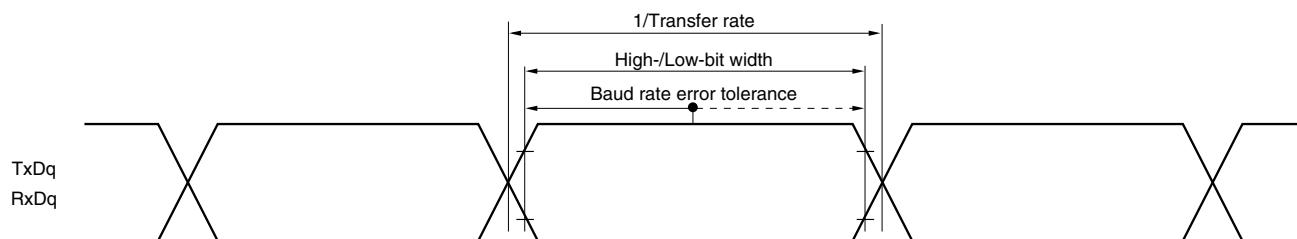
- 48-pin plastic LQFP (7 × 7 mm, 0.5 mm pitch)



**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1  $\mu$ F).

**Remarks 1.** For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

**UART mode connection diagram (during communication at same potential)****UART mode bit width (during communication at same potential) (reference)**

**Remarks 1.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

**2.**  $f_{MCK}$ : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

## (3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t <sub>KCY1</sub>	t <sub>KCY1</sub> ≥ 4/f <sub>CLK</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	125		500		1000		ns
			2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	250		500		1000		ns
			1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	500		500		1000		ns
			1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	1000		1000		1000		ns
			1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	—		1000		1000		ns
SCKp high-/low-level width	t <sub>KH1</sub> , t <sub>KL1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 12		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 18		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 38		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 100		t <sub>KCY1</sub> /2 – 100		t <sub>KCY1</sub> /2 – 100		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		t <sub>KCY1</sub> /2 – 100		t <sub>KCY1</sub> /2 – 100		ns
Slp setup time (to SCKp↑) <small>Note 1</small>	t <sub>SIK1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		44		110		110		ns
		2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		44		110		110		ns
		2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		75		110		110		ns
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		110		110		110		ns
		1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		220		220		220		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		220		220		ns
Slp hold time (from SCKp↑) <small>Note 2</small>	t <sub>KSI1</sub>	1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		19		19		19		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		19		19		ns
Delay time from SCKp↓ to SOp output <small>Note 3</small>	t <sub>KSO1</sub>	1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V C = 30 pF <small>Note 4</small>			25		25		25	ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V C = 30 pF <small>Note 4</small>			—		25		25	ns

- Notes**
1. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The Slp setup time becomes “to SCKp↓” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  2. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The Slp hold time becomes “from SCKp↓” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  3. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The delay time to SOp output becomes “from SCKp↑” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  4. C is the load capacitance of the SCKp and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

## (4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2)

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

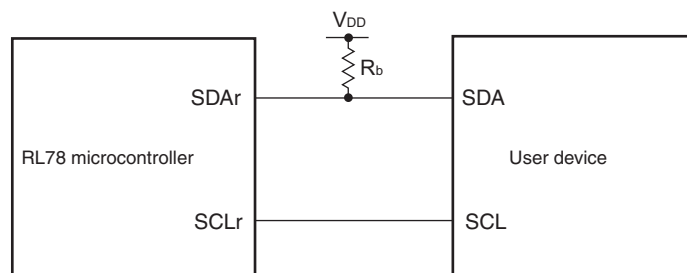
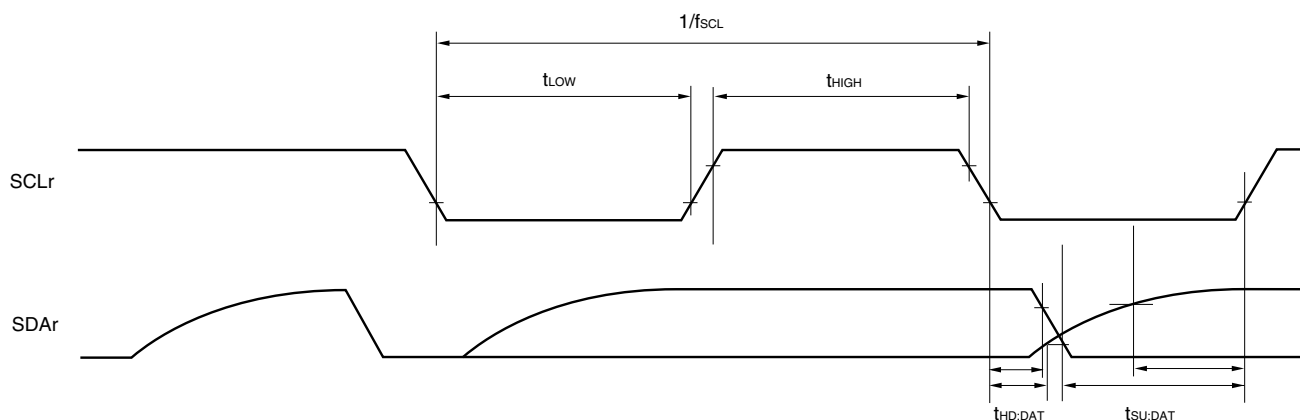
Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) <sup>Note 1</sup>	t <sub>SIK2</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +2 0		1/f <sub>MCK</sub> +30		1/f <sub>MCK</sub> +30		ns
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +3 0		1/f <sub>MCK</sub> +30		1/f <sub>MCK</sub> +30		ns
		1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +4 0		1/f <sub>MCK</sub> +40		1/f <sub>MCK</sub> +40		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		1/f <sub>MCK</sub> +40		1/f <sub>MCK</sub> +40		ns
Slp hold time (from SCKp↑) <sup>Note 2</sup>	t <sub>KSI2</sub>	1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +3 1		1/f <sub>MCK</sub> +31		1/f <sub>MCK</sub> +31		ns
		1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> + 250		1/f <sub>MCK</sub> + 250		1/f <sub>MCK</sub> + 250		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		1/f <sub>MCK</sub> + 250		1/f <sub>MCK</sub> + 250		ns
Delay time from SCKp↓ to SOp output <sup>Note 3</sup>	t <sub>KSO2</sub>	C = 30 pF <sup>Note 4</sup>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		2/f <sub>MCK</sub> + 44		2/f <sub>MCK</sub> + 110		2/f <sub>MCK</sub> + 110	ns
			2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		2/f <sub>MCK</sub> + 75		2/f <sub>MCK</sub> + 110		2/f <sub>MCK</sub> + 110	ns
			1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		2/f <sub>MCK</sub> + 110		2/f <sub>MCK</sub> + 110		2/f <sub>MCK</sub> + 110	ns
			1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		2/f <sub>MCK</sub> + 220		2/f <sub>MCK</sub> + 220		2/f <sub>MCK</sub> + 220	ns
			1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		2/f <sub>MCK</sub> + 220		2/f <sub>MCK</sub> + 220	ns

- Notes**
1. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The Slp setup time becomes “to SCKp↓” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  2. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The Slp hold time becomes “from SCKp↓” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  3. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The delay time to SOp output becomes “from SCKp↑” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  4. C is the load capacitance of the SOp output lines.
  5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

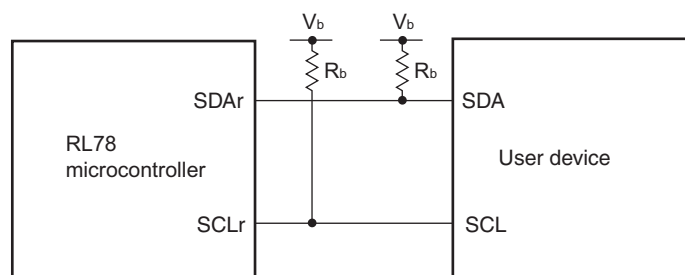
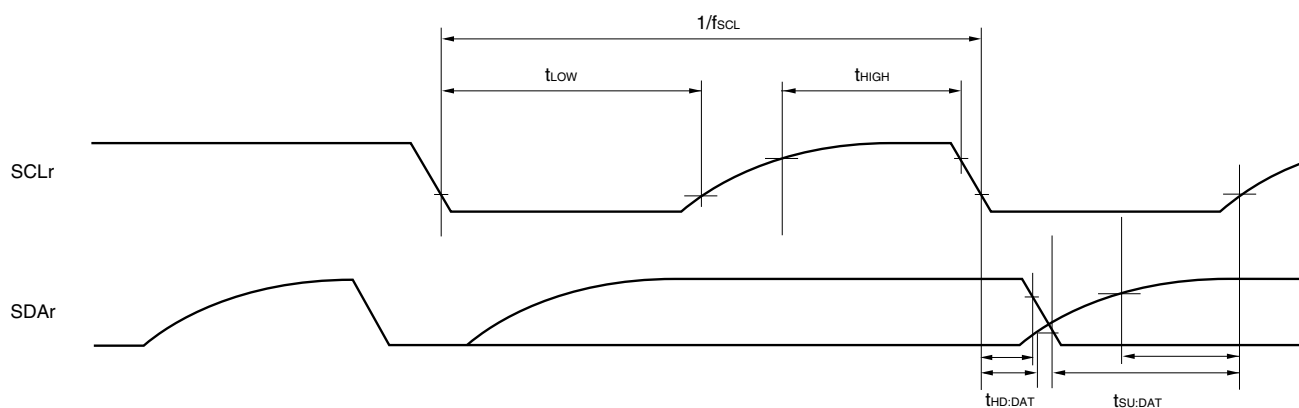
**Caution** Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),  
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)
  2. f<sub>MCK</sub>: Serial array unit operation clock frequency  
(Operation clock to be set by the CKS<sub>mn</sub> bit of serial mode register mn (SMR<sub>mn</sub>). m: Unit number,  
n: Channel number (mn = 00 to 03, 10 to 13))



**Simplified I<sup>2</sup>C mode connection diagram (during communication at same potential)****Simplified I<sup>2</sup>C mode serial transfer timing (during communication at same potential)**

- Remarks**
1.  $R_b[\Omega]$ : Communication line (SDAr) pull-up resistance,  $C_b[F]$ : Communication line (SDAr, SCLr) load capacitance
  2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14),  
h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)
  3.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),  
n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

**Simplified I<sup>2</sup>C mode connection diagram (during communication at different potential)****Simplified I<sup>2</sup>C mode serial transfer timing (during communication at different potential)**

- Remarks**
1.  $R_b[\Omega]$ : Communication line (SDAr, SCLr) pull-up resistance,  $C_b[F]$ : Communication line (SDAr, SCLr) load capacitance,  $V_b[V]$ : Communication line voltage
  2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)
  3.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

## 2.6.4 LVD circuit characteristics

**LVD Detection Voltage of Reset Mode and Interrupt Mode**(T<sub>A</sub> = -40 to +85°C, V<sub>PDR</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V <sub>LVD0</sub>	Power supply rise time	3.98	4.06	4.14	V
			Power supply fall time	3.90	3.98	4.06	V
		V <sub>LVD1</sub>	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V <sub>LVD2</sub>	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V <sub>LVD3</sub>	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V <sub>LVD4</sub>	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V <sub>LVD5</sub>	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V <sub>LVD6</sub>	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V <sub>LVD7</sub>	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V <sub>LVD8</sub>	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		V <sub>LVD9</sub>	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		V <sub>LVD10</sub>	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		V <sub>LVD11</sub>	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		V <sub>LVD12</sub>	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		V <sub>LVD13</sub>	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width		t <sub>LW</sub>		300			μs
Detection delay time						300	μs

**Remark** The electrical characteristics of the products G: Industrial applications ( $T_A = -40$  to  $+105^\circ\text{C}$ ) are different from those of the products “A: Consumer applications, and D: Industrial applications”. For details, refer to 3.1 to 3.10.

### 3.1 Absolute Maximum Ratings

#### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ ) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	$V_{DD}$		$-0.5$ to $+6.5$	V
	$EV_{DD0}, EV_{DD1}$	$EV_{DD0} = EV_{DD1}$	$-0.5$ to $+6.5$	V
	$EV_{SS0}, EV_{SS1}$	$EV_{SS0} = EV_{SS1}$	$-0.5$ to $+0.3$	V
REGC pin input voltage	$V_{IREGC}$	REGC	$-0.3$ to $+2.8$ and $-0.3$ to $V_{DD} + 0.3$ <sup>Note 1</sup>	V
Input voltage	$V_{I1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	$-0.3$ to $EV_{DD0} + 0.3$ and $-0.3$ to $V_{DD} + 0.3$ <sup>Note 2</sup>	V
	$V_{I2}$	P60 to P63 (N-ch open-drain)	$-0.3$ to $+6.5$	V
	$V_{I3}$	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, RESET	$-0.3$ to $V_{DD} + 0.3$ <sup>Note 2</sup>	V
Output voltage	$V_{O1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	$-0.3$ to $EV_{DD0} + 0.3$ and $-0.3$ to $V_{DD} + 0.3$ <sup>Note 2</sup>	V
	$V_{O2}$	P20 to P27, P150 to P156	$-0.3$ to $V_{DD} + 0.3$ <sup>Note 2</sup>	V
Analog input voltage	$V_{AI1}$	ANI16 to ANI26	$-0.3$ to $EV_{DD0} + 0.3$ and $-0.3$ to $AV_{REF(+)} + 0.3$ <sup>Notes 2, 3</sup>	V
	$V_{AI2}$	ANI0 to ANI14	$-0.3$ to $V_{DD} + 0.3$ and $-0.3$ to $AV_{REF(+)} + 0.3$ <sup>Notes 2, 3</sup>	V

**Notes 1.** Connect the REGC pin to  $V_{SS}$  via a capacitor (0.47 to 1  $\mu\text{F}$ ). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**2.** Must be 6.5 V or lower.

**3.** Do not exceed  $AV_{REF(+)} + 0.3$  V in case of A/D conversion target pin.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**2.**  $AV_{REF(+)}$  : + side reference voltage of the A/D converter.

**3.**  $V_{SS}$  : Reference voltage

## 3.3 DC Characteristics

## 3.3.1 Pin characteristics

(T<sub>A</sub> =  $-40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ ) (1/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high <sup>Note 1</sup>	I <sub>OH1</sub>	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		-3.0 <sup>Note 2</sup>	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty $\leq 70\%$ <sup>Note 3</sup> )	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		-30.0	mA
			$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$		-10.0	mA
			$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 2.7\text{ V}$		-5.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty $\leq 70\%$ <sup>Note 3</sup> )	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		-30.0	mA
			$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$		-19.0	mA
			$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 2.7\text{ V}$		-10.0	mA
		Total of all pins (When duty $\leq 70\%$ <sup>Note 3</sup> )	$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		-60.0	mA
	I <sub>OH2</sub>	Per pin for P20 to P27, P150 to P156	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$		-0.1 <sup>Note 2</sup>	mA
		Total of all pins (When duty $\leq 70\%$ <sup>Note 3</sup> )	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$		-1.5	mA

**Notes** 1. Value of current at which the device operation is guaranteed even if the current flows from the EV<sub>DD0</sub>, EV<sub>DD1</sub>, V<sub>DD</sub> pins to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor  $\leq 70\%$ .

The output current value that has changed to the duty factor  $> 70\%$  the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins =  $(I_{\text{OH}} \times 0.7)/(n \times 0.01)$

<Example> Where  $n = 80\%$  and  $I_{\text{OH}} = -10.0\text{ mA}$

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

**Caution** P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

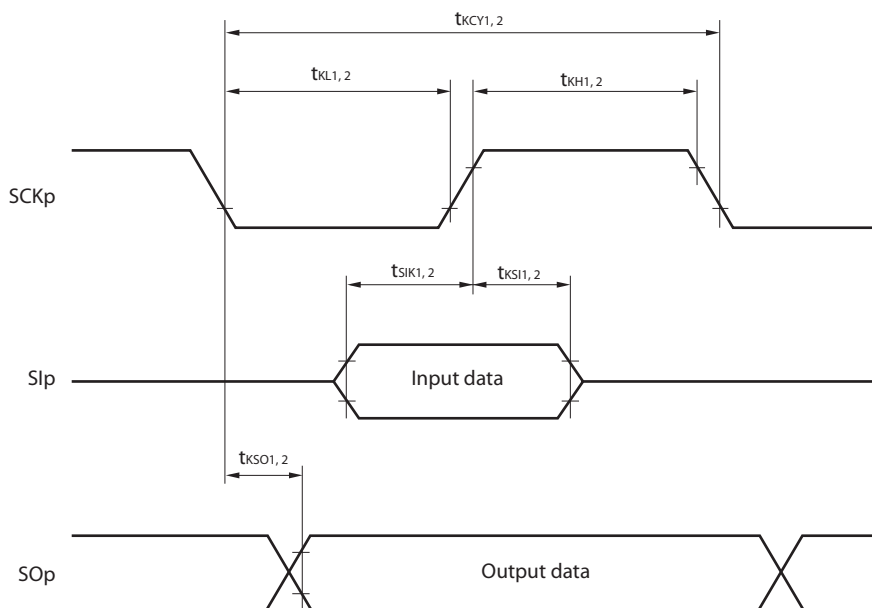
**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ ) (4/5)**

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	$\text{V}_{\text{OH1}}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH1}} = -3.0\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.7$		V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH1}} = -2.0\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.6$		V
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH1}} = -1.5\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.5$		V
	$\text{V}_{\text{OH2}}$	P20 to P27, P150 to P156	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH2}} = -100\text{ }\mu\text{A}$	$\text{V}_{\text{DD}} - 0.5$		V
Output voltage, low	$\text{V}_{\text{OL1}}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 8.5\text{ mA}$		0.7	V
			$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 3.0\text{ mA}$		0.6	V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 1.5\text{ mA}$		0.4	V
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 0.6\text{ mA}$		0.4	V
	$\text{V}_{\text{OL2}}$	P20 to P27, P150 to P156	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL2}} = 400\text{ }\mu\text{A}$		0.4	V
	$\text{V}_{\text{OL3}}$	P60 to P63	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 15.0\text{ mA}$		2.0	V
			$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 5.0\text{ mA}$		0.4	V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 3.0\text{ mA}$		0.4	V
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 2.0\text{ mA}$		0.4	V

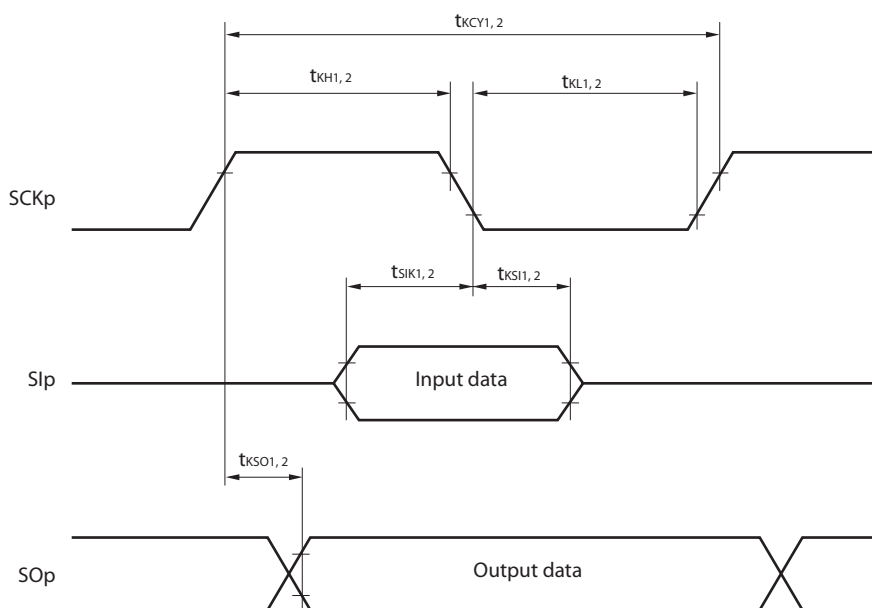
**Caution** P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

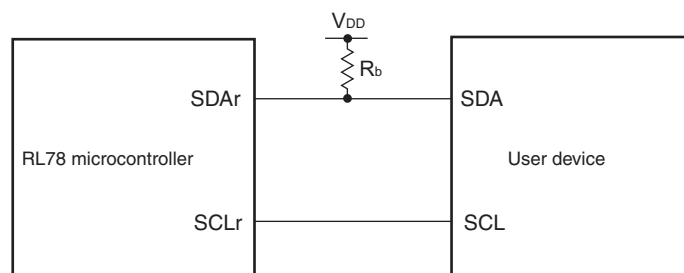
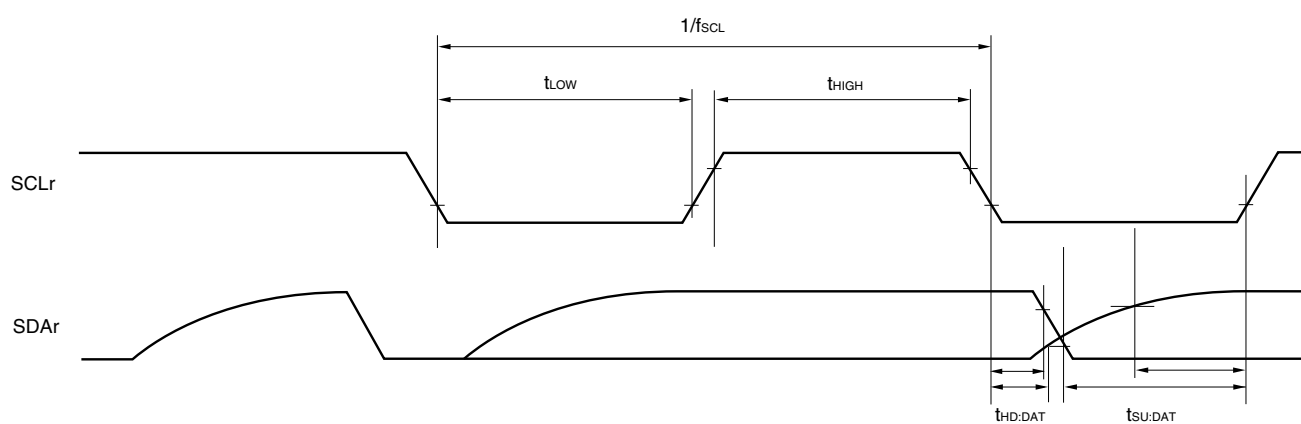
**CSI mode serial transfer timing (during communication at same potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (during communication at same potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



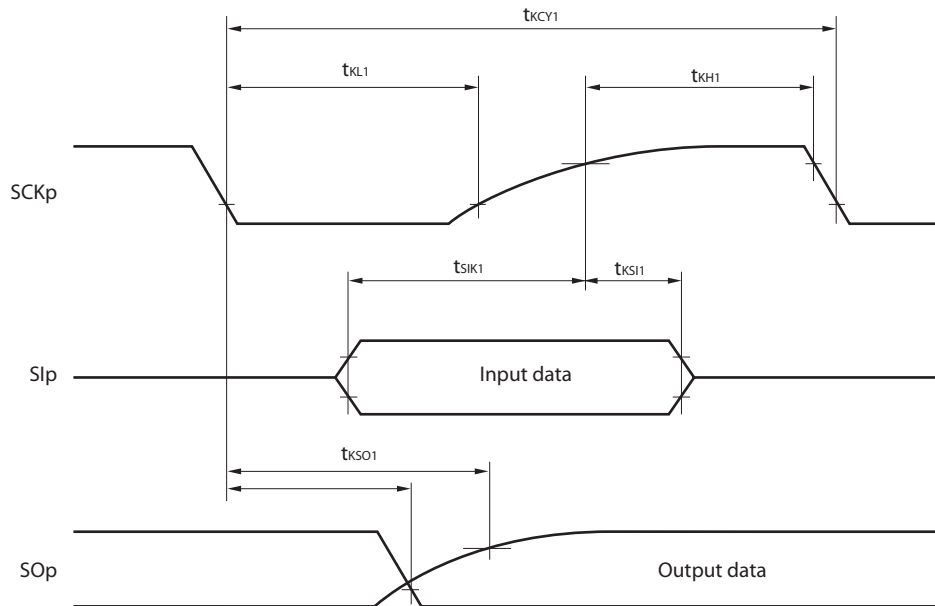
- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
  2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

**Simplified I<sup>2</sup>C mode connection diagram (during communication at same potential)****Simplified I<sup>2</sup>C mode serial transfer timing (during communication at same potential)**

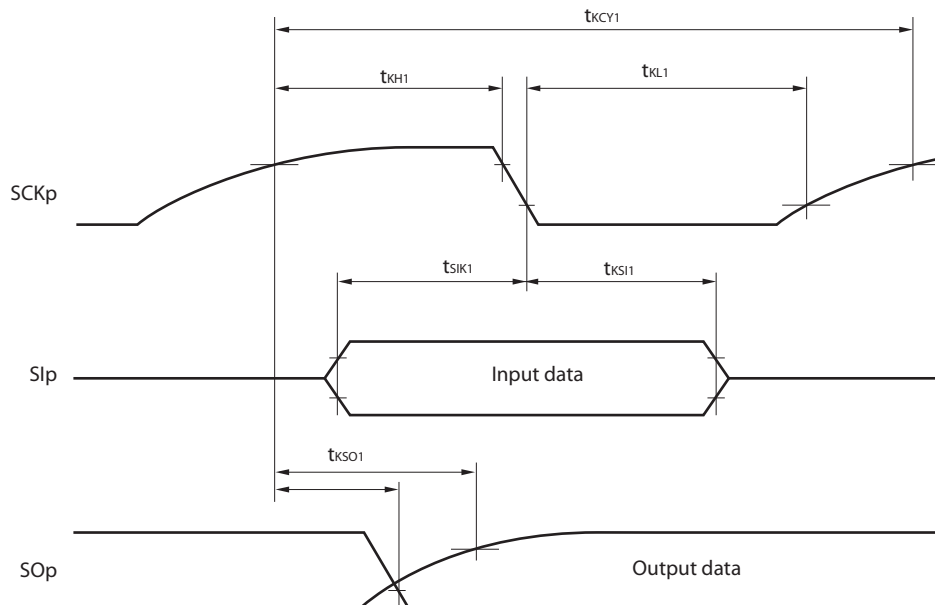
- Remarks**
- $R_b[\Omega]$ : Communication line (SDAr) pull-up resistance,  $C_b[F]$ : Communication line (SDAr, SCLr) load capacitance
  - r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14),  
h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)
  - $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)



**CSI mode serial transfer timing (master mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (master mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



- Remarks**
1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 00, 01, 02, 10, 12, 13), n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
  2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

## 3.5.2 Serial interface IICA

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f <sub>SCL</sub>	Fast mode: f <sub>CLK</sub> ≥ 3.5 MHz	–	–	0	400	kHz
		Standard mode: f <sub>CLK</sub> ≥ 1 MHz	0	100	–	–	kHz
Setup time of restart condition	t <sub>SU:STA</sub>		4.7		0.6		μs
Hold time <sup>Note 1</sup>	t <sub>HD:STA</sub>		4.0		0.6		μs
Hold time when SCLA0 = “L”	t <sub>LOW</sub>		4.7		1.3		μs
Hold time when SCLA0 = “H”	t <sub>HIGH</sub>		4.0		0.6		μs
Data setup time (reception)	t <sub>SU:DAT</sub>		250		100		ns
Data hold time (transmission) <sup>Note 2</sup>	t <sub>HD:DAT</sub>		0	3.45	0	0.9	μs
Setup time of stop condition	t <sub>SU:STO</sub>		4.0		0.6		μs
Bus-free time	t <sub>BUF</sub>		4.7		1.3		μs

**Notes** 1. The first clock pulse is generated after this period when the start/restart condition is detected.

<R> 2. The maximum value (MAX.) of tHD:DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

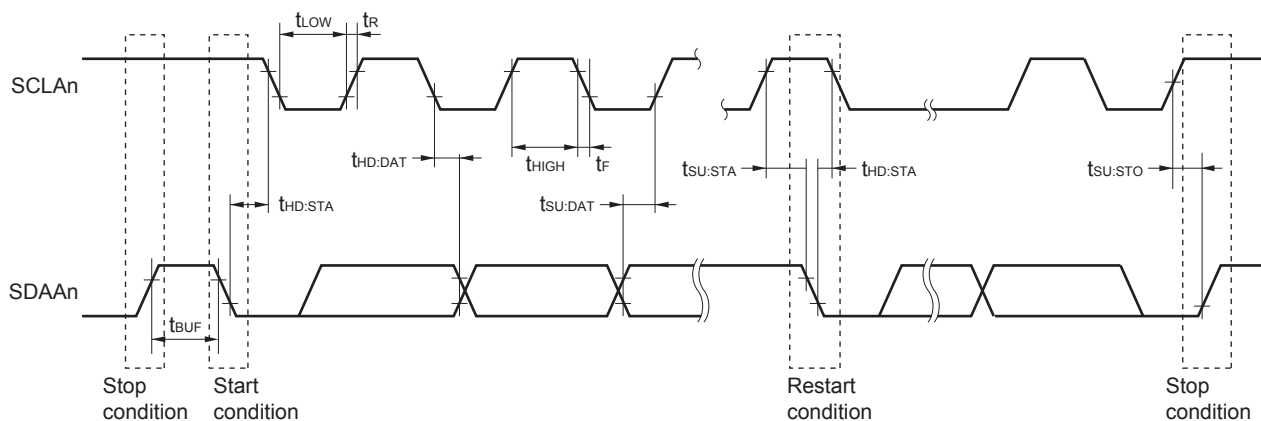
**Caution** The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: Cb = 400 pF, Rb = 2.7 kΩ

Fast mode: Cb = 320 pF, Rb = 1.1 kΩ

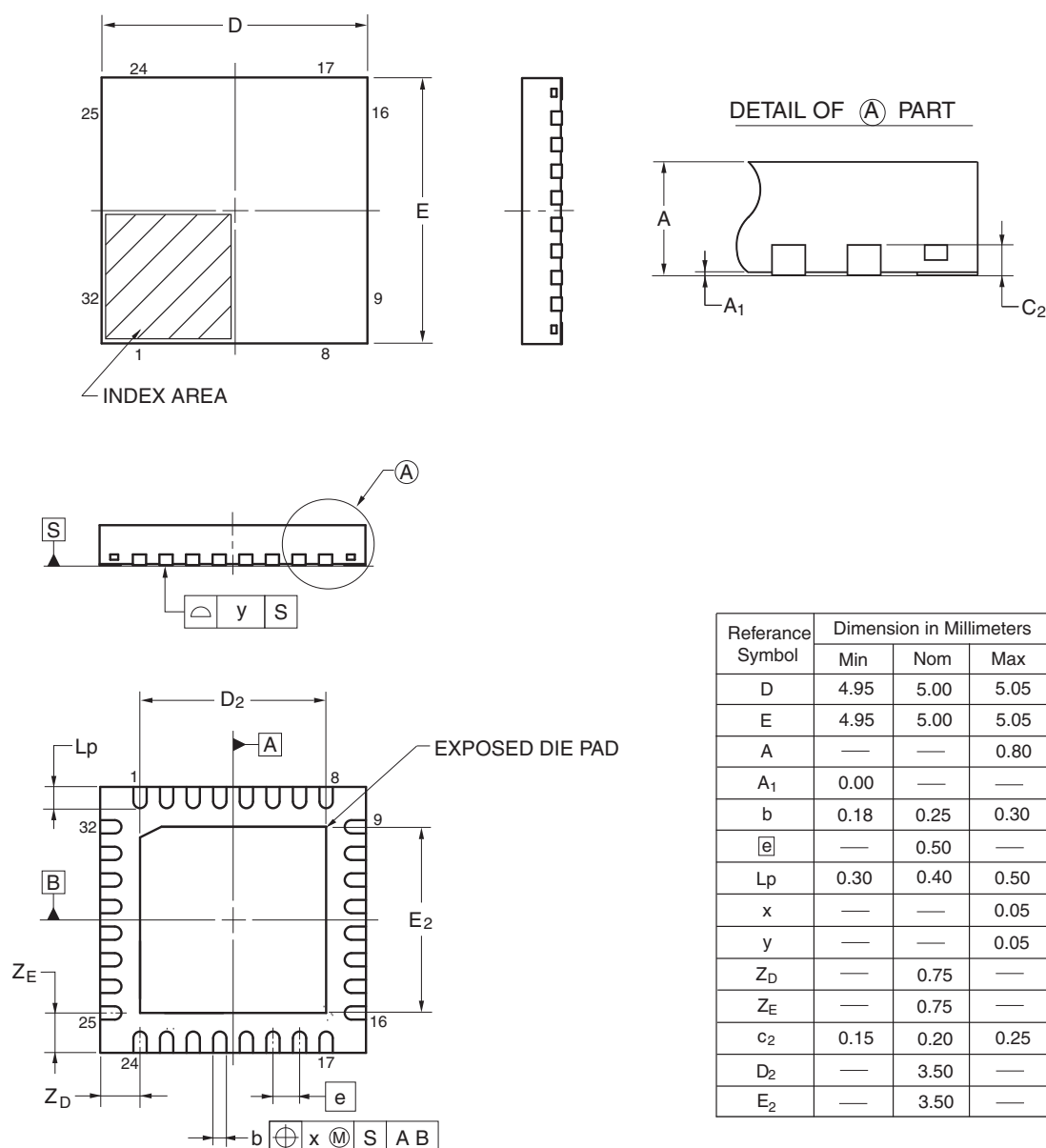
IICA serial transfer timing

**Remark** n = 0, 1

## 4.5 32-pin Products

R5F100BAANA, R5F100BCANA, R5F100BDANA, R5F100BEANA, R5F100BFANA, R5F100BGANA  
 R5F101BAANA, R5F101BCANA, R5F101BDANA, R5F101BEANA, R5F101BFANA, R5F101BGANA  
 R5F100BADNA, R5F100BCDNA, R5F100BDDNA, R5F100BEDNA, R5F100BFDNA, R5F100BGDNA  
 R5F101BADNA, R5F101BCDNA, R5F101BDDNA, R5F101BEDNA, R5F101BFDNA, R5F101BGDNA  
 R5F100BAGNA, R5F100BCGNA, R5F100BDGNA, R5F100BEGNA, R5F100BFGNA, R5F100BGGNA

JEITA Package code	RENESAS code	Previous code	MASS (TYP.)[g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-5	0.06

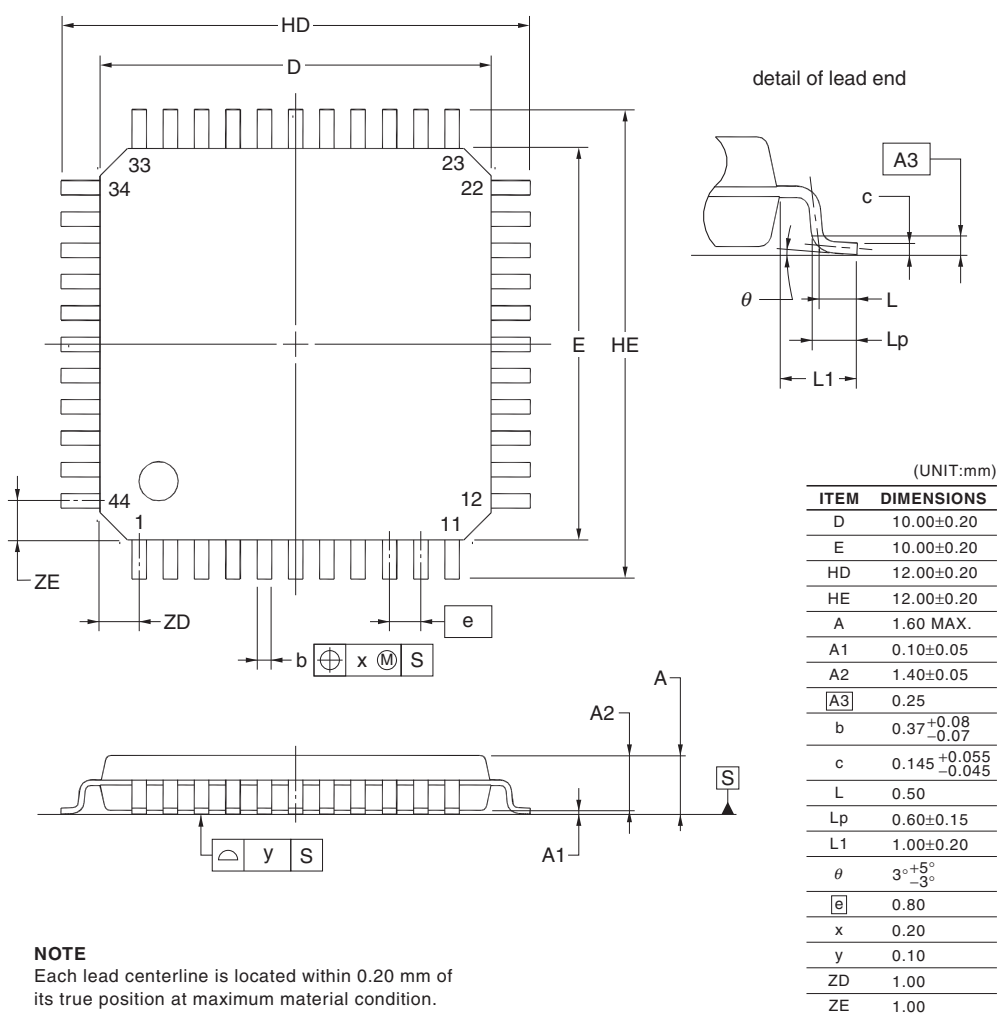


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## 4.8 44-pin Products

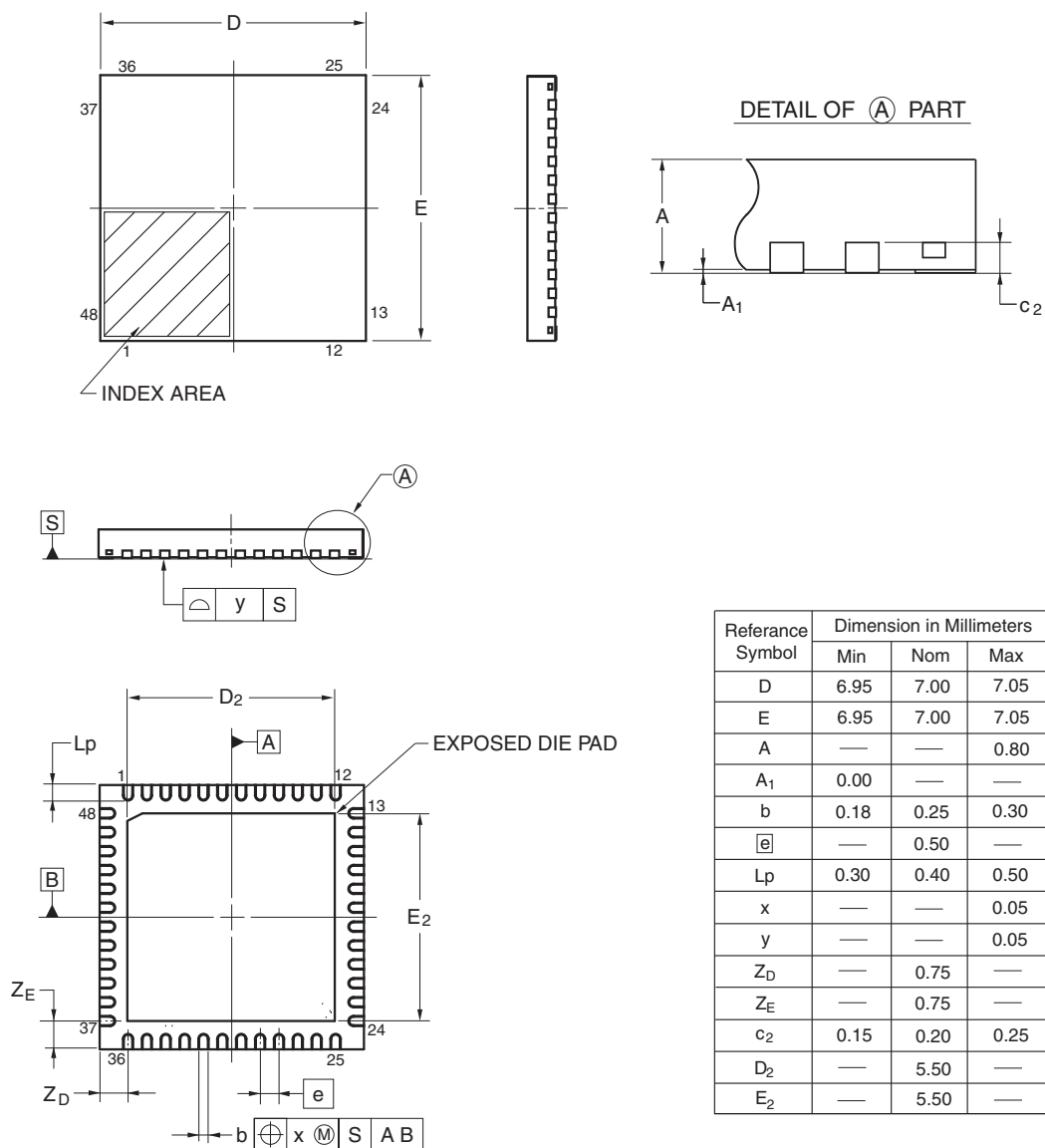
R5F100FAAFP, R5F100FCAFP, R5F100FDAFP, R5F100FEAFP, R5F100FFAFP, R5F100FGAFP,  
 R5F100FHAFP, R5F100FJAFP, R5F100FKAFP, R5F100FLAFP  
 R5F101FAAFP, R5F101FCAFP, R5F101FDAFP, R5F101FEAFP, R5F101FFAFP, R5F101FGAFP,  
 R5F101FHAFP, R5F101FJAFP, R5F101FKAFP, R5F101FLAFP  
 R5F100FADFP, R5F100FCDFP, R5F100FDDFP, R5F100FEDFP, R5F100FFDFP, R5F100FGDFP,  
 R5F100FHDFP, R5F100FJDFP, R5F100FKDFP, R5F100FLDFP  
 R5F101FADFP, R5F101FCDFP, R5F101FDDFP, R5F101FEDFP, R5F101FFDFP, R5F101FGDFP,  
 R5F101FHDFP, R5F101FJDFP, R5F101FKDFP, R5F101FLDFP  
 R5F100FAGFP, R5F100FCGFP, R5F100FDGFP, R5F100FEGFP, R5F100FFGFP, R5F100FGGFP,  
 R5F100FHGFP, R5F100FJGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP44-10x10-0.80	PLQP0044GC-A	P44GB-80-UES-2	0.36



R5F100GAANA, R5F100GCANA, R5F100GDANA, R5F100GEANA, R5F100GFANA, R5F100GGANA,  
 R5F100GHANA, R5F100GJANA, R5F100GKANA, R5F100GLANA  
 R5F101GAANA, R5F101GCANA, R5F101GDANA, R5F101GEANA, R5F101GFANA, R5F101GGANA,  
 R5F101GHANA, R5F101GJANA, R5F101GKANA, R5F101GLANA  
 R5F100GADNA, R5F100GCDNA, R5F100GDDNA, R5F100GEDNA, R5F100GFDNA, R5F100GGDNA,  
 R5F100GHDNA, R5F100GJDNA, R5F100GKDNA, R5F100GLDNA  
 R5F101GADNA, R5F101GCDNA, R5F101GDDNA, R5F101GEDNA, R5F101GFDNA, R5F101GGDNA,  
 R5F101GHDNA, R5F101GJDNA, R5F101GKDNA, R5F101GLDNA  
 R5F100GAGNA, R5F100GCGNA, R5F100GDGNA, R5F100GEGNA, R5F100GFGNA, R5F100GGGNA,  
 R5F100GHGNA, R5F100GJGNA

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-6	0.13



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