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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

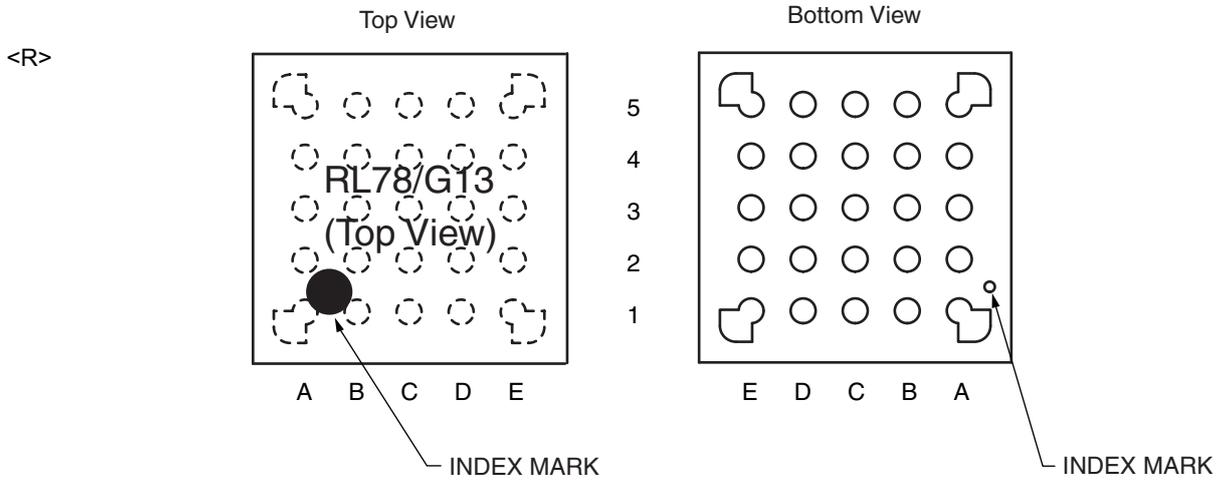
#### Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	30-LSSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100acgsp-v0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100acgsp-v0</a>



1.3.3 25-pin products

- 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch)



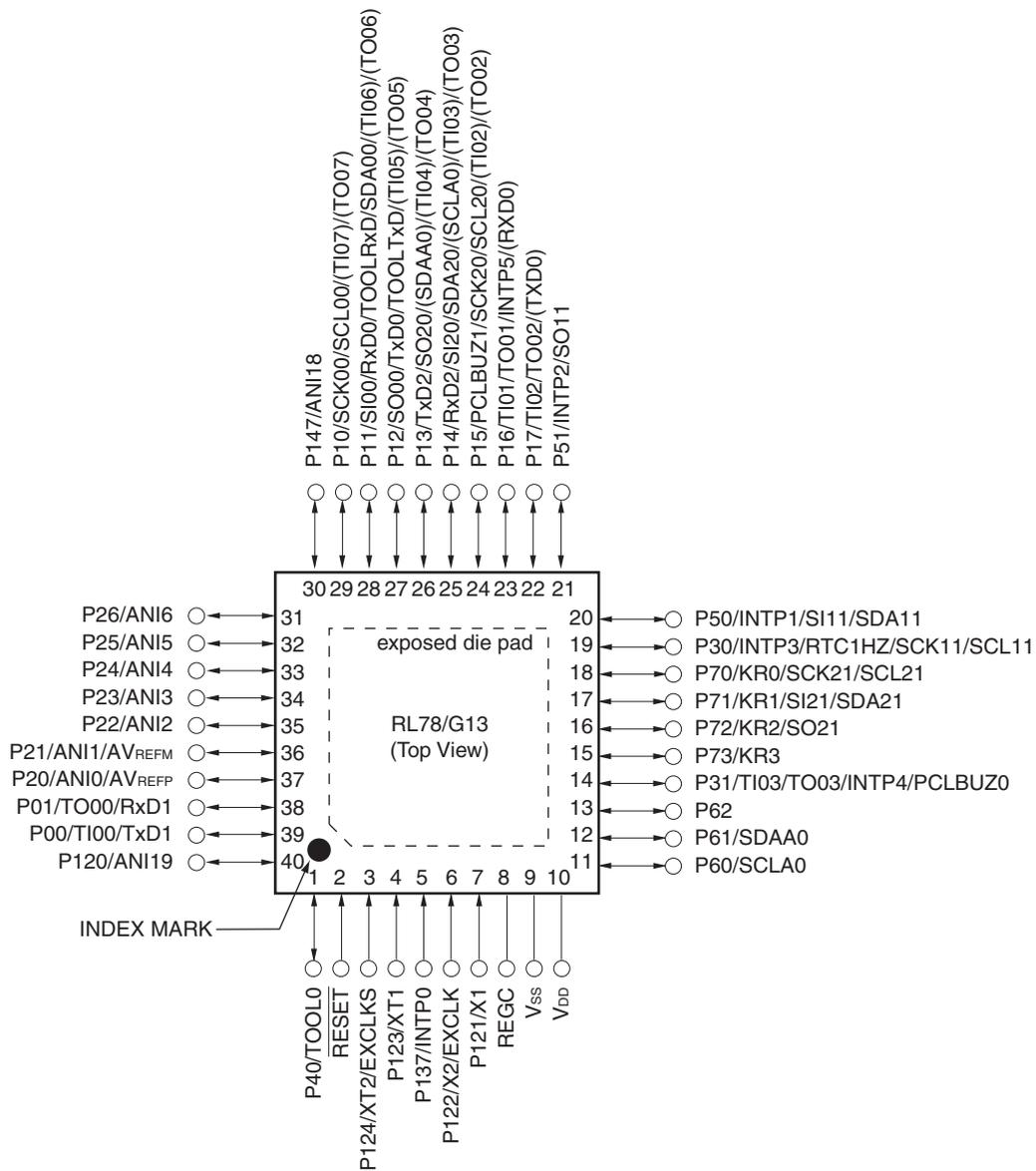
	A	B	C	D	E	
5	P40/TOOL0	RESET	P01/ANI16/ TO00/RxD1	P22/ANI2	P147/ANI18	5
4	P122/X2/ EXCLK	P137/INTP0	P00/ANI17/ TI00/TxD1	P21/ANI1/ AVREFM	P10/SCK00/ SCL00	4
3	P121/X1	V <sub>DD</sub>	P20/ANI0/ AVREFP	P12/SO00/ TxD0/ TOOLTxD	P11/SI00/ RxD0/ TOOLRxD/ SDA00	3
2	REGC	V <sub>SS</sub>	P30/INTP3/ SCK11/SCL11	P17/TI02/ TO02/SO11	P50/INTP1/ SI11/SDA11	2
1	P60/SCLA0	P61/SDAA0	P31/TI03/ TO03/INTP4/ PCLBUZ0	P16/TI01/ TO01/INTP5	P130	1
	A	B	C	D	E	

**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1 μF).

**Remark** For pin identification, see 1.4 Pin Identification.

1.3.7 40-pin products

- 40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)



**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1 μF).

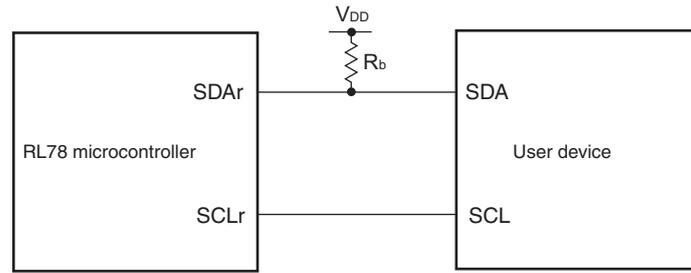
**Remarks 1.** For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.
- It is recommended to connect an exposed die pad to V<sub>SS</sub>.

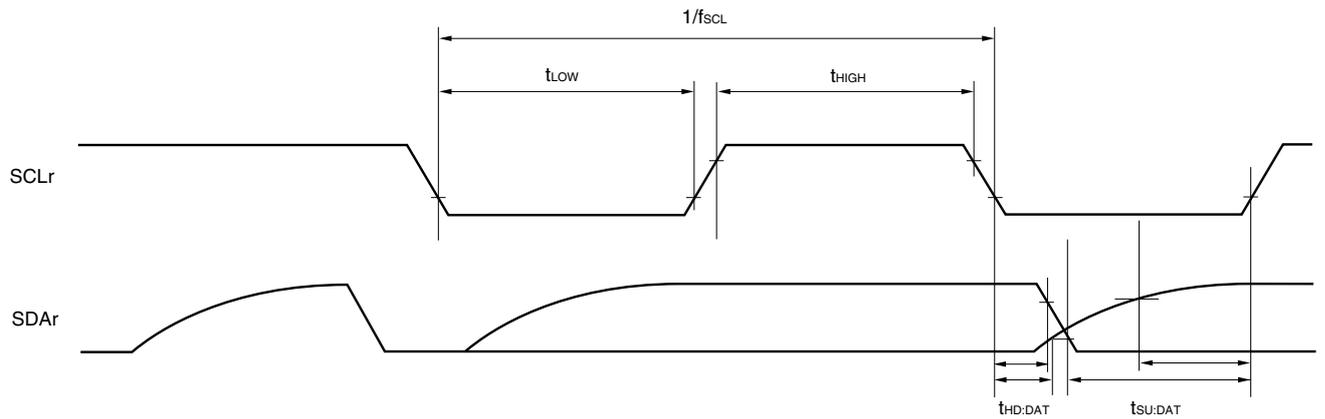
- Notes**
1. Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, or V<sub>SS</sub>, EV<sub>SS0</sub>, and EV<sub>SS1</sub>. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. When high-speed on-chip oscillator and subsystem clock are stopped.
  3. When high-speed system clock and subsystem clock are stopped.
  4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
    - HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 32\text{ MHz}$   
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 16\text{ MHz}$
    - LS (low-speed main) mode:  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 8\text{ MHz}$
    - LV (low-voltage main) mode:  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 4\text{ MHz}$

- Remarks**
1. f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2. f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
  3. f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

**Simplified I<sup>2</sup>C mode connection diagram (during communication at same potential)**



**Simplified I<sup>2</sup>C mode serial transfer timing (during communication at same potential)**



- Remarks**
1. R<sub>b</sub>[Ω]: Communication line (SDAr) pull-up resistance, C<sub>b</sub>[F]: Communication line (SDAr, SCLr) load capacitance
  2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14), h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)
  3. f<sub>MCK</sub>: Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),  
 n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

- The smaller maximum transfer rate derived by using  $f_{mck}/6$  or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when  $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$  and  $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.
- Use it with  $EV_{DD0} \geq V_b$ .
- The smaller maximum transfer rate derived by using  $f_{mck}/6$  or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when  $1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$  and  $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

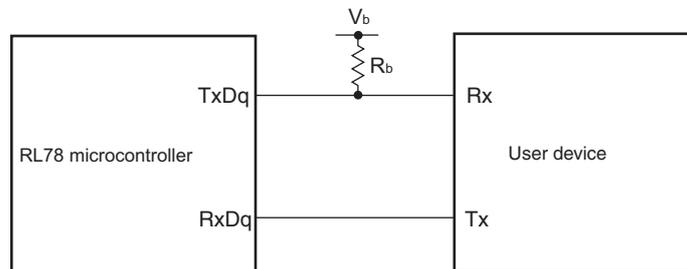
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 20- to 52-pin products)/EV<sub>DD</sub> tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)

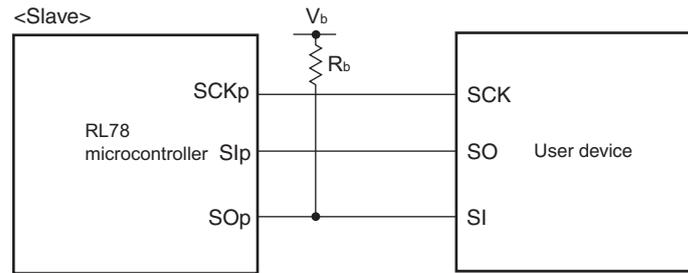


## (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (1/2)

(T<sub>A</sub> = -40 to +85°C, 2.7 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t <sub>KCY1</sub>	t <sub>KCY1</sub> ≥ 2/f <sub>CLK</sub> 4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 1.4 kΩ	200		1150		1150		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ	300		1150		1150		ns
SCKp high-level width	t <sub>KH1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 1.4 kΩ	t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ	t <sub>KCY1</sub> /2 – 120		t <sub>KCY1</sub> /2 – 120		t <sub>KCY1</sub> /2 – 120		ns
SCKp low-level width	t <sub>KL1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 1.4 kΩ	t <sub>KCY1</sub> /2 – 7		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ	t <sub>KCY1</sub> /2 – 10		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
Slp setup time (to SCKp↑) <sup>Note 1</sup>	t <sub>SIK1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 1.4 kΩ	58		479		479		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ	121		479		479		ns
Slp hold time (from SCKp↑) <sup>Note 1</sup>	t <sub>KSI1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 1.4 kΩ	10		10		10		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↓ to SOp output <sup>Note 1</sup>	t <sub>KSO1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 1.4 kΩ		60		60		60	ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ		130		130		130	ns

(Notes, Caution, and Remarks are listed on the next page.)

**CSI mode connection diagram (during communication at different potential)**

- Remarks**
- $R_b[\Omega]$ : Communication line (SO<sub>p</sub>) pull-up resistance,  $C_b[\text{F}]$ : Communication line (SO<sub>p</sub>) load capacitance,  $V_b[\text{V}]$ : Communication line voltage
  - p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
  - $f_{\text{MCK}}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKS<sub>mn</sub> bit of serial mode register mn (SMR<sub>mn</sub>).  
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))
  - CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.  
Use other CSI for communication at different potential.

**(3) I<sup>2</sup>C fast mode plus**

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f <sub>SCL</sub>	Fast mode plus: f <sub>CLK</sub> ≥ 10 MHz 2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	0	1000	—	—	—	—	kHz
Setup time of restart condition	t <sub>SU:STA</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	0.26		—	—	—	—	μs
Hold time <sup>Note 1</sup>	t <sub>HD:STA</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	0.26		—	—	—	—	μs
Hold time when SCLA0 = "L"	t <sub>LOW</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	0.5		—	—	—	—	μs
Hold time when SCLA0 = "H"	t <sub>HIGH</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	0.26		—	—	—	—	μs
Data setup time (reception)	t <sub>SU:DAT</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	50		—	—	—	—	μs
Data hold time (transmission) <sup>Note 2</sup>	t <sub>HD:DAT</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	0	0.45	—	—	—	—	μs
Setup time of stop condition	t <sub>SU:STO</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	0.26		—	—	—	—	μs
Bus-free time	t <sub>BUF</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	0.5		—	—	—	—	μs

**Notes** 1. The first clock pulse is generated after this period when the start/restart condition is detected.

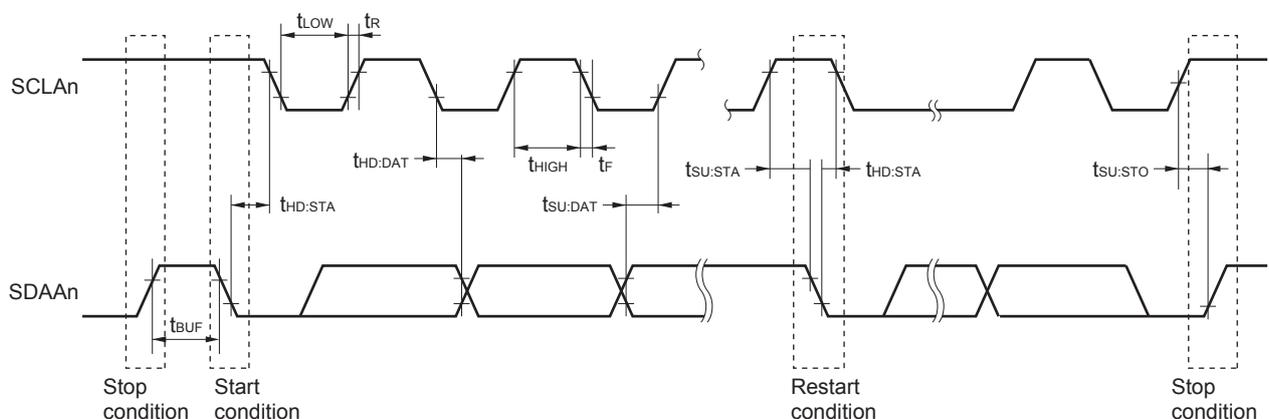
<R> 2. The maximum value (MAX.) of t<sub>HD:DAT</sub> is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution** The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I<sub>OH1</sub>, I<sub>OL1</sub>, V<sub>OH1</sub>, V<sub>OL1</sub>) must satisfy the values in the redirect destination.

**Remark** The maximum value of C<sub>b</sub> (communication line capacitance) and the value of R<sub>b</sub> (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: C<sub>b</sub> = 120 pF, R<sub>b</sub> = 1.1 kΩ

**IICA serial transfer timing**



**Remark** n = 0, 1

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AV<sub>REFM</sub>/ANI1 (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26

(T<sub>A</sub> = -40 to +85°C, 2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub>, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V, Reference voltage (+) = V<sub>BGR</sub><sup>Note 3</sup>, Reference voltage (-) = AV<sub>REFM</sub> = 0 V<sup>Note 4</sup>, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t <sub>CONV</sub>	8-bit resolution	2.4 V ≤ V <sub>DD</sub> ≤ 5.5 V	17		39	μs
Zero-scale error <sup>Notes 1, 2</sup>	E <sub>ZS</sub>	8-bit resolution	2.4 V ≤ V <sub>DD</sub> ≤ 5.5 V			±0.60	%FSR
Integral linearity error <sup>Note 1</sup>	ILE	8-bit resolution	2.4 V ≤ V <sub>DD</sub> ≤ 5.5 V			±2.0	LSB
Differential linearity error <sup>Note 1</sup>	DLE	8-bit resolution	2.4 V ≤ V <sub>DD</sub> ≤ 5.5 V			±1.0	LSB
Analog input voltage	V <sub>AIN</sub>			0		V <sub>BGR</sub> <sup>Note 3</sup>	V

**Notes** 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (-) = V<sub>SS</sub>, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AV<sub>REFM</sub>.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AV<sub>REFM</sub>.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AV<sub>REFM</sub>.

## 2.8 Flash Memory Programming Characteristics

(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f <sub>CLK</sub>	1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V	1		32	MHz
Number of code flash rewrites <small>Notes 1, 2, 3</small>	C <sub>enwr</sub>	Retained for 20 years T <sub>A</sub> = 85°C	1,000			Times
Number of data flash rewrites <small>Notes 1, 2, 3</small>		Retained for 1 years T <sub>A</sub> = 25°C		1,000,000		
		Retained for 5 years T <sub>A</sub> = 85°C	100,000			
		Retained for 20 years T <sub>A</sub> = 85°C	10,000			

**Notes** 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library
3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 2.9 Dedicated Flash Memory Programmer Communication (UART)

(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

- Notes**
1. Total current flowing into  $V_{DD}$  and  $EV_{DD0}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$  or  $V_{SS}$ ,  $EV_{SS0}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. During HALT instruction execution by flash memory.
  3. When high-speed on-chip oscillator and subsystem clock are stopped.
  4. When high-speed system clock and subsystem clock are stopped.
  5. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $RTCLPC = 1$  and setting ultra-low current consumption ( $AMPHS1 = 1$ ). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.  
HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$   
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
  8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^\circ\text{C}$

5. The smaller maximum transfer rate derived by using  $f_{MCK}/12$  or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when  $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$  and  $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

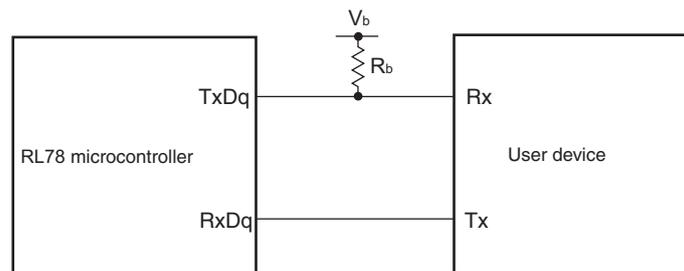
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

6. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 5 above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output ( $V_{DD}$  tolerance (for the 20- to 52-pin products)/ $EV_{DD}$  tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.

**UART mode connection diagram (during communication at different potential)**



**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )**

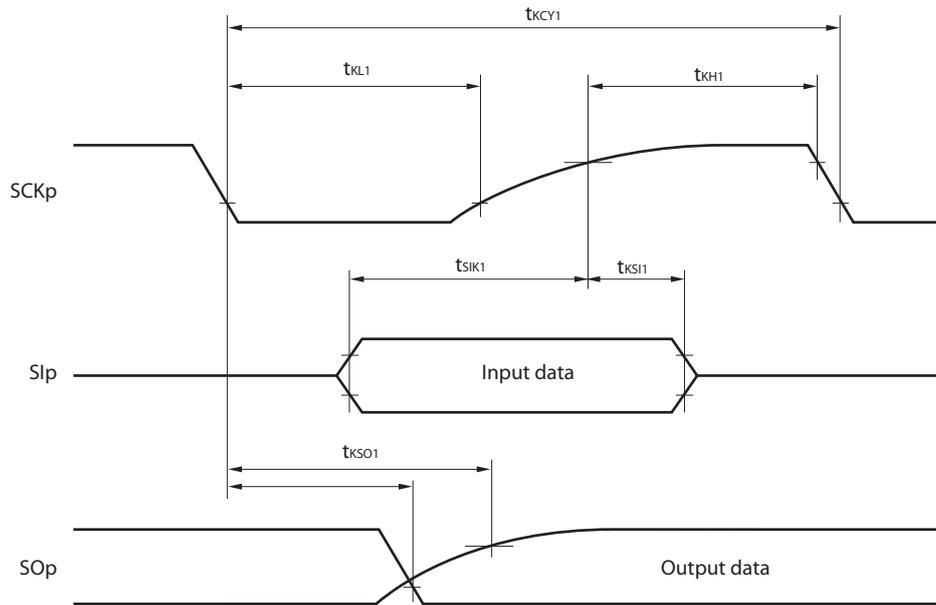
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp↓) <sup>Note</sup>	$t_{\text{SIK1}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$	88		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	88		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$	220		ns
Slp hold time (from SCKp↓) <sup>Note</sup>	$t_{\text{KS1}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$	38		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	38		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$	38		ns
Delay time from SCKp↑ to SOp output <sup>Note</sup>	$t_{\text{KS01}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$		50	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$		50	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$		50	ns

**Note** When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .

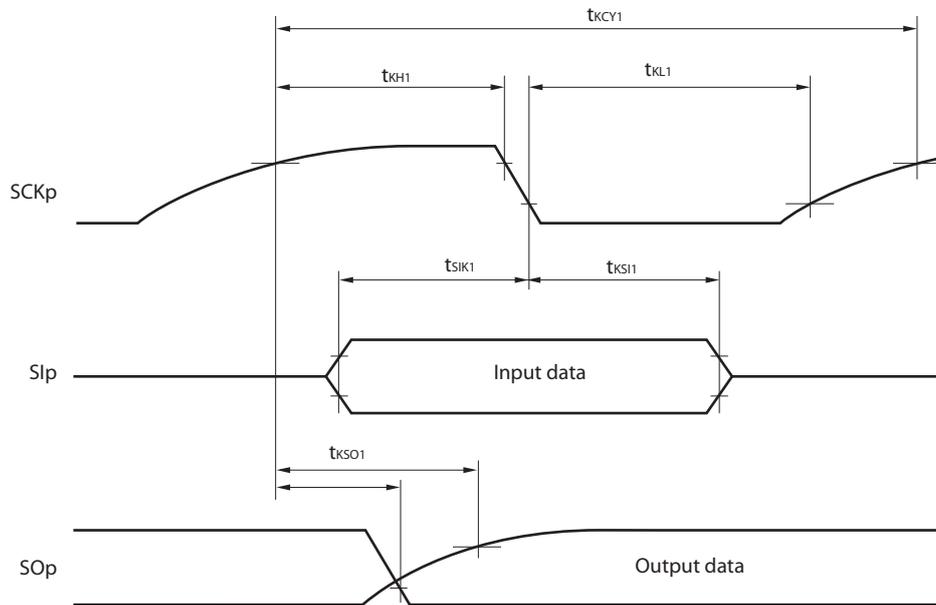
**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output ( $\text{V}_{\text{DD}}$  tolerance (for the 20- to 52-pin products)/ $\text{EV}_{\text{DD}}$  tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $\text{V}_{\text{IH}}$  and  $\text{V}_{\text{IL}}$ , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

**CSI mode serial transfer timing (master mode) (during communication at different potential)  
(When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ .)**



**CSI mode serial transfer timing (master mode) (during communication at different potential)  
(When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .)**



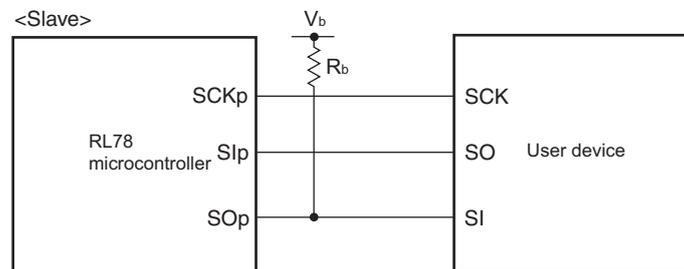
- Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 00, 01, 02, 10, 12, 13), n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
- 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**Notes** 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

2. When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ . The  $\text{Slp}$  setup time becomes “to  $\text{SCKp}\downarrow$ ” when  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .
3. When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ . The  $\text{Slp}$  hold time becomes “from  $\text{SCKp}\downarrow$ ” when  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .
4. When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ . The delay time to  $\text{SOp}$  output becomes “from  $\text{SCKp}\uparrow$ ” when  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .

**Caution** Select the TTL input buffer for the  $\text{Slp}$  pin and  $\text{SCKp}$  pin and the N-ch open drain output ( $V_{DD}$  tolerance (for the 20- to 52-pin products)/ $\text{EV}_{DD}$  tolerance (for the 64- to 128-pin products)) mode for the  $\text{SOp}$  pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.

**CSI mode connection diagram (during communication at different potential)**



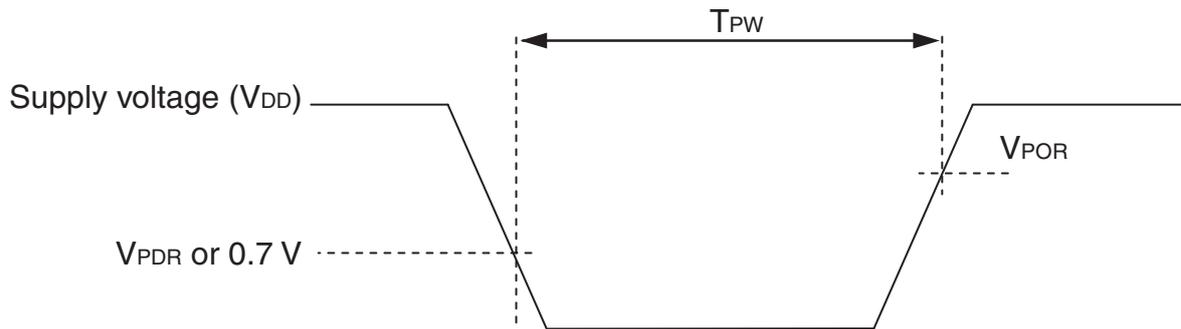
- Remarks** 1.  $R_b[\Omega]$ : Communication line ( $\text{SOp}$ ) pull-up resistance,  $C_b[\text{F}]$ : Communication line ( $\text{SOp}$ ) load capacitance,  $V_b[\text{V}]$ : Communication line voltage
2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
  3.  $f_{\text{MCK}}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the  $\text{CKSmn}$  bit of serial mode register mn (SMRmn).  
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))
  4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

3.6.3 POR circuit characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0$  V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	$V_{POR}$	Power supply rise time	1.45	1.51	1.57	V
	$V_{PDR}$	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width	$T_{PW}$		300			$\mu\text{s}$

**Note** Minimum time required for a POR reset when  $V_{DD}$  exceeds below  $V_{PDR}$ . This is also the minimum time required for a POR reset from when  $V_{DD}$  exceeds below 0.7 V to when  $V_{DD}$  exceeds  $V_{POR}$  while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



### 3.6.5 Power supply voltage rising slope characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0$  V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S <sub>VDD</sub>				54	V/ms

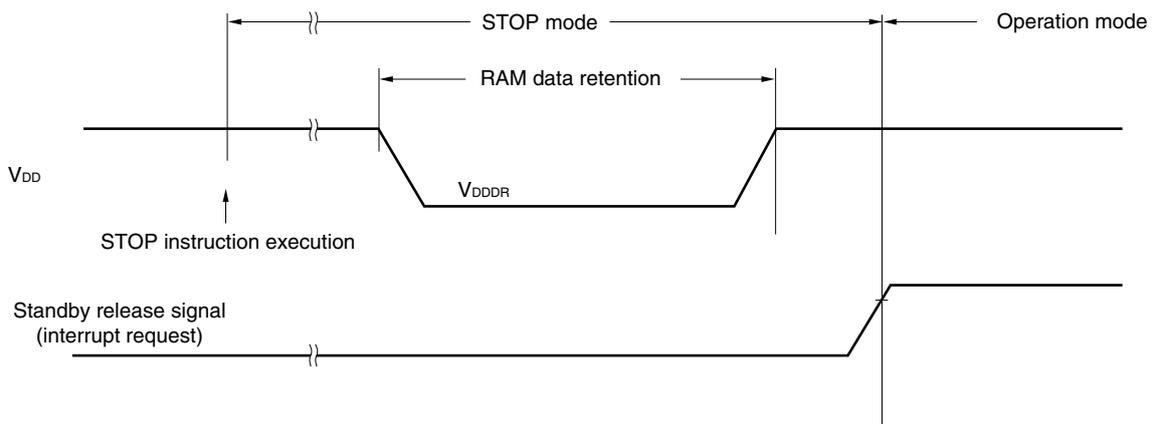
**Caution** Make sure to keep the internal reset state by the LVD circuit or an external reset until  $V_{DD}$  reaches the operating voltage range shown in 3.4 AC Characteristics.

### 3.7 RAM Data Retention Characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0$  V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V <sub>DDDR</sub>		1.44 <sup>Note</sup>		5.5	V

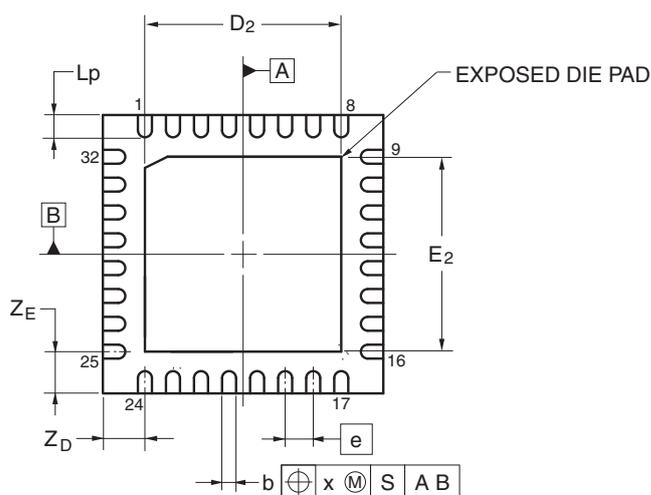
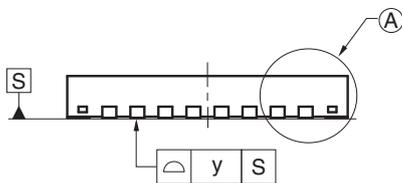
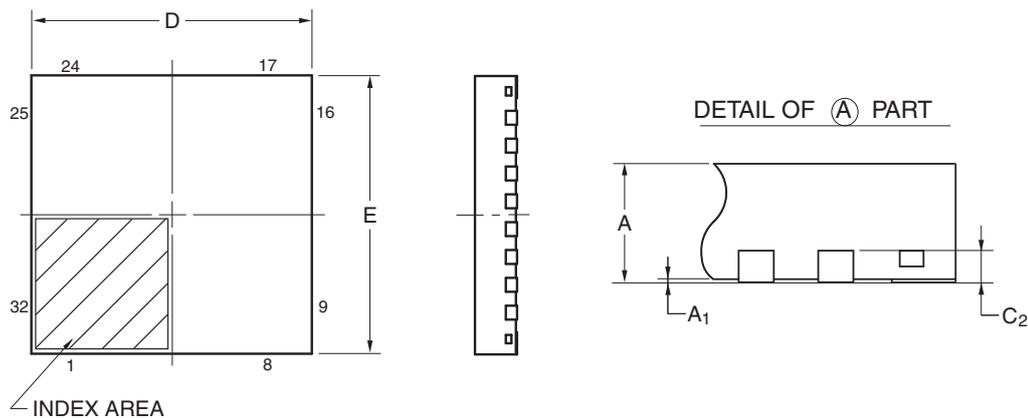
**Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



4.5 32-pin Products

R5F100BAANA, R5F100BCANA, R5F100BDANA, R5F100BEANA, R5F100BFANA, R5F100BGANA  
 R5F101BAANA, R5F101BCANA, R5F101BDANA, R5F101BEANA, R5F101BFANA, R5F101BGANA  
 R5F100BADNA, R5F100BCDNA, R5F100BDDNA, R5F100BEDNA, R5F100BFDNA, R5F100BGDNA  
 R5F101BADNA, R5F101BCDNA, R5F101BDDNA, R5F101BEDNA, R5F101BFDNA, R5F101BGDNA  
 R5F100BAGNA, R5F100BCGNA, R5F100BDGNA, R5F100BEGNA, R5F100BFGNA, R5F100BGGNA

JEITA Package code	RENESAS code	Previous code	MASS (TYP.)[g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-5	0.06



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.95	5.00	5.05
E	4.95	5.00	5.05
A	—	—	0.80
A <sub>1</sub>	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
L <sub>p</sub>	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z <sub>D</sub>	—	0.75	—
Z <sub>E</sub>	—	0.75	—
c <sub>2</sub>	0.15	0.20	0.25
D <sub>2</sub>	—	3.50	—
E <sub>2</sub>	—	3.50	—

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