



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	30-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100afgsp-v0

Table 1-1. List of Ordering Part Numbers

(2/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
25 pins	25-pin plastic WFLGA (3 × 3 mm, 0.5 mm pitch)	Mounted	A G	R5F1008AALA#U0, R5F1008CALA#U0, R5F1008DALA#U0, R5F1008EALA#U0 R5F1008AALA#W0, R5F1008CALA#W0, R5F1008DALA#W0, R5F1008EALA#W0 R5F1008AGLA#U0, R5F1008CGLA#U0, R5F1008DGLA#U0, R5F1008EGLA#U0 R5F1008AGLA#W0, R5F1008CGLA#W0, R5F1008DGLA#W0, R5F1008EGLA#W0
		Not mounted	A	R5F1018AALA#U0, R5F1018CALA#U0, R5F1018DALA#U0, R5F1018EALA#U0 R5F1018AALA#W0, R5F1018CALA#W0, R5F1018DALA#W0, R5F1018EALA#W0
30 pins	30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	Mounted	A D G	R5F100AAASP#V0, R5F100ACASP#V0, R5F100ADASP#V0, R5F100AEASP#V0, R5F100AFASP#V0, R5F100AGASP#V0 R5F100AAASP#X0, R5F100ACASP#X0, R5F100ADASP#X0, R5F100AEASP#X0, R5F100AFASP#X0, R5F100AGASP#X0 R5F100AADSP#V0, R5F100ACDSP#V0, R5F100ADDSP#V0, R5F100AEDSP#V0, R5F100AFDSP#V0, R5F100AGDSP#V0 R5F100AADSP#X0, R5F100ACDSP#X0, R5F100ADDSP#X0, R5F100AEDSP#X0, R5F100AFDSP#X0, R5F100AGDSP#X0 R5F100AAGSP#V0, R5F100ACGSP#V0, R5F100ADGSP#V0, R5F100AEGSP#V0, R5F100AFGSP#V0, R5F100AGGSP#V0 R5F100AAGSP#X0, R5F100ACGSP#X0, R5F100ADGSP#X0, R5F100AEGSP#X0, R5F100AFGSP#X0, R5F100AGGSP#X0
		Not mounted	A D	R5F101AAASP#V0, R5F101ACASP#V0, R5F101ADASP#V0, R5F101AEASP#V0, R5F101AFASP#V0, R5F101AGASP#V0 R5F101AAASP#X0, R5F101ACASP#X0, R5F101ADASP#X0, R5F101AEASP#X0, R5F101AFASP#X0, R5F101AGASP#X0 R5F101AADSP#V0, R5F101ACDSP#V0, R5F101ADDSP#V0, R5F101AEDSP#V0, R5F101AFDSP#V0, R5F101AGDSP#V0 R5F101AADSP#X0, R5F101ACDSP#X0, R5F101ADDSP#X0, R5F101AEDSP#X0, R5F101AFDSP#X0, R5F101AGDSP#X0
32 pins	32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)	Mounted	A D G	R5F100BAANA#U0, R5F100BCANA#U0, R5F100BDANA#U0, R5F100BEANA#U0, R5F100BFANA#U0, R5F100BGANA#U0 R5F100BAANA#W0, R5F100BCANA#W0, R5F100BDANA#W0, R5F100BEANA#W0, R5F100BFANA#W0, R5F100BGANA#W0 R5F100BADNA#U0, R5F100BCDNA#U0, R5F100BDDNA#U0, R5F100BEDNA#U0, R5F100BFDNA#U0, R5F100BGDNA#U0 R5F100BADNA#W0, R5F100BCDNA#W0, R5F100BDDNA#W0, R5F100BEDNA#W0, R5F100BFDNA#W0, R5F100BGDNA#W0 R5F100BAGNA#U0, R5F100BCGNA#U0, R5F100BDGNA#U0, R5F100BEGNA#U0, R5F100BFGNA#U0, R5F100BGGNA#U0 R5F100BAGNA#W0, R5F100BCGNA#W0, R5F100BDGNA#W0, R5F100BEGNA#W0, R5F100BFGNA#W0, R5F100BGGNA#W0
		Not mounted	A D	R5F101BAANA#U0, R5F101BCANA#U0, R5F101BDANA#U0, R5F101BEANA#U0, R5F101BFANA#U0, R5F101BGANA#U0 R5F101BAANA#W0, R5F101BCANA#W0, R5F101BDANA#W0, R5F101BEANA#W0, R5F101BFANA#W0, R5F101BGANA#W0 R5F101BADNA#U0, R5F101BCDNA#U0, R5F101BDDNA#U0, R5F101BEDNA#U0, R5F101BFDNA#U0, R5F101BGDNA#U0 R5F101BADNA#W0, R5F101BCDNA#W0, R5F101BDDNA#W0, R5F101BEDNA#W0, R5F101BFDNA#W0, R5F101BGDNA#W0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

(6/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
48 pins	48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)	Mounted	A	R5F100GAANA#U0, R5F100GCANA#U0, R5F100GDANA#U0, R5F100GEANA#U0, R5F100GFANA#U0, R5F100GGANA#U0, R5F100GHANA#U0, R5F100GJANA#U0, R5F100GKANA#U0, R5F100GLANA#U0 R5F100GAANA#W0, R5F100GCANA#W0, R5F100GDANA#W0, R5F100GEANA#W0, R5F100GFANA#W0, R5F100GGANA#W0, R5F100GHANA#W0, R5F100GJANA#W0, R5F100GKANA#W0, R5F100GLANA#W0
		Not mounted	D	R5F100GADNA#U0, R5F100GCDNA#U0, R5F100GDDNA#U0, R5F100GEDNA#U0, R5F100GFDNA#U0, R5F100GGDNA#U0, R5F100GHDNA#U0, R5F100GJDNA#U0, R5F100GKDNA#U0, R5F100GLDNA#U0 R5F100GADNA#W0, R5F100GCDNA#W0, R5F100GDDNA#W0, R5F100GEDNA#W0, R5F100GFDNA#W0, R5F100GGDNA#W0, R5F100GHDNA#W0, R5F100GJDNA#W0, R5F100GKDNA#W0, R5F100GLDNA#W0
			G	R5F100GAGNA#U0, R5F100GCGNA#U0, R5F100GDGNA#U0, R5F100GEGNA#U0, R5F100GFGNA#U0, R5F100GGGNA#U0, R5F100GHGNA#U0, R5F100GJGNA#U0 R5F100GAGNA#W0, R5F100GCGNA#W0, R5F100GDGNA#W0, R5F100GEGNA#W0, R5F100GFGNA#W0, R5F100GGGNA#W0, R5F100GHGNA#W0, R5F100GJGNA#W0
			A	R5F101GAANA#U0, R5F101GCANA#U0, R5F101GDANA#U0, R5F101GEANA#U0, R5F101GFANA#U0, R5F101GGANA#U0, R5F101GHANA#U0, R5F101GJANA#U0, R5F101GKANA#U0, R5F101GLANA#U0 R5F101GAANA#W0, R5F101GCANA#W0, R5F101GDANA#W0, R5F101GEANA#W0, R5F101GFANA#W0, R5F101GGANA#W0, R5F101GHANA#W0, R5F101GJANA#W0, R5F101GKANA#W0, R5F101GLANA#W0
			D	R5F101GADNA#U0, R5F101GCDNA#U0, R5F101GDDNA#U0, R5F101GEDNA#U0, R5F101GFDNA#U0, R5F101GGDNA#U0, R5F101GHDNA#U0, R5F101GJDNA#U0, R5F101GKDNA#U0, R5F101GLDNA#U0 R5F101GADNA#W0, R5F101GCDNA#W0, R5F101GDDNA#W0, R5F101GEDNA#W0, R5F101GFDNA#W0, R5F101GGDNA#W0, R5F101GHDNA#W0, R5F101GJDNA#W0, R5F101GKDNA#W0, R5F101GLDNA#W0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

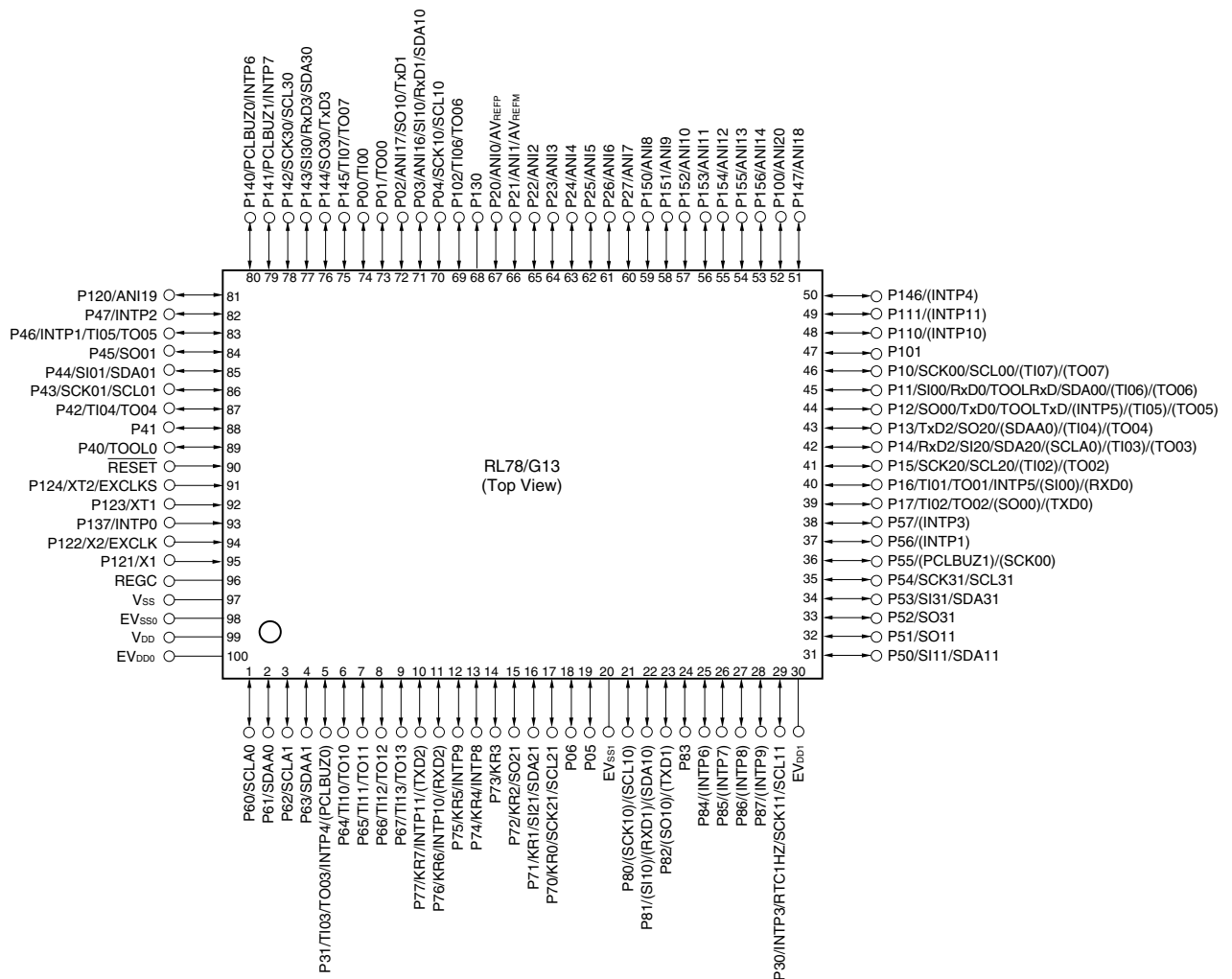
(9/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
64 pins	64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)	Mounted	A	R5F100LCAFB#V0, R5F100LDAFB#V0, R5F100LEAFB#V0, R5F100LFAFB#V0, R5F100LGAFB#V0, R5F100LHAFB#V0, R5F100LJAFB#V0, R5F100LKAFB#V0, R5F100LLAFB#V0 R5F100LCAFB#X0, R5F100LDAFB#X0, R5F100LEAFB#X0, R5F100LFAFB#X0, R5F100LGAFB#X0, R5F100LHAFB#X0, R5F100LJAFB#X0, R5F100LKAFB#X0, R5F100LLAFB#X0
			D	R5F100LCDFB#V0, R5F100LDDFB#V0, R5F100LEDFB#V0, R5F100LFDDB#V0, R5F100LGDFB#V0, R5F100LHDFB#V0, R5F100LJDFB#V0, R5F100LKDFB#V0, R5F100LLDFB#V0 R5F100LCDFB#X0, R5F100LDDFB#X0, R5F100LEDFB#X0, R5F100LFDDB#X0, R5F100LGDFB#X0, R5F100LHDFB#X0, R5F100LJDFB#X0, R5F100LKDFB#X0, R5F100LLDFB#X0
			G	R5F100LCGFB#V0, R5F100LDGFB#V0, R5F100LEGFB#V0, R5F100LFGFB#V0 R5F100LCGFB#X0, R5F100LDGFB#X0, R5F100LEGFB#X0, R5F100LFGFB#X0 R5F100LGGFB#V0, R5F100LHGFB#V0, R5F100LJGFB#V0 R5F100LGGFB#X0, R5F100LHGFB#X0, R5F100LJGFB#X0
	64-pin plastic VFPGA (4 × 4 mm, 0.4 mm pitch)	Not mounted	A	R5F101LCAFB#V0, R5F101LDAFB#V0, R5F101LEAFB#V0, R5F101LFAFB#V0, R5F101LGAFB#V0, R5F101LHAFB#V0, R5F101LJAFB#V0, R5F101LKAFB#V0, R5F101LLAFB#V0 R5F101LCAFB#X0, R5F101LDAFB#X0, R5F101LEAFB#X0, R5F101LFAFB#X0, R5F101LGAFB#X0, R5F101LHAFB#X0, R5F101LJAFB#X0, R5F101LKAFB#X0, R5F101LLAFB#X0
			D	R5F101LCDFB#V0, R5F101LDDFB#V0, R5F101LEDFB#V0, R5F101LFDDB#V0, R5F101LGDFB#V0, R5F101LHDFB#V0, R5F101LJDFB#V0, R5F101LKDFB#V0, R5F101LLDFB#V0 R5F101LCDFB#X0, R5F101LDDFB#X0, R5F101LEDFB#X0, R5F101LFDDB#X0, R5F101LGDFB#X0, R5F101LHDFB#X0, R5F101LJDFB#X0, R5F101LKDFB#X0, R5F101LLDFB#X0
	64-pin plastic VFPGA (4 × 4 mm, 0.4 mm pitch)	Mounted	A	R5F100LCABG#U0, R5F100LDABG#U0, R5F100LEABG#U0, R5F100LFABG#U0, R5F100LGABG#U0, R5F100LHABG#U0, R5F100LJABG#U0 R5F100LCABG#W0, R5F100LDABG#W0, R5F100LEABG#W0, R5F100LFABG#W0, R5F100LGABG#W0, R5F100LHABG#W0, R5F100LJABG#W0
			G	R5F100LCGBG#U0, R5F100LDGBG#U0, R5F100LEGBG#U0, R5F100LFGBG#U0, R5F100LGGBG#U0, R5F100LHGBG#U0, R5F100LJGBG#U0 R5F100LCGBG#W0, R5F100LDGBG#W0, R5F100LEGBG#W0, R5F100LFGBG#W0, R5F100LGGBG#W0, R5F100LHGBG#W0, R5F100LJGBG#W0
		Not mounted	A	R5F101LCABG#U0, R5F101LDABG#U0, R5F101LEABG#U0, R5F101LFABG#U0, R5F101LGABG#U0, R5F101LHABG#U0, R5F101LJABG#U0 R5F101LCABG#W0, R5F101LDABG#W0, R5F101LEABG#W0, R5F101LFABG#W0, R5F101LGABG#W0, R5F101LHABG#W0, R5F101LJABG#W0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

- 100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch)



- Cautions**
1. Make EV_{SS0}, EV_{SS1} pins the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is higher than EV_{DD0}, EV_{DD1} pins (EV_{DD0} = EV_{DD1}).
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

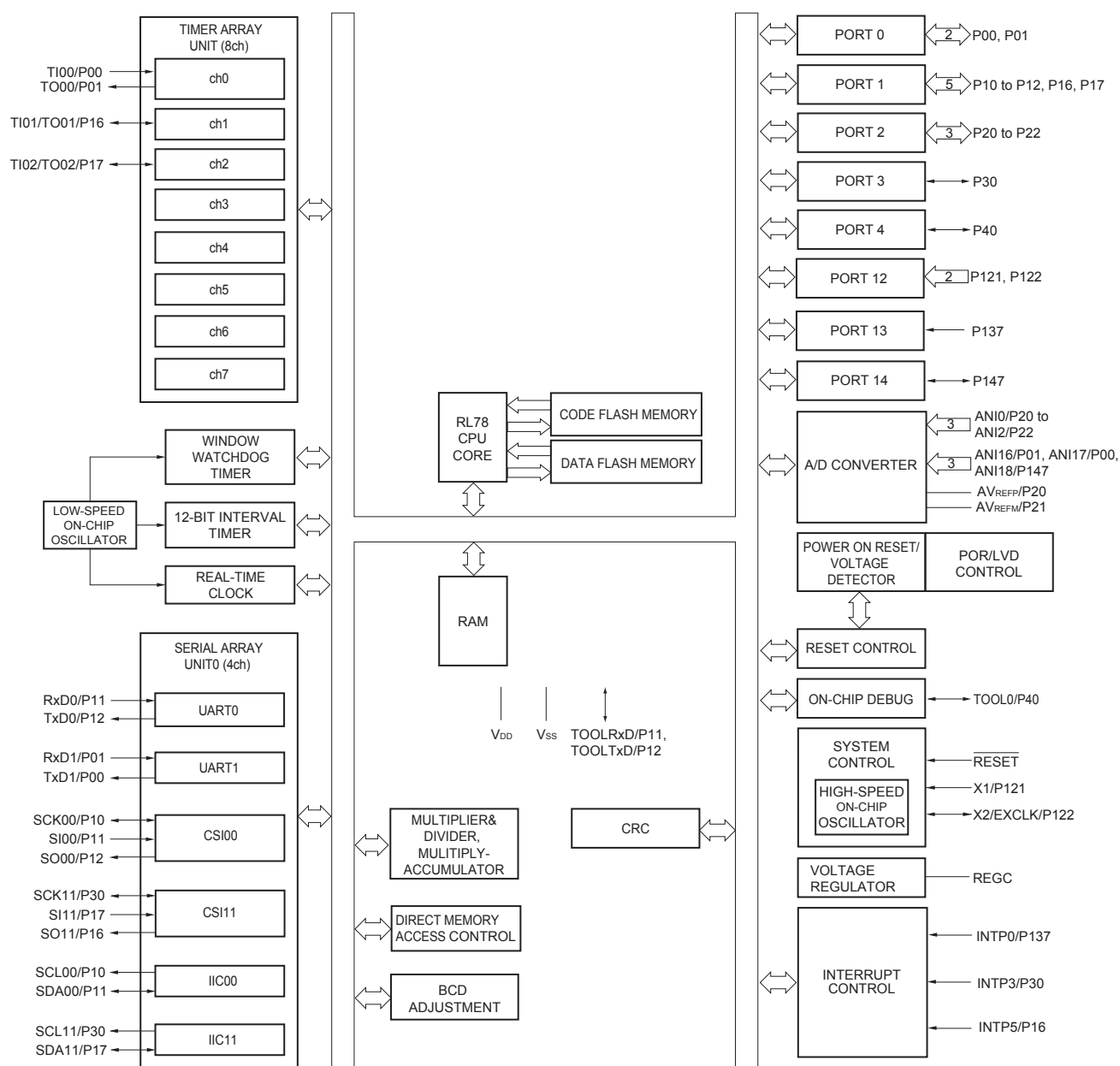
- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD}, EV_{DD0} and EV_{DD1} pins and connect the V_{SS}, EV_{SS0} and EV_{SS1} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.4 Pin Identification

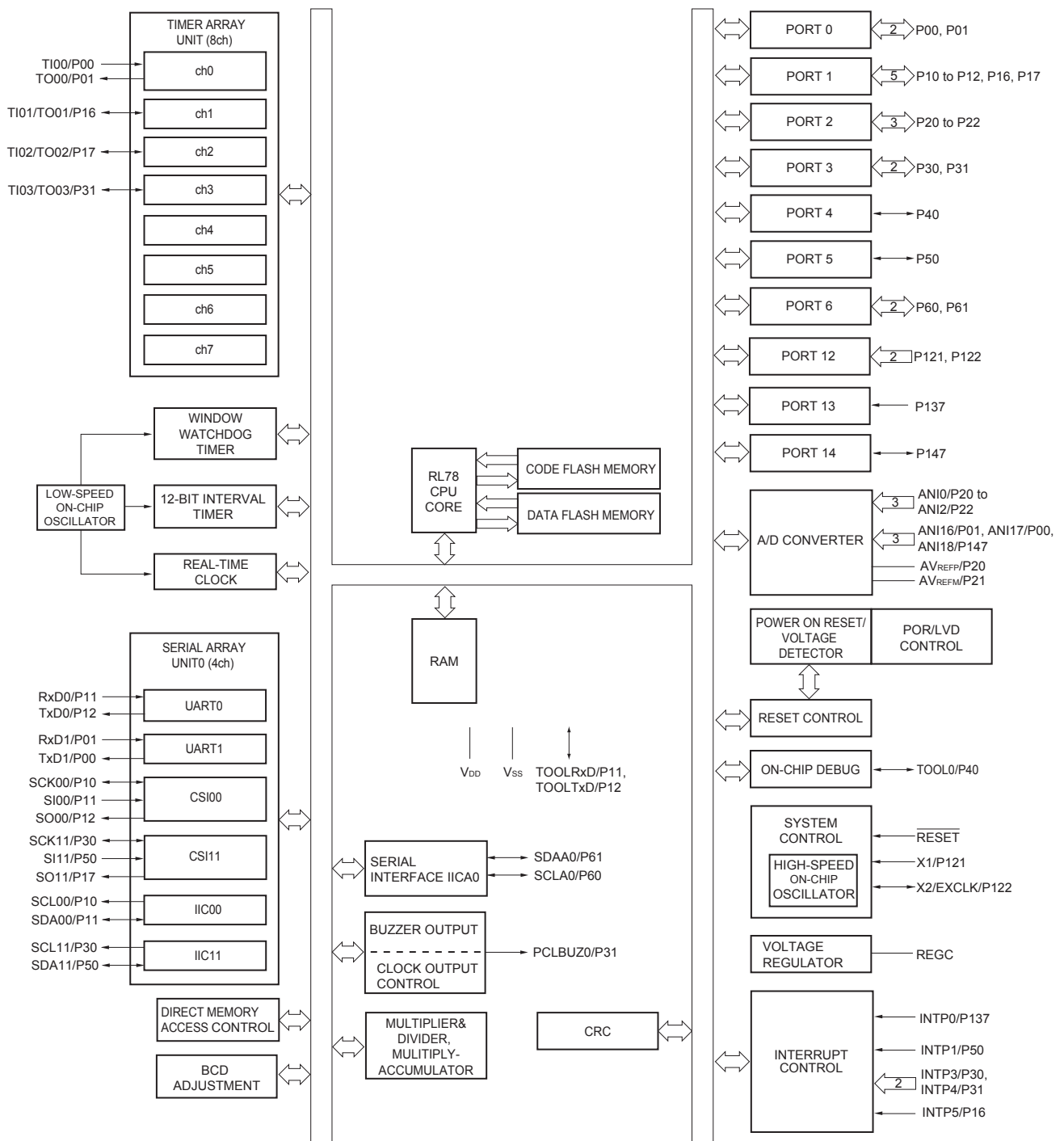
ANI0 to ANI14,		REGC:	Regulator capacitance
ANI16 to ANI26:	Analog input	RESET:	Reset
AVREFM:	A/D converter reference potential (– side) input	RTC1HZ:	Real-time clock correction clock (1 Hz) output
AVREFP:	A/D converter reference potential (+ side) input	RxD0 to RxD3:	Receive data
EVDD0, EVDD1:	Power supply for port	SCK00, SCK01, SCK10, SCK11, SCK20, SCK21,	
EVSS0, EVSS1:	Ground for port	SCLA0, SCLA1:	Serial clock input/output
EXCLK:	External clock input (Main system clock)	SCLA0, SCLA1, SCL00, SCL01, SCL10, SCL11,	
EXCLKS:	External clock input (Subsystem clock)	SCL20, SCL21, SCL30, SCL31:	Serial clock output
INTP0 to INTP11:	Interrupt request from peripheral	SDAA0, SDAA1, SDA00, SDA01, SDA10, SDA11, SDA20, SDA21, SDA30,	
KR0 to KR7:	Key return	SDA31:	Serial data input/output
P00 to P07:	Port 0	SI00, SI01, SI10, SI11,	
P10 to P17:	Port 1	SI20, SI21, SI30, SI31:	Serial data input
P20 to P27:	Port 2	SO00, SO01, SO10,	
P30 to P37:	Port 3	SO11, SO20, SO21,	
P40 to P47:	Port 4	SO30, SO31:	Serial data output
P50 to P57:	Port 5	TI00 to TI07,	
P60 to P67:	Port 6	TI10 to TI17:	Timer input
P70 to P77:	Port 7	TO00 to TO07,	
P80 to P87:	Port 8	TO10 to TO17:	Timer output
P90 to P97:	Port 9	TOOL0:	Data input/output for tool
P100 to P106:	Port 10	TOOLRxD, TOOLTxD:	Data input/output for external device
P110 to P117:	Port 11	TxD0 to TxD3:	Transmit data
P120 to P127:	Port 12	V _{DD} :	Power supply
P130, P137:	Port 13	V _{SS} :	Ground
P140 to P147:	Port 14	X1, X2:	Crystal oscillator (main system clock)
P150 to P156:	Port 15	XT1, XT2:	Crystal oscillator (subsystem clock)
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output		

1.5 Block Diagram

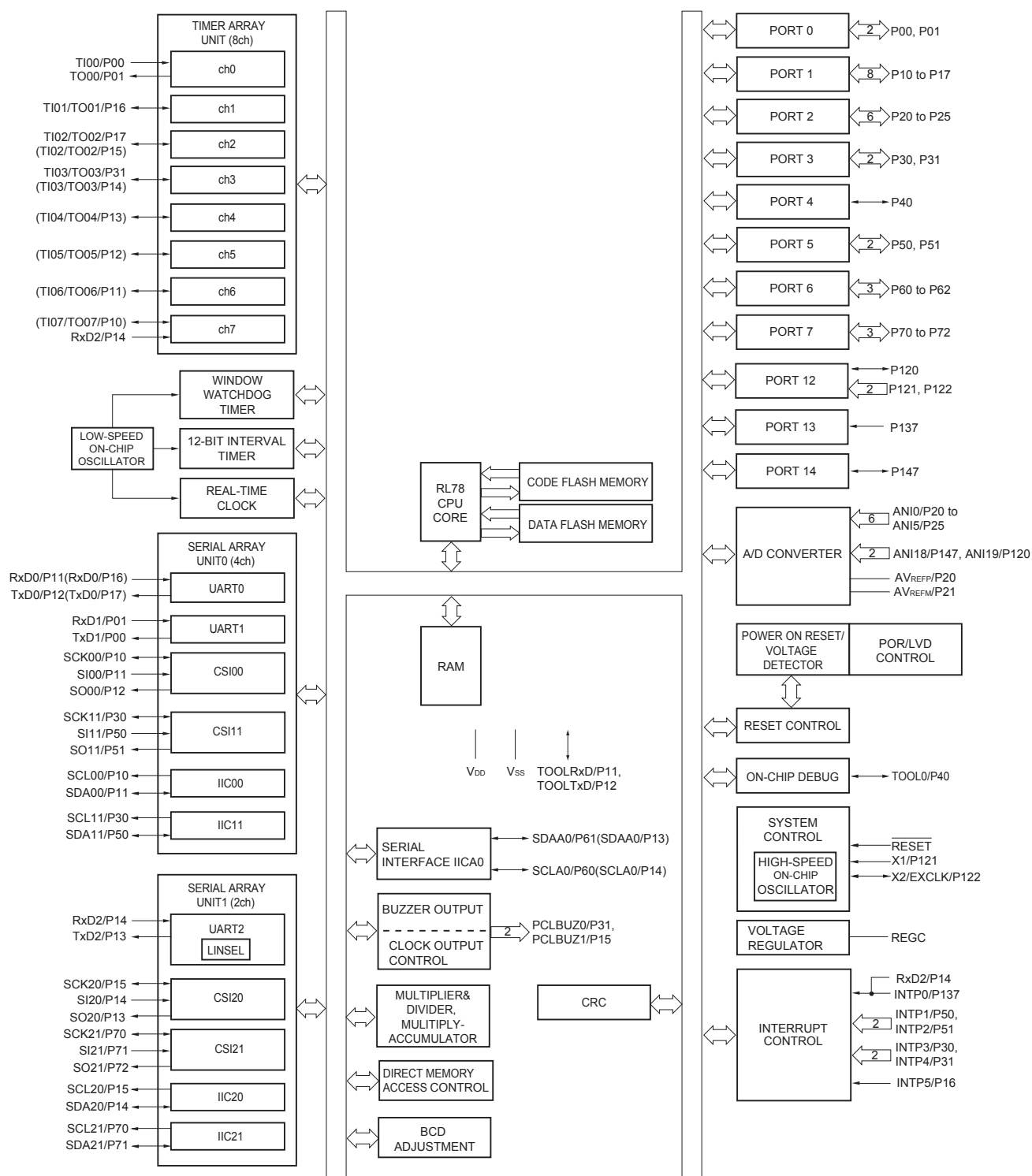
1.5.1 20-pin products



1.5.2 24-pin products



1.5.6 36-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V _{DD}		-0.5 to +6.5	V
	EV _{DD0} , EV _{DD1}	EV _{DD0} = EV _{DD1}	-0.5 to +6.5	V
	EV _{SS0} , EV _{SS1}	EV _{SS0} = EV _{SS1}	-0.5 to +0.3	V
REGC pin input voltage	V _{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V _{DD} + 0.3 ^{Note 1}	V
Input voltage	V _{I1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	-0.3 to EV _{DD0} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{I2}	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V _{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, RESET	-0.3 to V _{DD} + 0.3 ^{Note 2}	V
Output voltage	V _{O1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-0.3 to EV _{DD0} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{O2}	P20 to P27, P150 to P156	-0.3 to V _{DD} + 0.3 ^{Note 2}	V
Analog input voltage	V _{AI1}	ANI16 to ANI26	-0.3 to EV _{DD0} + 0.3 and -0.3 to AV _{REF} (+) + 0.3 ^{Notes 2, 3}	V
	V _{AI2}	ANI0 to ANI14	-0.3 to V _{DD} + 0.3 and -0.3 to AV _{REF} (+) + 0.3 ^{Notes 2, 3}	V

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed AV_{REF}(+) + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

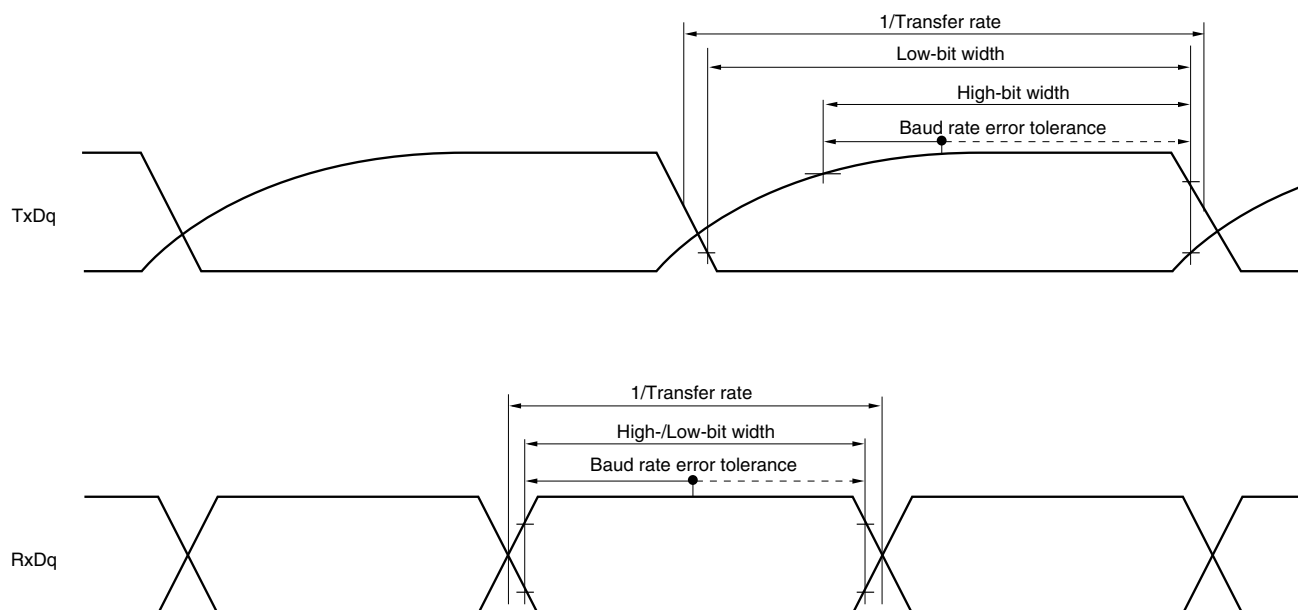
2. AV_{REF}(+) : + side reference voltage of the A/D converter.

3. V_{SS} : Reference voltage

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I _{DD1}	Operating mode	HS (high-speed main) mode Note 5	f _{IH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.3		mA
						V _{DD} = 3.0 V		2.3		mA
					Normal operation	V _{DD} = 5.0 V		5.2	8.5	mA
						V _{DD} = 3.0 V		5.2	8.5	mA
				f _{IH} = 24 MHz Note 3	Normal operation	V _{DD} = 5.0 V		4.1	6.6	mA
						V _{DD} = 3.0 V		4.1	6.6	mA
				f _{IH} = 16 MHz Note 3	Normal operation	V _{DD} = 5.0 V		3.0	4.7	mA
						V _{DD} = 3.0 V		3.0	4.7	mA
			LS (low-speed main) mode Note 5	f _{IH} = 8 MHz Note 3	Normal operation	V _{DD} = 3.0 V		1.3	2.1	mA
						V _{DD} = 2.0 V		1.3	2.1	mA
			LV (low-voltage main) mode Note 5	f _{IH} = 4 MHz Note 3	Normal operation	V _{DD} = 3.0 V		1.3	1.8	mA
						V _{DD} = 2.0 V		1.3	1.8	mA
			HS (high-speed main) mode Note 5	f _{MX} = 20 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		3.4	5.5	mA
						Resonator connection		3.6	5.7	mA
				f _{MX} = 20 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		3.4	5.5	mA
						Resonator connection		3.6	5.7	mA
				f _{MX} = 10 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		2.1	3.2	mA
						Resonator connection		2.1	3.2	mA
				f _{MX} = 10 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		2.1	3.2	mA
						Resonator connection		2.1	3.2	mA
			LS (low-speed main) mode Note 5	f _{MX} = 8 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.2	2.0	mA
				f _{MX} = 8 MHz Note 2, V _{DD} = 2.0 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.2	2.0	mA
			Subsystem clock operation	f _{SUB} = 32.768 kHz Note 4 T _A = -40°C	Normal operation	Square wave input		4.8	5.9	μA
						Resonator connection		4.9	6.0	μA
				f _{SUB} = 32.768 kHz Note 4 T _A = +25°C	Normal operation	Square wave input		4.9	5.9	μA
						Resonator connection		5.0	6.0	μA
				f _{SUB} = 32.768 kHz Note 4 T _A = +50°C	Normal operation	Square wave input		5.0	7.6	μA
						Resonator connection		5.1	7.7	μA
				f _{SUB} = 32.768 kHz Note 4 T _A = +70°C	Normal operation	Square wave input		5.2	9.3	μA
						Resonator connection		5.3	9.4	μA
				f _{SUB} = 32.768 kHz Note 4 T _A = +85°C	Normal operation	Square wave input		5.7	13.3	μA
						Resonator connection		5.8	13.4	μA

(Notes and Remarks are listed on the next page.)

UART mode bit width (during communication at different potential) (reference)

- Remarks**
1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance,
 $C_b[\text{F}]$: Communication line (TxDq) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))
 4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)
(3/3)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↓) ^{Note 1}	t _{SIK1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ	110		110		110		ns
Slp hold time (from SCKp↓) ^{Note 1}	t _{KSH1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output ^{Note 1}	t _{KSO1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ		25		25		25	ns

- Notes**
1. When DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 2. Use it with EV_{DD0} ≥ V_b.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time ^{Note 1}	t _{KCY2}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	24 MHz < f _{MCK}	14/ f _{MCK}		—		—		ns
			20 MHz < f _{MCK} ≤ 24 MHz	12/ f _{MCK}		—		—		ns
			8 MHz < f _{MCK} ≤ 20 MHz	10/ f _{MCK}		—		—		ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		16/ f _{MCK}		—		ns
			f _{MCK} ≤ 4 MHz	6/f _{MCK}		10/ f _{MCK}		10/ f _{MCK}		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	24 MHz < f _{MCK}	20/ f _{MCK}		—		—		ns
			20 MHz < f _{MCK} ≤ 24 MHz	16/ f _{MCK}		—		—		ns
			16 MHz < f _{MCK} ≤ 20 MHz	14/ f _{MCK}		—		—		ns
			8 MHz < f _{MCK} ≤ 16 MHz	12/ f _{MCK}		—		—		ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		16/ f _{MCK}		—		ns
			f _{MCK} ≤ 4 MHz	6/f _{MCK}		10/ f _{MCK}		10/ f _{MCK}		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	24 MHz < f _{MCK}	48/ f _{MCK}		—		—		ns
			20 MHz < f _{MCK} ≤ 24 MHz	36/ f _{MCK}		—		—		ns
			16 MHz < f _{MCK} ≤ 20 MHz	32/ f _{MCK}		—		—		ns
			8 MHz < f _{MCK} ≤ 16 MHz	26/ f _{MCK}		—		—		ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/ f _{MCK}		16/ f _{MCK}		—		ns
			f _{MCK} ≤ 4 MHz	10/ f _{MCK}		10/ f _{MCK}		10/ f _{MCK}		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	t _{KCY2} /2 - 12		t _{KCY2} /2 - 50		t _{KCY2} /2 - 50		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	t _{KCY2} /2 - 18		t _{KCY2} /2 - 50		t _{KCY2} /2 - 50		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	t _{KCY2} /2 - 50		t _{KCY2} /2 - 50		t _{KCY2} /2 - 50		ns
Slp setup time (to SCKp↑) ^{Note 3}	t _{SIK2}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	1/f _{MCK} + 20		1/f _{MCK} + 30		1/f _{MCK} + 30		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	1/f _{MCK} + 20		1/f _{MCK} + 30		1/f _{MCK} + 30		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	1/f _{MCK} + 30		1/f _{MCK} + 30		1/f _{MCK} + 30		ns
Slp hold time (from SCKp↑) ^{Note 4}	t _{KS12}		1/f _{MCK} + 31		1/f _{MCK} + 31		1/f _{MCK} + 31		ns
Delay time from SCKp↓ to SOp output ^{Note 5}	t _{KSO2}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		2/f _{MCK} + 120		2/f _{MCK} + 573		2/f _{MCK} + 573	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		2/f _{MCK} + 214		2/f _{MCK} + 573		2/f _{MCK} + 573	ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ		2/f _{MCK} + 573		2/f _{MCK} + 573		2/f _{MCK} + 573	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps2. Use it with EV_{DD0} ≥ V_b.

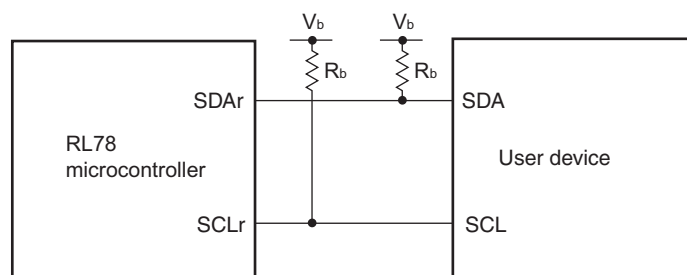
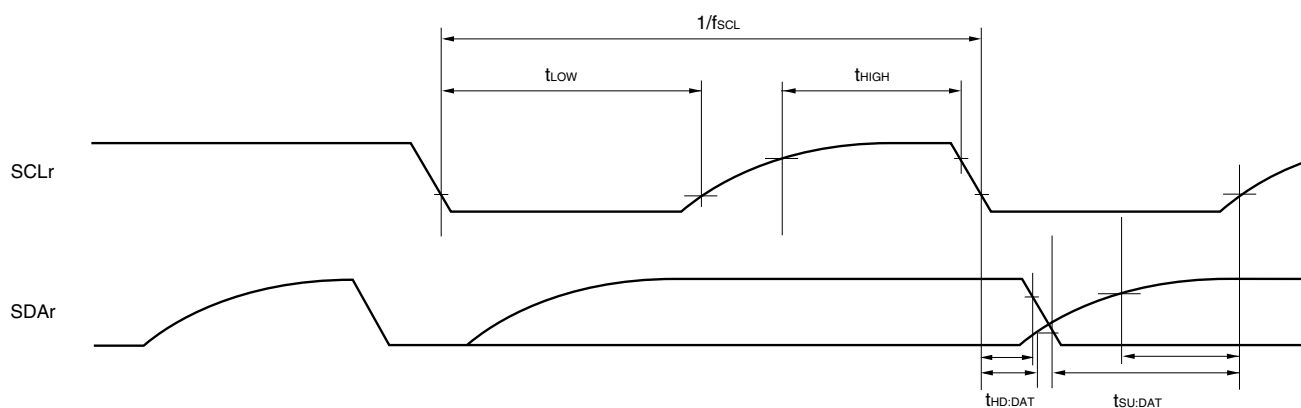
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
 2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

Remark The electrical characteristics of the products G: Industrial applications ($T_A = -40$ to $+105^\circ\text{C}$) are different from those of the products “A: Consumer applications, and D: Industrial applications”. For details, refer to 3.1 to 3.10.

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to $+6.5$	V
	EV_{DD0}, EV_{DD1}	$EV_{DD0} = EV_{DD1}$	-0.5 to $+6.5$	V
	EV_{SS0}, EV_{SS1}	$EV_{SS0} = EV_{SS1}$	-0.5 to $+0.3$	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to $+2.8$ and -0.3 to $V_{DD} + 0.3$ ^{Note 1}	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	-0.3 to $EV_{DD0} + 0.3$ and -0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
	V_{I2}	P60 to P63 (N-ch open-drain)	-0.3 to $+6.5$	V
	V_{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, RESET	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
Output voltage	V_{O1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-0.3 to $EV_{DD0} + 0.3$ and -0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
	V_{O2}	P20 to P27, P150 to P156	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
Analog input voltage	V_{AI1}	ANI16 to ANI26	-0.3 to $EV_{DD0} + 0.3$ and -0.3 to $AV_{REF(+)} + 0.3$ ^{Notes 2, 3}	V
	V_{AI2}	ANI0 to ANI14	-0.3 to $V_{DD} + 0.3$ and -0.3 to $AV_{REF(+)} + 0.3$ ^{Notes 2, 3}	V

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed $AV_{REF(+)} + 0.3$ V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

3. V_{SS} : Reference voltage

Absolute Maximum Ratings ($T_A = 25^{\circ}\text{C}$) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I _{OH1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	−70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	−100	mA
	I _{OH2}	Per pin	P20 to P27, P150 to P156	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I _{OL1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
	I _{OL2}	Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T _A	In normal operation mode		−40 to +105	°C
		In flash memory programming mode			
Storage temperature	T _{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- Notes**
1. Total current flowing into V_{DD} and EV_{DD0} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When $AMPHS1 = 1$ (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 32 MHz
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 16 MHz

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

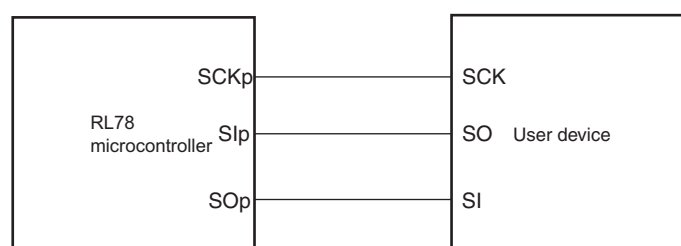
(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time ^{Note 5}	t_{KCY2}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	$20\text{ MHz} < f_{\text{MCK}}$	$16/f_{\text{MCK}}$		ns
			$f_{\text{MCK}} \leq 20\text{ MHz}$	$12/f_{\text{MCK}}$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	$16\text{ MHz} < f_{\text{MCK}}$	$16/f_{\text{MCK}}$		ns
			$f_{\text{MCK}} \leq 16\text{ MHz}$	$12/f_{\text{MCK}}$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$		$16/f_{\text{MCK}}$		ns
				$12/f_{\text{MCK}}$ and 1000		ns
SCKp high-/low-level width	$t_{\text{KH2}}, t_{\text{KL2}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$		$t_{\text{KCY2}}/2 - 14$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$		$t_{\text{KCY2}}/2 - 16$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$		$t_{\text{KCY2}}/2 - 36$		ns
Slp setup time (to SCKp $\uparrow$) ^{Note 1}	t_{SIK2}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$		$1/f_{\text{MCK}} + 40$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$		$1/f_{\text{MCK}} + 60$		ns
Slp hold time (from SCKp $\uparrow$) ^{Note 2}	t_{KSI2}	$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$		$1/f_{\text{MCK}} + 62$		ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note 3}	t_{KS02}	$C = 30\text{ pF}$ ^{Note 4}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$		$2/f_{\text{MCK}} + 66$	ns
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$		$2/f_{\text{MCK}} + 113$	ns

- Notes**
1. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp setup time becomes “to SCKp $\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 2. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp hold time becomes “from SCKp $\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 3. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The delay time to SOp output becomes “from SCKp $\uparrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 4. C is the load capacitance of the SOp output lines.
 5. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

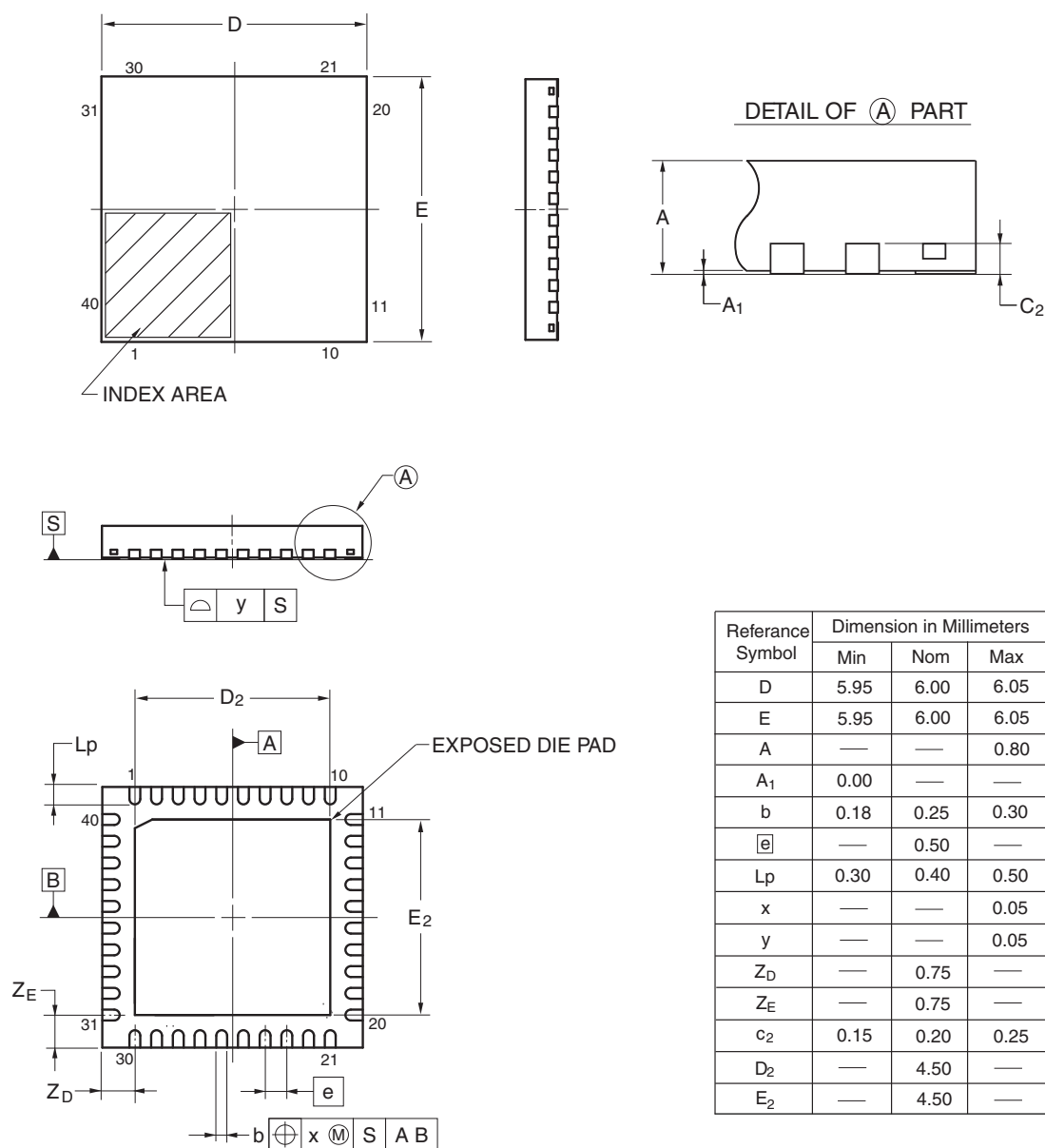
- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

CSI mode connection diagram (during communication at same potential)

4.7 40-pin Products

R5F100EAANA, R5F100ECANA, R5F100EDANA, R5F100EEANA, R5F100EFANA, R5F100EGANA, R5F100EHANA
 R5F101EAANA, R5F101ECANA, R5F101EDANA, R5F101EEANA, R5F101EFANA, R5F101EGANA, R5F101EHANA
 R5F100EADNA, R5F100ECDNA, R5F100EDDNA, R5F100EEDNA, R5F100EFDNA, R5F100EGDNA,
 R5F100EHDNA
 R5F101EADNA, R5F101ECDNA, R5F101EDDNA, R5F101EEDNA, R5F101EFDNA, R5F101EGDNA,
 R5F101EHDNA
 R5F100EAGNA, R5F100ECGNA, R5F100EDGNA, R5F100EEGNA, R5F100EFGNA, R5F100EGGNA,
 R5F100EHGNA

JEITA Package code	RENESAS code	Previous code	MASS (TYP.) [g]
P-HWQFN40-6x6-0.50	PWQN0040KC-A	P40K8-50-4B4-5	0.09



©2013 Renesas Electronics Corporation. All rights reserved.