



Welcome to [E-XFL.COM](#)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	30-LSSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100aggsp-v0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100aggsp-v0</a>

Table 1-1. List of Ordering Part Numbers

(6/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
48 pins	48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)	Mounted	A	R5F100GAANA#U0, R5F100GCANA#U0, R5F100GDANA#U0, R5F100GEANA#U0, R5F100GFANA#U0, R5F100GGANA#U0, R5F100GHANA#U0, R5F100GJANA#U0, R5F100GKANA#U0, R5F100GLANA#U0 R5F100GAANA#W0, R5F100GCANA#W0, R5F100GDANA#W0, R5F100GEANA#W0, R5F100GFANA#W0, R5F100GGANA#W0, R5F100GHANA#W0, R5F100GJANA#W0, R5F100GKANA#W0, R5F100GLANA#W0
		Not mounted	D	R5F100GADNA#U0, R5F100GCDNA#U0, R5F100GDDNA#U0, R5F100GEDNA#U0, R5F100GFDNA#U0, R5F100GGDNA#U0, R5F100GHDNA#U0, R5F100GJDNA#U0, R5F100GKDNA#U0, R5F100GLDNA#U0 R5F100GADNA#W0, R5F100GCDNA#W0, R5F100GDDNA#W0, R5F100GEDNA#W0, R5F100GFDNA#W0, R5F100GGDNA#W0, R5F100GHDNA#W0, R5F100GJDNA#W0, R5F100GKDNA#W0, R5F100GLDNA#W0
			G	R5F100GAGNA#U0, R5F100GCGNA#U0, R5F100GDGNA#U0, R5F100GEGNA#U0, R5F100GFGNA#U0, R5F100GGGNA#U0, R5F100GHGNA#U0, R5F100GJGNA#U0 R5F100GAGNA#W0, R5F100GCGNA#W0, R5F100GDGNA#W0, R5F100GEGNA#W0, R5F100GFGNA#W0, R5F100GGGNA#W0, R5F100GHGNA#W0, R5F100GJGNA#W0
			A	R5F101GAANA#U0, R5F101GCANA#U0, R5F101GDANA#U0, R5F101GEANA#U0, R5F101GFANA#U0, R5F101GGANA#U0, R5F101GHANA#U0, R5F101GJANA#U0, R5F101GKANA#U0, R5F101GLANA#U0 R5F101GAANA#W0, R5F101GCANA#W0, R5F101GDANA#W0, R5F101GEANA#W0, R5F101GFANA#W0, R5F101GGANA#W0, R5F101GHANA#W0, R5F101GJANA#W0, R5F101GKANA#W0, R5F101GLANA#W0
			D	R5F101GADNA#U0, R5F101GCDNA#U0, R5F101GDDNA#U0, R5F101GEDNA#U0, R5F101GFDNA#U0, R5F101GGDNA#U0, R5F101GHDNA#U0, R5F101GJDNA#U0, R5F101GKDNA#U0, R5F101GLDNA#U0 R5F101GADNA#W0, R5F101GCDNA#W0, R5F101GDDNA#W0, R5F101GEDNA#W0, R5F101GFDNA#W0, R5F101GGDNA#W0, R5F101GHDNA#W0, R5F101GJDNA#W0, R5F101GKDNA#W0, R5F101GLDNA#W0

**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

**Caution** The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

### Table 1-1. List of Ordering Part Numbers

(7/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
52 pins	52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)	Mounted	<p>A</p> <p>D</p> <p>G</p>	<p>R5F100JCAFA#V0, R5F100JDAFA#V0, R5F100JEAFA#V0, R5F100JFAFA#V0, R5F100JGAFA#V0, R5F100JHAFA#V0, R5F100JJAFA#V0, R5F100JKAF#V0, R5F100JLAFA#V0</p> <p>R5F100JCAFA#X0, R5F100JDAFA#X0, R5F100JEAFA#X0, R5F100JFAFA#X0, R5F100JGAFA#X0, R5F100JHAFA#X0, R5F100JJAFA#X0, R5F100JKAF#X0, R5F100JLAFA#X0</p> <p>R5F100JCDAFA#V0, R5F100JDDFA#V0, R5F100JEDFA#V0, R5F100JFDAFA#V0, R5F100JGDFA#V0, R5F100JHDAFA#V0, R5F100JDDFA#V0, R5F100JKDAFA#V0, R5F100JLDAFA#V0</p> <p>R5F100JCDAFA#X0, R5F100JDDFA#X0, R5F100JEDFA#X0, R5F100JFDAFA#X0, R5F100JGDFA#X0, R5F100JHDAFA#X0, R5F100JDDFA#X0, R5F100JKDAFA#X0, R5F100JLDAFA#X0</p> <p>R5F100JCGFA#V0, R5F100JDGFA#V0, R5F100JEGFA#V0, R5F100JFGFA#V0, R5F100JGGFA#V0, R5F100JHGFA#V0, R5F100JJGFA#V0</p> <p>R5F100JCGFA#X0, R5F100JDGFA#X0, R5F100JEGFA#X0, R5F100JFGFA#X0, R5F100JGGFA#X0, R5F100JHGFA#X0, R5F100JJGFA#X0</p>
		Not mounted	<p>A</p> <p>D</p>	<p>R5F101JCAFA#V0, R5F101JDAFA#V0, R5F101JEAFA#V0, R5F101JFAFA#V0, R5F101JGAFA#V0, R5F101JHAFA#V0, R5F101JJAFA#V0, R5F101JKAF#V0, R5F101JLAFA#V0</p> <p>R5F101JCAFA#X0, R5F101JDAFA#X0, R5F101JEAFA#X0, R5F101JFAFA#X0, R5F101JGAFA#X0, R5F101JHAFA#X0, R5F101JJAFA#X0, R5F101JKAF#X0, R5F101JLAFA#X0</p> <p>R5F101JCDAFA#V0, R5F101JDDFA#V0, R5F101JEDFA#V0, R5F101JFDAFA#V0, R5F101JGDFA#V0, R5F101JHDAFA#V0, R5F101JDDFA#V0, R5F101JKDAFA#V0, R5F101JLDAFA#V0</p> <p>R5F101JCDAFA#X0, R5F101JDDFA#X0, R5F101JEDFA#X0, R5F101JFDAFA#X0, R5F101JGDFA#X0, R5F101JHDAFA#X0, R5F101JDDFA#X0, R5F101JKDAFA#X0, R5F101JLDAFA#X0</p>

**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

**Caution** The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

(10/12)

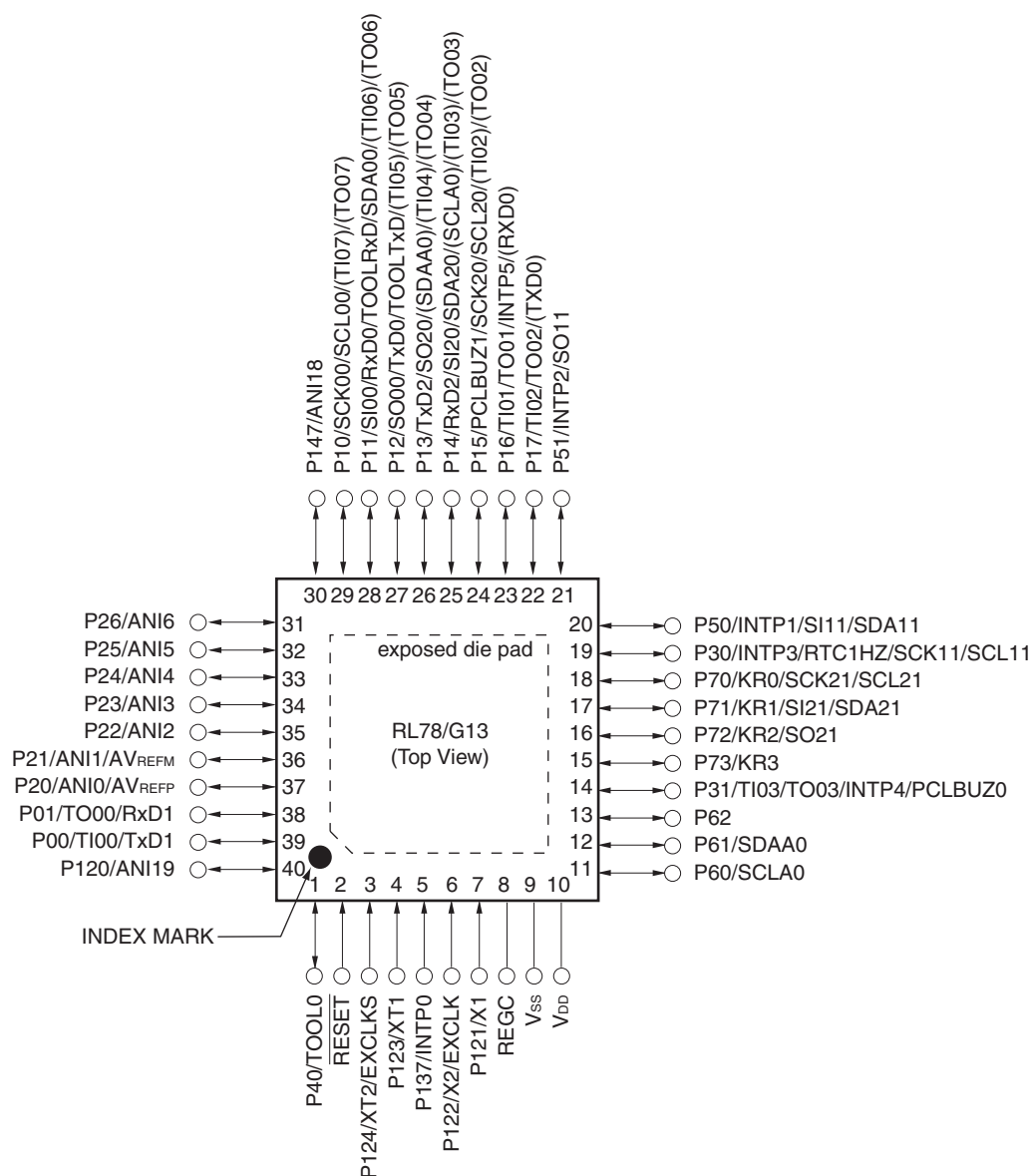
Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
80 pins	80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)	Mounted	A	R5F100MFAFA#V0, R5F100MGFAFA#V0, R5F100MHAFA#V0, R5F100MJFAFA#V0, R5F100MKAFA#V0, R5F100MLAFA#V0 R5F100MFAFA#X0, R5F100MGFAFA#X0, R5F100MHAFA#X0, R5F100MJFAFA#X0, R5F100MKAFA#X0, R5F100MLAFA#X0
			D	R5F100MFDFA#V0, R5F100MGDFA#V0, R5F100MHDFA#V0, R5F100MJDFA#V0, R5F100MKDFA#V0, R5F100MLDFA#V0 R5F100MFDFA#X0, R5F100MGDFA#X0, R5F100MHDFA#X0, R5F100MJDFA#X0, R5F100MKDFA#X0, R5F100MLDFA#X0
			G	R5F100MFGFA#V0, R5F100MGGFA#V0, R5F100MHGFA#V0, R5F100MJGFA#V0 R5F100MFGFA#X0, R5F100MGGFA#X0, R5F100MHGFA#X0, R5F100MJGFA#X0
		Not mounted	A	R5F101MFAFA#V0, R5F101MGFAFA#V0, R5F101MHAFA#V0, R5F101MJFAFA#V0, R5F101MKAFA#V0, R5F101MLAFA#V0 R5F101MFAFA#X0, R5F101MGFAFA#X0, R5F101MHAFA#X0, R5F101MJFAFA#X0, R5F101MKAFA#X0, R5F101MLAFA#X0
			D	R5F101MFDFA#V0, R5F101MGDFA#V0, R5F101MHDFA#V0, R5F101MJDFA#V0, R5F101MKDFA#V0, R5F101MLDFA#V0 R5F101MFDFA#X0, R5F101MGDFA#X0, R5F101MHDFA#X0, R5F101MJDFA#X0, R5F101MKDFA#X0, R5F101MLDFA#X0
			G	R5F101MFGFA#V0, R5F101MGGFA#V0, R5F101MHGFA#V0, R5F101MJGFA#V0 R5F101MFGFA#X0, R5F101MGGFA#X0, R5F101MHGFA#X0, R5F101MJGFA#X0
	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	Mounted	A	R5F100MFAFB#V0, R5F100MGAFB#V0, R5F100MHAFB#V0, R5F100MJAFB#V0, R5F100MKAFB#V0, R5F100MLAFB#V0 R5F100MFAFB#X0, R5F100MGAFB#X0, R5F100MHAFB#X0, R5F100MJAFB#X0, R5F100MKAFB#X0, R5F100MLAFB#X0
			D	R5F100MFDDB#V0, R5F100MGDFB#V0, R5F100MHDDB#V0, R5F100MJDFB#V0, R5F100MKDFB#V0, R5F100MLDFB#V0 R5F100MFDDB#X0, R5F100MGDFB#X0, R5F100MHDDB#X0, R5F100MJDFB#X0, R5F100MKDFB#X0, R5F100MLDFB#X0
			G	R5F100MFGFB#V0, R5F100MGGFB#V0, R5F100MHGFB#V0, R5F100MJGFB#V0 R5F100MFGFB#X0, R5F100MGGFB#X0, R5F100MHGFB#X0, R5F100MJGFB#X0
		Not mounted	A	R5F101MFAFB#V0, R5F101MGAFB#V0, R5F101MHAFB#V0, R5F101MJAFB#V0, R5F101MKAFB#V0, R5F101MLAFB#V0 R5F101MFAFB#X0, R5F101MGAFB#X0, R5F101MHAFB#X0, R5F101MJAFB#X0, R5F101MKAFB#X0, R5F101MLAFB#X0
			D	R5F101MFDDB#V0, R5F101MGDFB#V0, R5F101MHDDB#V0, R5F101MJDFB#V0, R5F101MKDFB#V0, R5F101MLDFB#V0 R5F101MFDDB#X0, R5F101MGDFB#X0, R5F101MHDDB#X0, R5F101MJDFB#X0, R5F101MKDFB#X0, R5F101MLDFB#X0
			G	R5F101MFGFB#V0, R5F101MGGFB#V0, R5F101MHGFB#V0, R5F101MJGFB#V0 R5F101MFGFB#X0, R5F101MGGFB#X0, R5F101MHGFB#X0, R5F101MJGFB#X0

**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

**Caution** The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

## 1.3.7 40-pin products

- 40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)



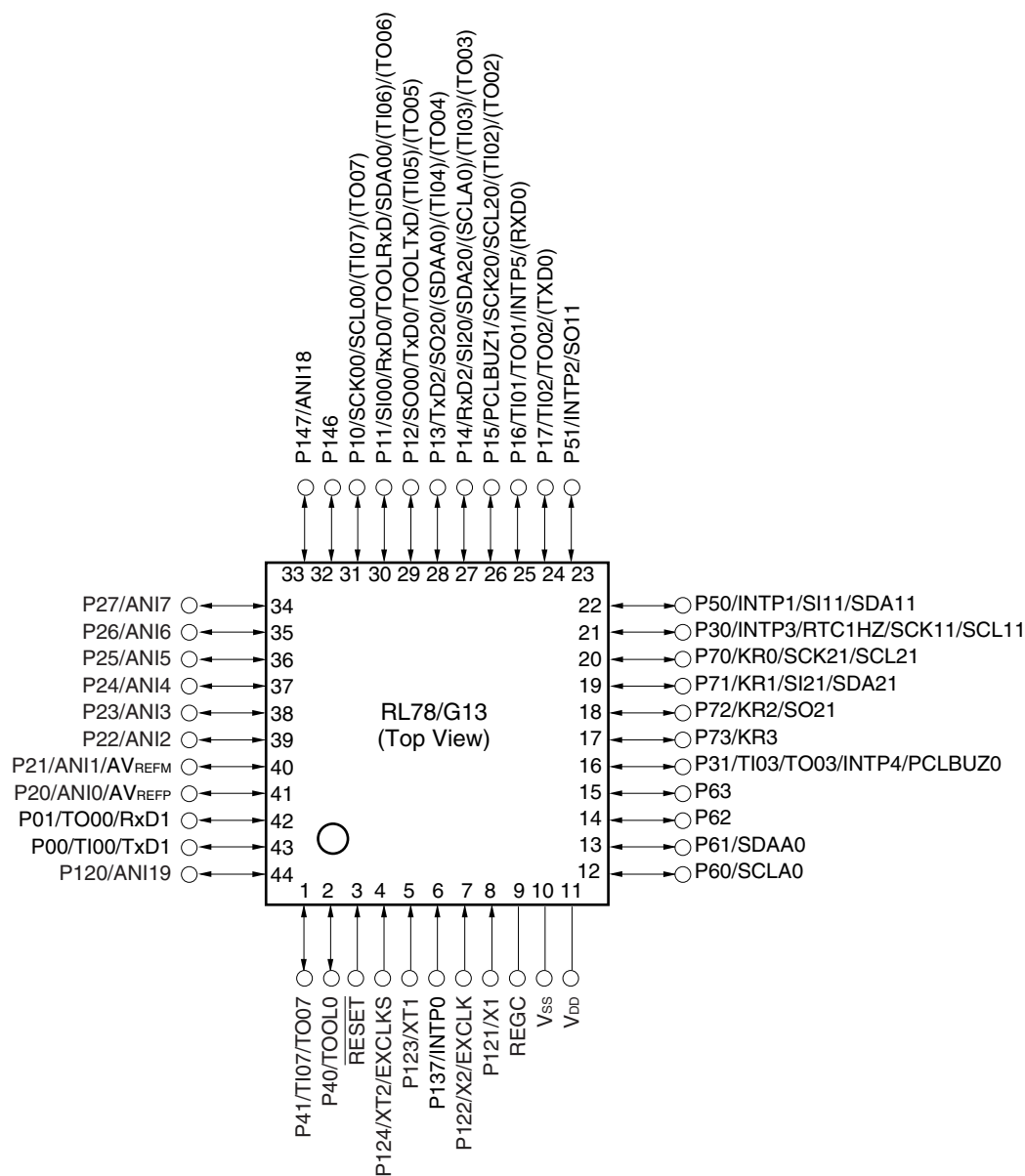
**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1 μF).

**Remarks 1.** For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.
- It is recommended to connect an exposed die pad to V<sub>SS</sub>.

## 1.3.8 44-pin products

- 44-pin plastic LQFP (10 × 10 mm, 0.8 mm pitch)



**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1  $\mu$ F).

**Remarks 1.** For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (3/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V <sub>IH1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0.8EV <sub>DD0</sub>	EV <sub>DD0</sub>	V
	V <sub>IH2</sub>	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	2.2	EV <sub>DD0</sub>	V
			TTL input buffer 3.3 V ≤ EV <sub>DD0</sub> < 4.0 V	2.0	EV <sub>DD0</sub>	V
			TTL input buffer 1.6 V ≤ EV <sub>DD0</sub> < 3.3 V	1.5	EV <sub>DD0</sub>	V
	V <sub>IH3</sub>	P20 to P27, P150 to P156	0.7V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH4</sub>	P60 to P63	0.7EV <sub>DD0</sub>		6.0	V
	V <sub>IH5</sub>	P121 to P124, P137, EXCLK, EXCLKS, RESET	0.8V <sub>DD</sub>		V <sub>DD</sub>	V
Input voltage, low	V <sub>IL1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0	0.2EV <sub>DD0</sub>	V
	V <sub>IL2</sub>	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	0	0.8	V
			TTL input buffer 3.3 V ≤ EV <sub>DD0</sub> < 4.0 V	0	0.5	V
			TTL input buffer 1.6 V ≤ EV <sub>DD0</sub> < 3.3 V	0	0.32	V
	V <sub>IL3</sub>	P20 to P27, P150 to P156	0		0.3V <sub>DD</sub>	V
	V <sub>IL4</sub>	P60 to P63	0		0.3EV <sub>DD0</sub>	V
	V <sub>IL5</sub>	P121 to P124, P137, EXCLK, EXCLKS, RESET	0		0.2V <sub>DD</sub>	V

**Caution** The maximum value of V<sub>IH</sub> of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 is EV<sub>DD0</sub>, even in the N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ E<sub>VDD0</sub> = E<sub>VDD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = E<sub>VSS0</sub> = E<sub>VSS1</sub> = 0 V) (4/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V <sub>OH1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OH1</sub> = -10.0 mA	E <sub>VDD0</sub> - 1.5		V
			4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OH1</sub> = -3.0 mA	E <sub>VDD0</sub> - 0.7		V
			2.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OH1</sub> = -2.0 mA	E <sub>VDD0</sub> - 0.6		V
			1.8 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OH1</sub> = -1.5 mA	E <sub>VDD0</sub> - 0.5		V
			1.6 V ≤ E <sub>VDD0</sub> < 5.5 V, I <sub>OH1</sub> = -1.0 mA	E <sub>VDD0</sub> - 0.5		V
	V <sub>OH2</sub>	P20 to P27, P150 to P156	1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V, I <sub>OH2</sub> = -100 μA	V <sub>DD</sub> - 0.5		V
Output voltage, low	V <sub>OL1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 20 mA		1.3	V
			4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 8.5 mA		0.7	V
			2.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 3.0 mA		0.6	V
			2.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 1.5 mA		0.4	V
			1.8 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 0.6 mA		0.4	V
			1.6 V ≤ E <sub>VDD0</sub> < 5.5 V, I <sub>OL1</sub> = 0.3 mA		0.4	V
	V <sub>OL2</sub>	P20 to P27, P150 to P156	1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V, I <sub>OL2</sub> = 400 μA		0.4	V
	V <sub>OL3</sub>	P60 to P63	4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL3</sub> = 15.0 mA		2.0	V
			4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL3</sub> = 5.0 mA		0.4	V
			2.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL3</sub> = 3.0 mA		0.4	V
			1.8 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL3</sub> = 2.0 mA		0.4	V
			1.6 V ≤ E <sub>VDD0</sub> < 5.5 V, I <sub>OL3</sub> = 1.0 mA		0.4	V

**Caution** P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



**(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products****(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ E<sub>VDD0</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = E<sub>VSS0</sub> = 0 V) (2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I <sub>DD2</sub> Note 2	HALT mode	HS (high-speed main) mode Note 7	f <sub>IH</sub> = 32 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V		0.54	1.63	mA	
					V <sub>DD</sub> = 3.0 V		0.54	1.63	mA	
				f <sub>IH</sub> = 24 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V		0.44	1.28	mA	
					V <sub>DD</sub> = 3.0 V		0.44	1.28	mA	
				f <sub>IH</sub> = 16 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V		0.40	1.00	mA	
					V <sub>DD</sub> = 3.0 V		0.40	1.00	mA	
				LS (low-speed main) mode Note 7	f <sub>IH</sub> = 8 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 3.0 V		260	530	μA
						V <sub>DD</sub> = 2.0 V		260	530	μA
				LV (low-voltage main) mode Note 7	f <sub>IH</sub> = 4 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 3.0 V		420	640	μA
						V <sub>DD</sub> = 2.0 V		420	640	μA
			HS (high-speed main) mode Note 7	f <sub>MX</sub> = 20 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 5.0 V	Square wave input		0.28	1.00	mA	
					Resonator connection		0.45	1.17	mA	
				f <sub>MX</sub> = 20 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 3.0 V	Square wave input		0.28	1.00	mA	
					Resonator connection		0.45	1.17	mA	
				f <sub>MX</sub> = 10 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 5.0 V	Square wave input		0.19	0.60	mA	
					Resonator connection		0.26	0.67	mA	
				f <sub>MX</sub> = 10 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 3.0 V	Square wave input		0.19	0.60	mA	
					Resonator connection		0.26	0.67	mA	
			LS (low-speed main) mode Note 7	f <sub>MX</sub> = 8 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 3.0 V	Square wave input		95	330	μA	
					Resonator connection		145	380	μA	
				f <sub>MX</sub> = 8 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 2.0 V	Square wave input		95	330	μA	
					Resonator connection		145	380	μA	
			Subsystem clock operation	f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = −40°C	Square wave input		0.25	0.57	μA	
					Resonator connection		0.44	0.76	μA	
				f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = +25°C	Square wave input		0.30	0.57	μA	
					Resonator connection		0.49	0.76	μA	
				f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = +50°C	Square wave input		0.37	1.17	μA	
					Resonator connection		0.56	1.36	μA	
				f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = +70°C	Square wave input		0.53	1.97	μA	
					Resonator connection		0.72	2.16	μA	
				f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = +85°C	Square wave input		0.82	3.37	μA	
					Resonator connection		1.01	3.56	μA	
	I <sub>DD3</sub> <sup>Note 6</sup>	STOP mode <sup>Note 8</sup>	T <sub>A</sub> = −40°C					0.18	0.50	μA
			T <sub>A</sub> = +25°C					0.23	0.50	μA
			T <sub>A</sub> = +50°C					0.30	1.10	μA
			T <sub>A</sub> = +70°C					0.46	1.90	μA
			T <sub>A</sub> = +85°C					0.75	3.30	μA

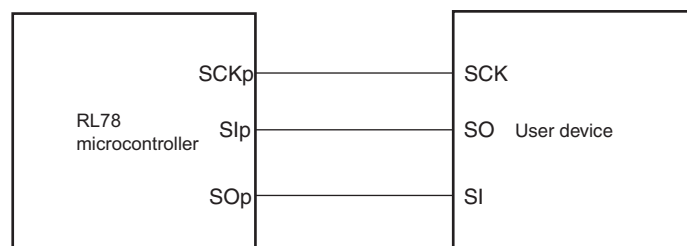
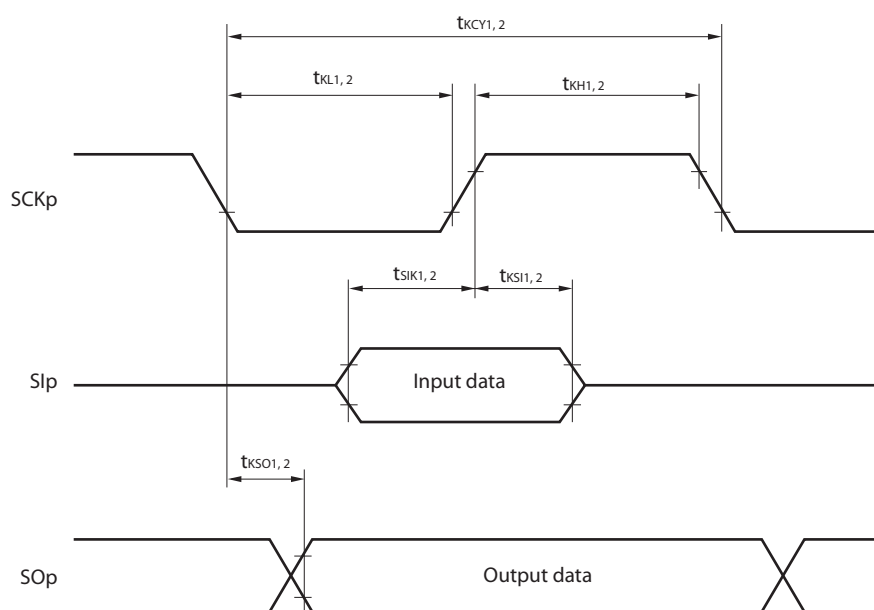
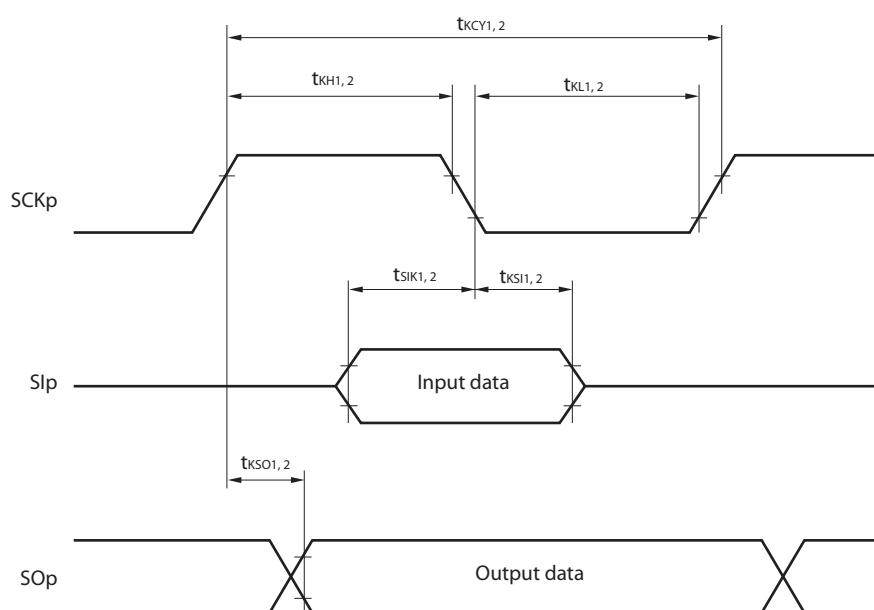
(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into  $V_{DD}$  and  $EV_{DD0}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$  or  $V_{SS}$ ,  $EV_{SS0}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. During HALT instruction execution by flash memory.
  3. When high-speed on-chip oscillator and subsystem clock are stopped.
  4. When high-speed system clock and subsystem clock are stopped.
  5. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $RTCLPC = 1$  and setting ultra-low current consumption ( $AMPHS1 = 1$ ). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.  
HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 32 MHz  
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 16 MHz  
LS (low-speed main) mode:  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 8 MHz  
LV (low-voltage main) mode:  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 4 MHz
  8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

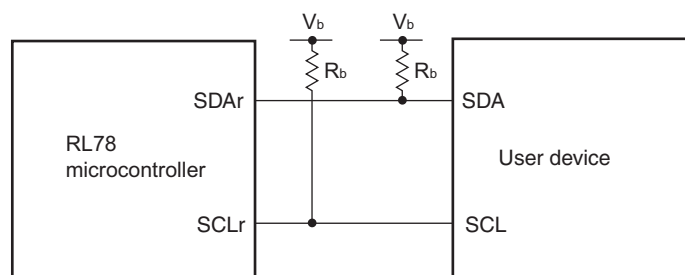
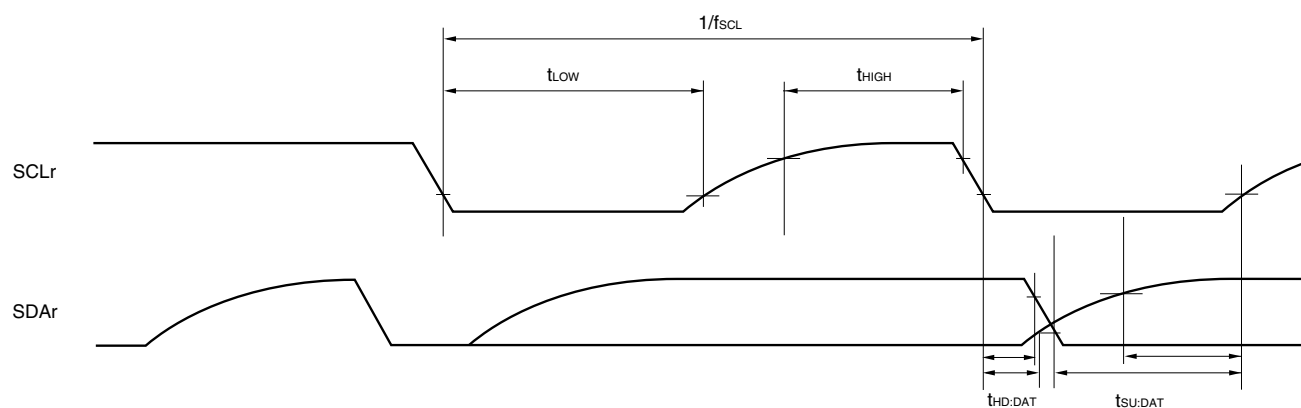
- Remarks 1.** f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
3. f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of  $I_{DD1}$  or  $I_{DD2}$  and  $I_{ADC}$  when the A/D converter operates in an operation mode or the HALT mode.
7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of  $I_{DD1}$ ,  $I_{DD2}$  or  $I_{DD3}$  and  $I_{LVD}$  when the LVD circuit is in operation.
8. Current flowing only during data flash rewrite.
9. Current flowing only during self programming.
10. For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode**.

- Remarks**
1.  $f_{IL}$ : Low-speed on-chip oscillator clock frequency
  2.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  3.  $f_{CLK}$ : CPU/peripheral hardware clock frequency
  4. Temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$

**CSI mode connection diagram (during communication at same potential)****CSI mode serial transfer timing (during communication at same potential)  
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)****CSI mode serial transfer timing (during communication at same potential)  
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
  2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

**Simplified I<sup>2</sup>C mode connection diagram (during communication at different potential)****Simplified I<sup>2</sup>C mode serial transfer timing (during communication at different potential)**

- Remarks**
1.  $R_b[\Omega]$ : Communication line (SDAr, SCLr) pull-up resistance,  $C_b[F]$ : Communication line (SDAr, SCLr) load capacitance,  $V_b[V]$ : Communication line voltage
  2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)
  3.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

&lt;R&gt;

- Notes**
1. The first clock pulse is generated after this period when the start/restart condition is detected.
  2. The maximum value (MAX.) of t<sub>HD:DAT</sub> is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution** The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I<sub>OH1</sub>, I<sub>OL1</sub>, V<sub>OH1</sub>, V<sub>OL1</sub>) must satisfy the values in the redirect destination.

**Remark** The maximum value of C<sub>b</sub> (communication line capacitance) and the value of R<sub>b</sub> (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C<sub>b</sub> = 400 pF, R<sub>b</sub> = 2.7 kΩ

- Notes**
1. Total current flowing into  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , or  $V_{SS}$ ,  $EV_{SS0}$ , and  $EV_{SS1}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. When high-speed on-chip oscillator and subsystem clock are stopped.
  3. When high-speed system clock and subsystem clock are stopped.
  4. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $AMPHS1 = 1$  (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$

$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$

## 3.4 AC Characteristics

(T<sub>A</sub> =  $-40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T <sub>cy</sub>	Main system clock (f <sub>MAIN</sub> ) operation	HS (high-speed main) mode	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V <sub>DD</sub> < 2.7 V	0.0625		1	μs
		Subsystem clock (f <sub>SUB</sub> ) operation		2.4 V ≤ V <sub>DD</sub> ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V <sub>DD</sub> < 2.7 V	0.0625		1	μs
External system clock frequency	f <sub>EX</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V <sub>DD</sub> < 2.7 V			1.0		16.0	MHz
	f <sub>EXS</sub>				32		35	kHz
External system clock input high-level width, low-level width	t <sub>EXH</sub> , t <sub>EXL</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V			24			ns
		2.4 V ≤ V <sub>DD</sub> < 2.7 V			30			ns
	t <sub>EXHS</sub> , t <sub>EXLS</sub>				13.7			μs
TI00 to TI07, TI10 to TI17 input high-level width, low-level width	t <sub>TIH</sub> , t <sub>TIL</sub>				1/f <sub>MCK</sub> +10			ns <sup>Note</sup>
TO00 to TO07, TO10 to TO17 output frequency	f <sub>TO</sub>	HS (high-speed main) mode	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V			16	MHz	
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V			8	MHz	
			2.4 V ≤ EV <sub>DD0</sub> < 2.7 V			4	MHz	
PCLBUZ0, PCLBUZ1 output frequency	f <sub>PCL</sub>	HS (high-speed main) mode	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V			16	MHz	
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V			8	MHz	
			2.4 V ≤ EV <sub>DD0</sub> < 2.7 V			4	MHz	
Interrupt input high-level width, low-level width	t <sub>INTH</sub> , t <sub>INTL</sub>	INTP0	2.4 V ≤ V <sub>DD</sub> ≤ 5.5 V	1			μs	
		INTP1 to INTP11	2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	1			μs	
Key interrupt input low-level width	t <sub>KR</sub>	KR0 to KR7	2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	250			ns	
RESET low-level width	t <sub>RSL</sub>				10			μs

**Note** The following conditions are required for low voltage interface when  $\text{EV}_{\text{DD}0} < \text{V}_{\text{DD}}$   
 $2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 2.7\text{ V}$  : MIN. 125 ns

**Remark** f<sub>MCK</sub>: Timer array unit operation clock frequency  
 (Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn).  
 m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7))



**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp↓) <sup>Note</sup>	$t_{SIK1}$	$4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$	88		ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	88		ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$	220		ns
Slp hold time (from SCKp↓) <sup>Note</sup>	$t_{KSI1}$	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$	38		ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	38		ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$	38		ns
Delay time from SCKp↑ to SOp output <sup>Note</sup>	$t_{KSO1}$	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$		50	ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$		50	ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$		50	ns

**Note** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output ( $V_{DD}$  tolerance (for the 20- to 52-pin products)/ $EV_{DD}$  tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

### 3.6 Analog Characteristics

#### 3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = $AV_{REFP}$ Reference voltage (-) = $AV_{REFM}$	Reference voltage (+) = $V_{DD}$ Reference voltage (-) = $V_{SS}$	Reference voltage (+) = $V_{BGR}$ Reference voltage (-) = $AV_{REFM}$
ANI0 to ANI14	Refer to 3.6.1 (1).	Refer to 3.6.1 (3).	Refer to 3.6.1 (4).
ANI16 to ANI26	Refer to 3.6.1 (2).		
Internal reference voltage Temperature sensor output voltage	Refer to 3.6.1 (1).		—

(1) When reference voltage (+) =  $AV_{REFP}/ANI0$  ( $ADREFP1 = 0$ ,  $ADREFP0 = 1$ ), reference voltage (-) =  $AV_{REFM}/ANI1$  ( $ADREFM = 1$ ), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , Reference voltage (+) =  $AV_{REFP}$ , Reference voltage (-) =  $AV_{REFM} = 0\text{ V}$ )

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error <sup>Note 1</sup>	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ <sup>Note 3</sup>	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		1.2	$\pm 3.5$	LSB
Conversion time	$t_{CONV}$	10-bit resolution Target pin: ANI2 to ANI14	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	$\mu\text{s}$
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	$\mu\text{s}$
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	$\mu\text{s}$
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	$\mu\text{s}$
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	$\mu\text{s}$
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	$\mu\text{s}$
Zero-scale error <sup>Notes 1, 2</sup>	$E_{ZS}$	10-bit resolution $AV_{REFP} = V_{DD}$ <sup>Note 3</sup>	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			$\pm 0.25$	%FSR
Full-scale error <sup>Notes 1, 2</sup>	$E_{FS}$	10-bit resolution $AV_{REFP} = V_{DD}$ <sup>Note 3</sup>	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			$\pm 0.25$	%FSR
Integral linearity error <sup>Note 1</sup>	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ <sup>Note 3</sup>	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			$\pm 2.5$	LSB
Differential linearity error <sup>Note 1</sup>	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ <sup>Note 3</sup>	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			$\pm 1.5$	LSB
Analog input voltage	$V_{AIN}$	ANI2 to ANI14		0		$AV_{REFP}$	V
		Internal reference voltage output ( $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , HS (high-speed main) mode)		$V_{BGR}$ <sup>Note 4</sup>			V
		Temperature sensor output voltage ( $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , HS (high-speed main) mode)		$V_{TMPS25}$ <sup>Note 4</sup>			V

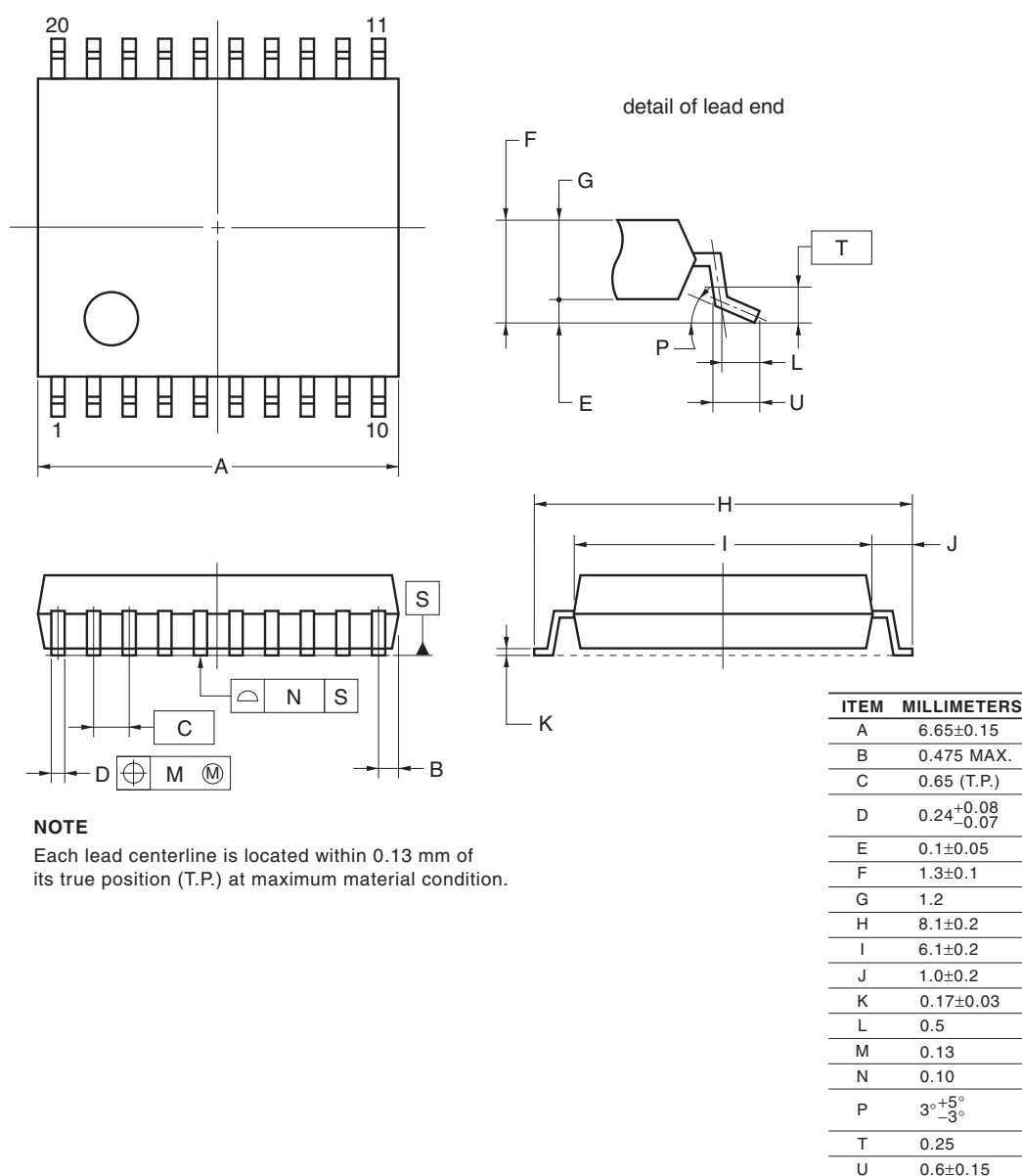
(Notes are listed on the next page.)

## 4. PACKAGE DRAWINGS

### 4.1 20-pin Products

R5F1006AASP, R5F1006CASP, R5F1006DASP, R5F1006EASP  
 R5F1016AASP, R5F1016CASP, R5F1016DASP, R5F1016EASP  
 R5F1006ADSP, R5F1006CDSP, R5F1006DDSP, R5F1006EDSP  
 R5F1016ADSP, R5F1016CDSP, R5F1016DDSP, R5F1016EDSP  
 R5F1006AGSP, R5F1006CGSP, R5F1006DGSP, R5F1006EGSP

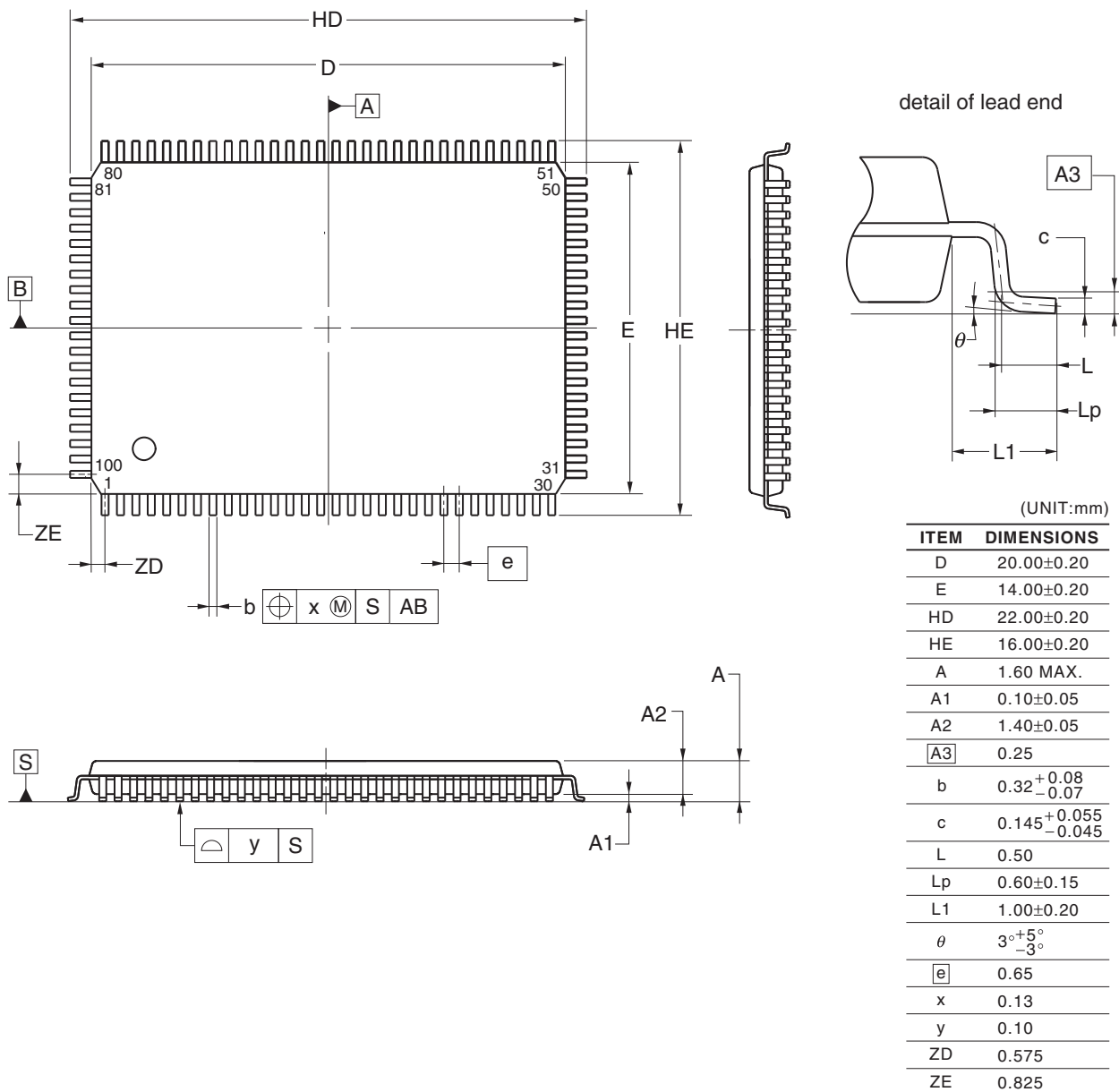
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-0300-0.65	PLSP0020JC-A	S20MC-65-5A4-3	0.12



©2012 Renesas Electronics Corporation. All rights reserved.

R5F100PFAFA, R5F100PGAFA, R5F100PHAFA, R5F100PJAF, R5F100PKAFA, R5F100PLAFA  
 R5F101PFAFA, R5F101PGAFA, R5F101PHAFA, R5F101PJAF, R5F101PKAFA, R5F101PLAFA  
 R5F100PFDFA, R5F100PGDFA, R5F100PHDFA, R5F100PJDFA, R5F100PKDFA, R5F100PLDFA  
 R5F101PFDFA, R5F101PGDFA, R5F101PHDFA, R5F101PJDFA, R5F101PKDFA, R5F101PLDFA  
 R5F100PFGFA, R5F100PGGFA, R5F100PHGFA, R5F100PJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP100-14x20-0.65	PLQP0100JC-A	P100GF-65-GBN-1	0.92



©2012 Renesas Electronics Corporation. All rights reserved.

## Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
  2. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
  3. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
  4. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics product.
  5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.  
"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.  
"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; and safety equipment etc.  
Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (nuclear reactor control systems, military equipment etc.). You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application for which it is not intended. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
  6. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
  7. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or systems manufactured by you.
  8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
  9. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You should not use Renesas Electronics products or technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. When exporting the Renesas Electronics products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations.
  10. It is the responsibility of the buyer or distributor of Renesas Electronics products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the contents and conditions set forth in this document, Renesas Electronics assumes no responsibility for any losses incurred by you or third parties as a result of unauthorized use of Renesas Electronics products.
  11. This document may not be reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
  12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.
- (Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.
- (Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.



### SALES OFFICES

### Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "http://www.renesas.com/" for the latest and detailed information.

#### California Eastern Laboratories, Inc.

4590 Patrick Henry Drive, Santa Clara, California 95054-1817, U.S.A.  
Tel: +1-408-919-2500, Fax: +1-408-988-0279

#### Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K  
Tel: +44-1628-585-100, Fax: +44-1628-585-900

#### Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

#### Renesas Electronics (China) Co., Ltd.

Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

#### Renesas Electronics (Shanghai) Co., Ltd.

Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333  
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

#### Renesas Electronics Hong Kong Limited

Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2265-6688, Fax: +852 2886-9022

#### Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan  
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

#### Renesas Electronics Singapore Pte. Ltd.

80 Bendemeer Road, Unit #06-02, Hyflux Innovation Centre, Singapore 339949  
Tel: +65-6213-0200, Fax: +65-6213-0300

#### Renesas Electronics Malaysia Sdn.Bhd.

Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

#### Renesas Electronics India Pvt. Ltd.

No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India  
Tel: +91-80-67208700, Fax: +91-80-67208777

#### Renesas Electronics Korea Co., Ltd.

12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea  
Tel: +82-2-558-3737, Fax: +82-2-558-5141