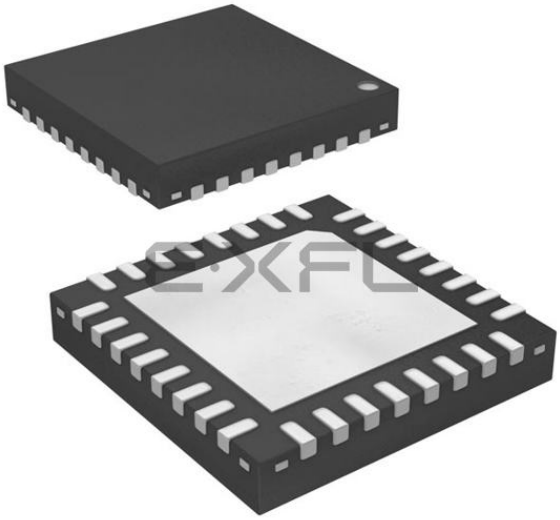
Renesas Electronics America Inc - R5F100BFGNA#U0 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	32-HWQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100bfgna-u0

Table 1-1. List of Ordering Part Numbers

(1/12)

Pin count	Package	Data flash	Fields of Application [Note]	Ordering Part Number
20 pins	20-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	Mounted	A	R5F1006AASP#V0, R5F1006CASP#V0, R5F1006DASP#V0, R5F1006EASP#V0 R5F1006AASP#X0, R5F1006CASP#X0, R5F1006DASP#X0, R5F1006EASP#X0
			D	R5F1006ADSP#V0, R5F1006CDSP#V0, R5F1006DDSP#V0, R5F1006EDSP#V0 R5F1006ADSP#X0, R5F1006CDSP#X0, R5F1006DDSP#X0, R5F1006EDSP#X0
			G	R5F1006AGSP#V0, R5F1006CGSP#V0, R5F1006DGSP#V0, R5F1006EGSP#V0 R5F1006AGSP#X0, R5F1006CGSP#X0, R5F1006DGSP#X0, R5F1006EGSP#X0
		Not mounted	A	R5F1016AASP#V0, R5F1016CASP#V0, R5F1016DASP#V0, R5F1016EASP#V0 R5F1016AASP#X0, R5F1016CASP#X0, R5F1016DASP#X0, R5F1016EASP#X0
			D	R5F1016ADSP#V0, R5F1016CDSP#V0, R5F1016DDSP#V0, R5F1016EDSP#V0 R5F1016ADSP#X0, R5F1016CDSP#X0, R5F1016DDSP#X0, R5F1016EDSP#X0
24 pins	24-pin plastic HWQFN (4 × 4mm, 0.5 mm pitch)	Mounted	A	R5F1007AANA#U0, R5F1007CANA#U0, R5F1007DANA#U0, R5F1007EANA#U0 R5F1007AANA#W0, R5F1007CANA#W0, R5F1007DANA#W0, R5F1007EANA#W0
			D	R5F1007ADNA#U0, R5F1007CDNA#U0, R5F1007DDNA#U0, R5F1007EDNA#U0 R5F1007ADNA#W0, R5F1007CDNA#W0, R5F1007DDNA#W0, R5F1007EDNA#W0
			G	R5F1007AGNA#U0, R5F1007CGNA#U0, R5F1007DGNA#U0, R5F1007EGNA#U0 R5F1007AGNA#W0, R5F1007CGNA#W0, R5F1007DGNA#W0, R5F1007EGNA#W0
		Not mounted	A	R5F1017AANA#U0, R5F1017CANA#U0, R5F1017DANA#U0, R5F1017EANA#U0 R5F1017AANA#W0, R5F1017CANA#W0, R5F1017DANA#W0, R5F1017EANA#W0
			D	R5F1017ADNA#U0, R5F1017CDNA#U0, R5F1017DDNA#U0, R5F1017EDNA#U0 R5F1017ADNA#W0, R5F1017CDNA#W0, R5F1017DDNA#W0, R5F1017EDNA#W0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

[80-pin, 100-pin, 128-pin products]

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		80-pin		100-pin		128-pin	
		R5F100Mx	R5F101Mx	R5F100Px	R5F101Px	R5F100Sx	R5F101Sx
Code flash memory (KB)		96 to 512		96 to 512		192 to 512	
Data flash memory (KB)		8	–	8	–	8	–
RAM (KB)		8 to 32 Note 1		8 to 32 Note 1		16 to 32 Note 1	
Address space		1 MB					
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)					
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)					
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz					
Low-speed on-chip oscillator		15 kHz (TYP.)					
General-purpose register		(8-bit register × 8) × 4 banks					
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)					
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)					
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)					
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.					
I/O port	Total	74		92		120	
	CMOS I/O	64 (N-ch O.D. I/O [EV_{DD} withstand voltage]: 21)		82 (N-ch O.D. I/O [EV_{DD} withstand voltage]: 24)		110 (N-ch O.D. I/O [EV_{DD} withstand voltage]: 25)	
	CMOS input	5		5		5	
	CMOS output	1		1		1	
	N-ch O.D. I/O (withstand voltage: 6 V)	4		4		4	
Timer	16-bit timer	12 channels		12 channels		16 channels	
	Watchdog timer	1 channel		1 channel		1 channel	
	Real-time clock (RTC)	1 channel		1 channel		1 channel	
	12-bit interval timer (IT)	1 channel		1 channel		1 channel	
	Timer output	12 channels (PWM outputs: 10 Note 2)		12 channels (PWM outputs: 10 Note 2)		16 channels (PWM outputs: 14 Note 2)	
	RTC output	1 channel • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)					

Notes 1. The flash library uses RAM in self-programming and rewriting of the data flash memory.

The target products and start address of the RAM areas used by the flash library are shown below.

R5F100xJ, R5F101xJ (x = M, P): Start address FAF00H

R5F100xL, R5F101xL (x = M, P, S): Start address F7F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	−70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	−100	mA
	I_{OH2}	Per pin	P20 to P27, P150 to P156	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
	I_{OL2}	Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147				20.0 Note 2	mA
		Per pin for P60 to P63				15.0 Note 2	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			70.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			15.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			9.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			80.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			35.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			20.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			10.0	mA
		Total of all pins (When duty ≤ 70% Note 3)				150.0	mA
	I_{OL2}	Per pin for P20 to P27, P150 to P156				0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	1.6 V ≤ V_{DD} ≤ 5.5 V			5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0}, EV_{SS1} and V_{SS} pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current . However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V @1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

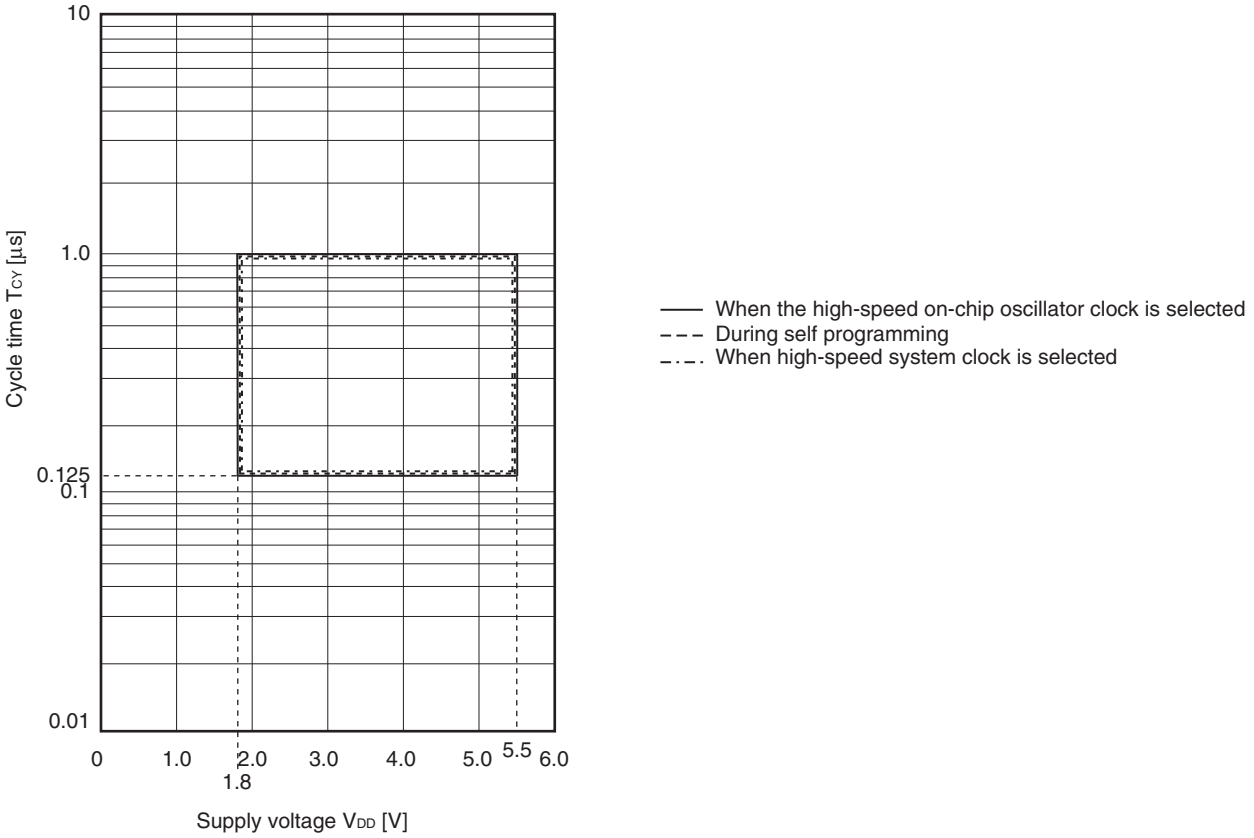
Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

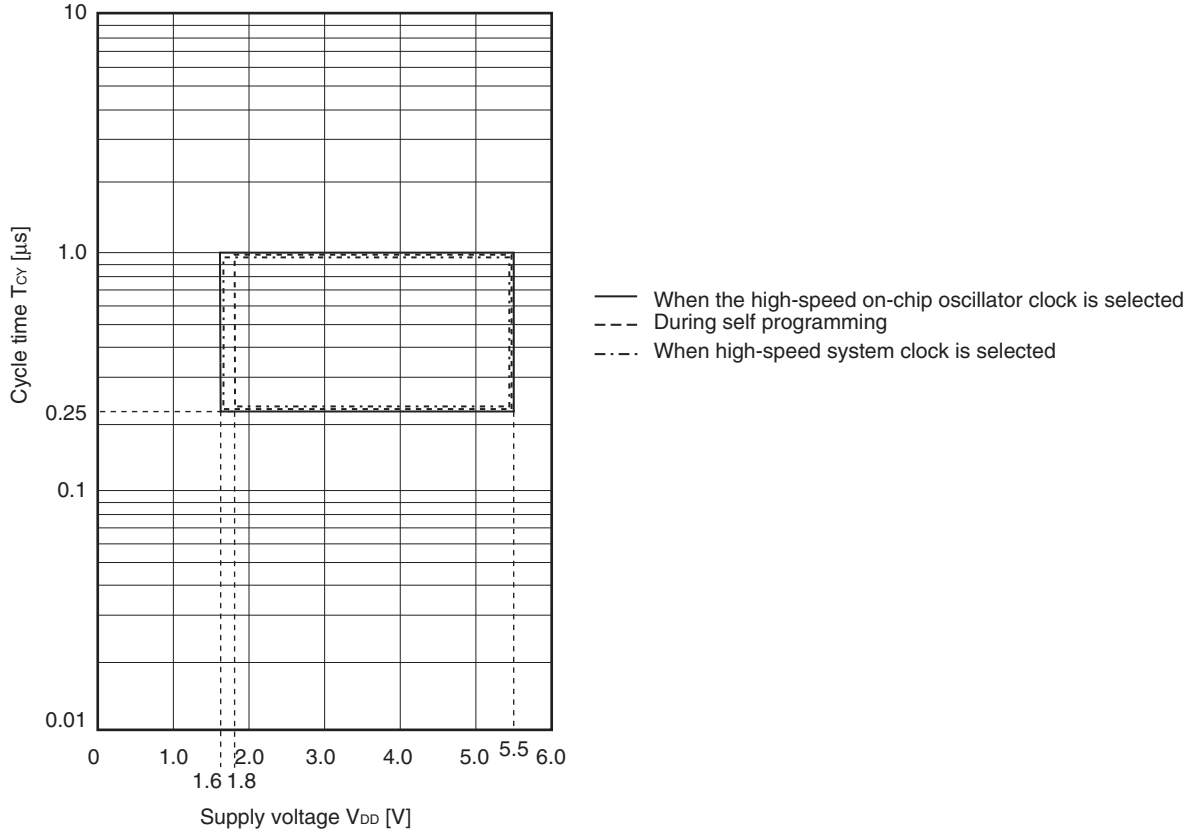
3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

T_{CY} vs V_{DD} (LS (low-speed main) mode)



T_{CY} vs V_{DD} (LV (low-voltage main) mode)



(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = –40 to +85°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V	62.5		250		500		ns
			2.7 V ≤ EV_{DD0} ≤ 5.5 V	83.3		250		500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		$t_{KCY1}/2$ – 7		$t_{KCY1}/2$ – 50		$t_{KCY1}/2$ – 50		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		$t_{KCY1}/2$ – 10		$t_{KCY1}/2$ – 50		$t_{KCY1}/2$ – 50		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		23		110		110		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		33		110		110		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		10		10		10		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 20 pF Note 4			10		10		10	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. This value is valid only when CSI00's peripheral I/O redirect function is not used.

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V	125		500		1000		ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V	250		500		1000		ns
			1.8 V ≤ EV_{DD0} ≤ 5.5 V	500		500		1000		ns
			1.7 V ≤ EV_{DD0} ≤ 5.5 V	1000		1000		1000		ns
			1.6 V ≤ EV_{DD0} ≤ 5.5 V	—		1000		1000		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 – 12		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 – 18		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 – 38		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		1.7 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 – 100		t_{KCY1}/2 – 100		t_{KCY1}/2 – 100		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		t_{KCY1}/2 – 100		t_{KCY1}/2 – 100		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		44		110		110		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		44		110		110		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		75		110		110		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		110		110		110		ns
		1.7 V ≤ EV_{DD0} ≤ 5.5 V		220		220		220		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		220		220		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}	1.7 V ≤ EV_{DD0} ≤ 5.5 V		19		19		19		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		19		19		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	1.7 V ≤ EV_{DD0} ≤ 5.5 V C = 30 pF Note 4			25		25		25	ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V C = 30 pF Note 4			—		25		25	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

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4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2)

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK}+20		1/f_{MCK}+30		1/f_{MCK}+30		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK}+30		1/f_{MCK}+30		1/f_{MCK}+30		ns
		1.7 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK}+40		1/f_{MCK}+40		1/f_{MCK}+40		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		1/f_{MCK}+40		1/f_{MCK}+40		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}	1.8 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK}+31		1/f_{MCK}+31		1/f_{MCK}+31		ns
		1.7 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK}+250		1/f_{MCK}+250		1/f_{MCK}+250		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		1/f_{MCK}+250		1/f_{MCK}+250		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	2.7 V ≤ EV_{DD0} ≤ 5.5 V		2/f_{MCK}+44		2/f_{MCK}+110		2/f_{MCK}+110	ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V		2/f_{MCK}+75		2/f_{MCK}+110		2/f_{MCK}+110	ns
			1.8 V ≤ EV_{DD0} ≤ 5.5 V		2/f_{MCK}+110		2/f_{MCK}+110		2/f_{MCK}+110	ns
			1.7 V ≤ EV_{DD0} ≤ 5.5 V		2/f_{MCK}+220		2/f_{MCK}+220		2/f_{MCK}+220	ns
			1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		2/f_{MCK}+220		2/f_{MCK}+220	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SOp output lines.

5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)

2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		1150		1150		ns
			2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500		1150		1150		ns
			1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note], C_b = 30 pF, R_b = 5.5 kΩ	1150		1150		1150		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 75		t_{KCY1}/2 – 75		t_{KCY1}/2 – 75		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 170		t_{KCY1}/2 – 170		t_{KCY1}/2 – 170		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note], C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 – 458		t_{KCY1}/2 – 458		t_{KCY1}/2 – 458		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 12		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 18		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note], C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns

Note Use it with EV_{DD0} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed two pages after the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ	110		110		110		ns
SIp hold time (from SCKp↓) Note 1	t_{KSI1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output Note 1	t_{KSO1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ		25		25		25	ns

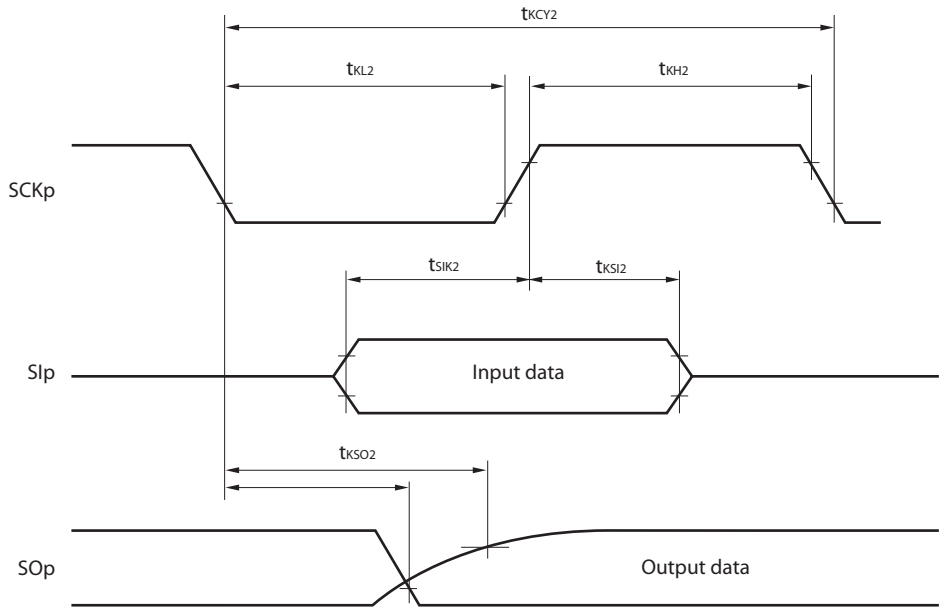
Notes **1.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. Use it with EV_{DD0} ≥ V_b.

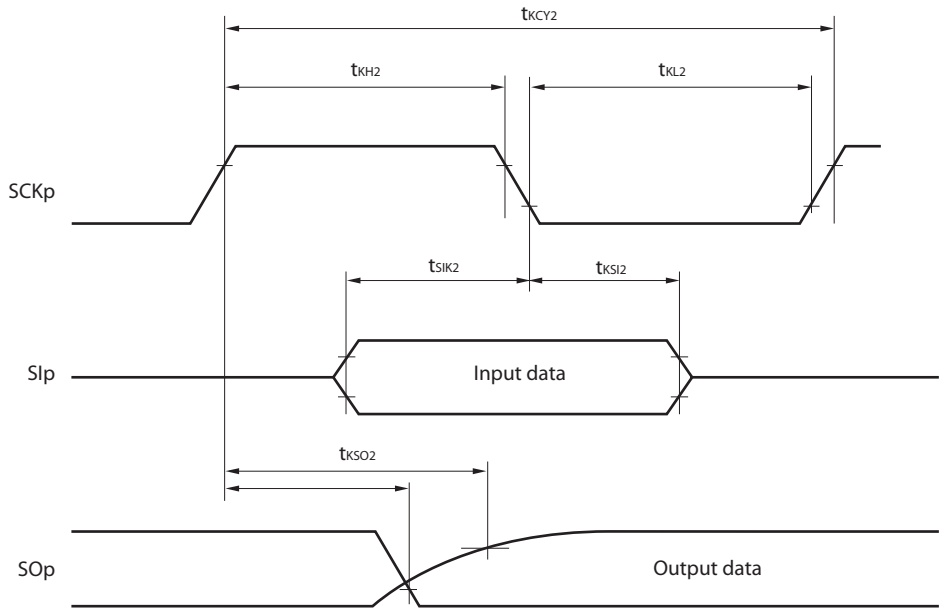
Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,
n: Channel number (mn = 00, 01, 02, 10, 12. 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

LVD Detection Voltage of Interrupt & Reset Mode

(T_A = –40 to +85°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDA0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 0, falling reset voltage			1.60	1.63	1.66	V
	V_{LVDA1}	LVIS1, LVIS0 = 1, 0		Rising release reset voltage	1.74	1.77	1.81	V
				Falling interrupt voltage	1.70	1.73	1.77	V
	V_{LVDA2}	LVIS1, LVIS0 = 0, 1		Rising release reset voltage	1.84	1.88	1.91	V
				Falling interrupt voltage	1.80	1.84	1.87	V
	V_{LVDA3}	LVIS1, LVIS0 = 0, 0		Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDB0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 1, falling reset voltage			1.80	1.84	1.87	V
	V_{LVDB1}	LVIS1, LVIS0 = 1, 0		Rising release reset voltage	1.94	1.98	2.02	V
				Falling interrupt voltage	1.90	1.94	1.98	V
	V_{LVDB2}	LVIS1, LVIS0 = 0, 1		Rising release reset voltage	2.05	2.09	2.13	V
				Falling interrupt voltage	2.00	2.04	2.08	V
	V_{LVDB3}	LVIS1, LVIS0 = 0, 0		Rising release reset voltage	3.07	3.13	3.19	V
				Falling interrupt voltage	3.00	3.06	3.12	V
	V_{LVDC0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0, falling reset voltage			2.40	2.45	2.50	V
	V_{LVDC1}	LVIS1, LVIS0 = 1, 0		Rising release reset voltage	2.56	2.61	2.66	V
				Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVDC2}	LVIS1, LVIS0 = 0, 1		Rising release reset voltage	2.66	2.71	2.76	V
				Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVDC3}	LVIS1, LVIS0 = 0, 0		Rising release reset voltage	3.68	3.75	3.82	V
				Falling interrupt voltage	3.60	3.67	3.74	V
	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage			2.70	2.75	2.81	V
	V_{LVDD1}	LVIS1, LVIS0 = 1, 0		Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDD2}	LVIS1, LVIS0 = 0, 1		Rising release reset voltage	2.96	3.02	3.08	V
				Falling interrupt voltage	2.90	2.96	3.02	V
	V_{LVDD3}	LVIS1, LVIS0 = 0, 0		Rising release reset voltage	3.98	4.06	4.14	V
				Falling interrupt voltage	3.90	3.98	4.06	V

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f_{IH} = 32 MHz Note 4	V_{DD} = 5.0 V		0.54	2.90	mA
					V_{DD} = 3.0 V		0.54	2.90	mA
				f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.44	2.30	mA
					V_{DD} = 3.0 V		0.44	2.30	mA
				f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.40	1.70	mA
					V_{DD} = 3.0 V		0.40	1.70	mA
			HS (high-speed main) mode Note 7	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.28	1.90	mA
					Resonator connection		0.45	2.00	mA
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.28	1.90	mA
					Resonator connection		0.45	2.00	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.19	1.02	mA
					Resonator connection		0.26	1.10	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.19	1.02	mA
					Resonator connection		0.26	1.10	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5 T_A = –40°C	Square wave input		0.25	0.57	μA
					Resonator connection		0.44	0.76	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +25°C	Square wave input		0.30	0.57	μA
					Resonator connection		0.49	0.76	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +50°C	Square wave input		0.37	1.17	μA
					Resonator connection		0.56	1.36	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +70°C	Square wave input		0.53	1.97	μA
					Resonator connection		0.72	2.16	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +85°C	Square wave input		0.82	3.37	μA
					Resonator connection		1.01	3.56	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +105°C	Square wave input		3.01	15.37	μA
					Resonator connection		3.20	15.56	μA
	I_{DD3} Note 6	STOP mode Note 8	T_A = –40°C				0.18	0.50	μA
			T_A = +25°C				0.23	0.50	μA
			T_A = +50°C				0.30	1.10	μA
			T_A = +70°C				0.46	1.90	μA
			T_A = +85°C				0.75	3.30	μA
			T_A = +105°C				2.94	15.30	μA

(**Notes** and **Remarks** are listed on the next page.)

3.4 AC Characteristics

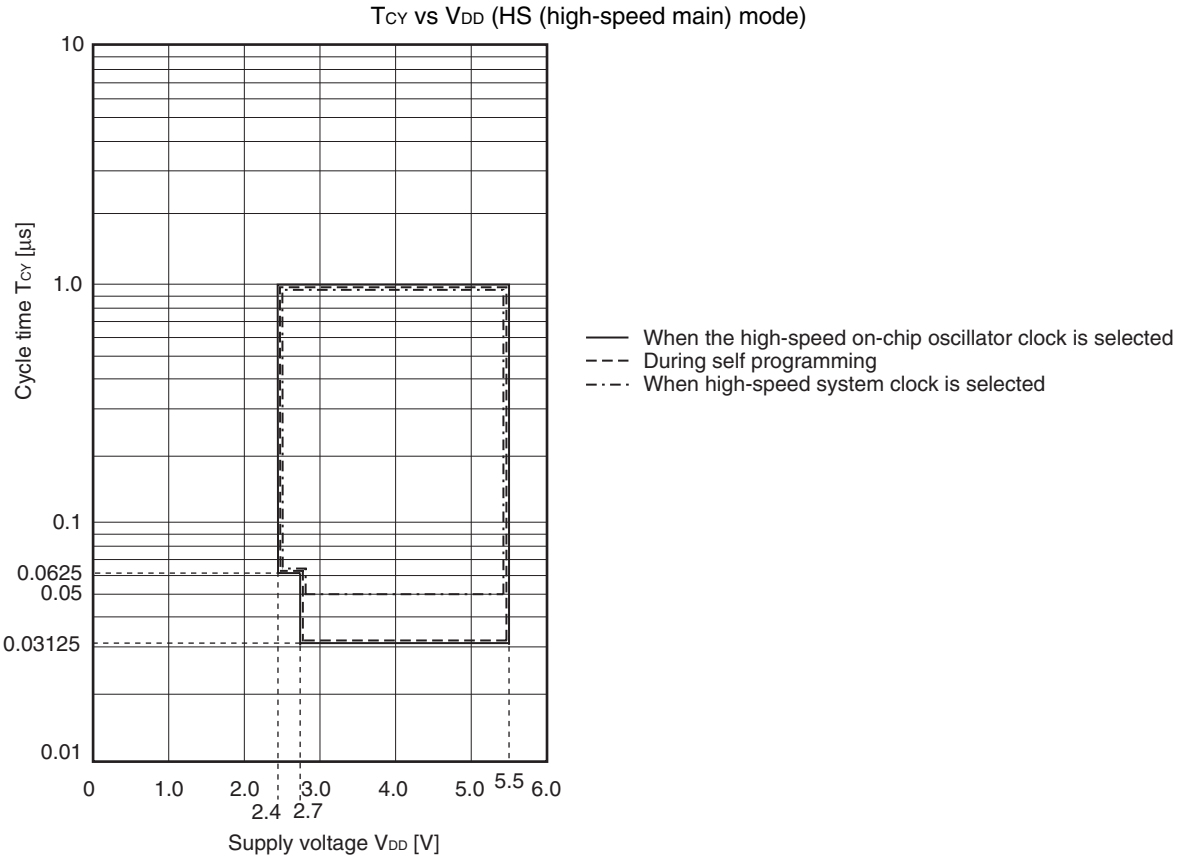
(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
		Subsystem clock (f_{SUB}) operation		2.4 V ≤ V_{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
External system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V			1.0		16.0	MHz
	f_{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V_{DD} < 2.7 V			30			ns
	t_{EXHS}, t_{EXLS}				13.7			μs
TI00 to TI07, TI10 to TI17 input high-level width, low-level width	t_{TIH}, t_{TIL}				1/f_{MCK}+10			ns[Note]
TO00 to TO07, TO10 to TO17 output frequency	f_{TO}	HS (high-speed main) mode		4.0 V ≤ EV_{DD0} ≤ 5.5 V			16	MHz
				2.7 V ≤ EV_{DD0} < 4.0 V			8	MHz
				2.4 V ≤ EV_{DD0} < 2.7 V			4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode		4.0 V ≤ EV_{DD0} ≤ 5.5 V			16	MHz
				2.7 V ≤ EV_{DD0} < 4.0 V			8	MHz
				2.4 V ≤ EV_{DD0} < 2.7 V			4	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0		2.4 V ≤ V_{DD} ≤ 5.5 V	1			μs
		INTP1 to INTP11		2.4 V ≤ EV_{DD0} ≤ 5.5 V	1			μs
Key interrupt input low-level width	t_{KR}	KR0 to KR7		2.4 V ≤ EV_{DD0} ≤ 5.5 V	250			ns
$\overline{RESET}$ low-level width	t_{RSL}				10			μs

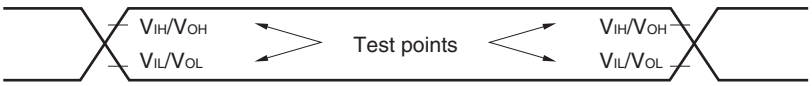
Note The following conditions are required for low voltage interface when EV_{DD0} < V_{DD}
2.4V ≤ EV_{DD0} < 2.7 V : MIN. 125 ns

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn).
m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7))

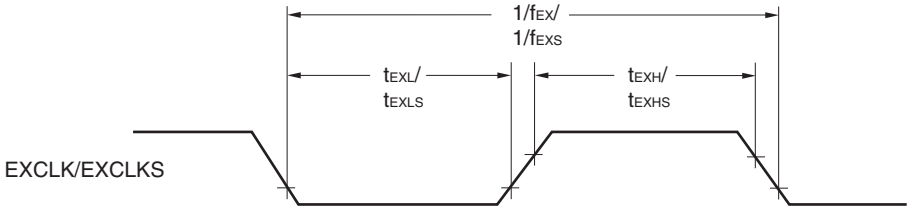
Minimum Instruction Execution Time during Main System Clock Operation



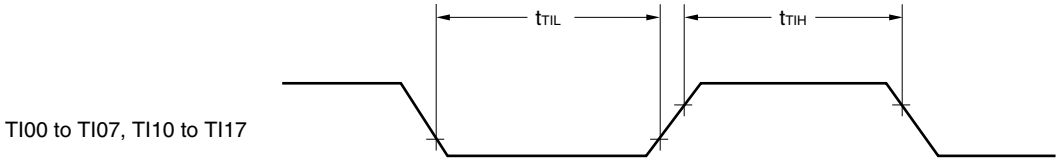
AC Timing Test Points

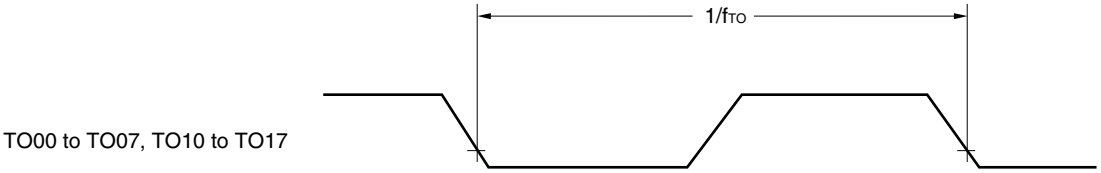


External System Clock Timing

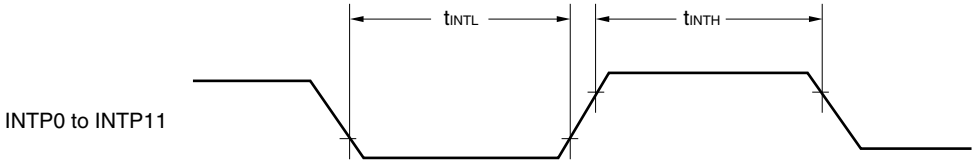


TI/TO Timing

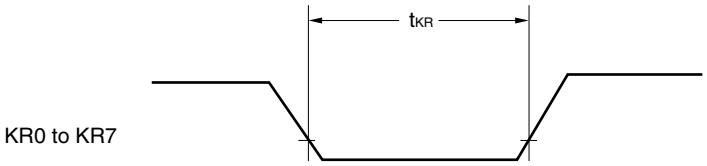




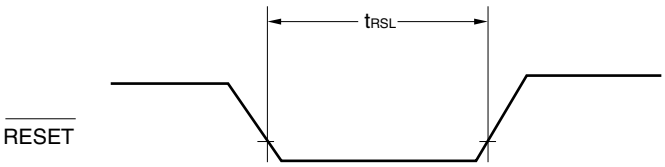
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	24 MHz < f_{MCK}	28/f_{MCK}		ns
			20 MHz < f_{MCK} ≤ 24 MHz	24/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 20 MHz	20/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	24 MHz < f_{MCK}	40/f_{MCK}		ns
			20 MHz < f_{MCK} ≤ 24 MHz	32/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	28/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	24/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	24 MHz < f_{MCK}	96/f_{MCK}		ns
			20 MHz < f_{MCK} ≤ 24 MHz	72/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	64/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	52/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	32/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	20/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 – 24		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 – 36		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		t_{KCY2}/2 – 100		ns
SIp setup time (to SCKp↑) Note2	t_{SIK2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 40		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 40		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		1/f_{MCK} + 60		ns
SIp hold time (from SCKp↑) Note 3	t_{KSI2}			1/f_{MCK} + 62		ns
Delay time from SCKp↓ to SOp output Note 4	t_{KSO2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			2/f_{MCK} + 240	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 428	ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ			2/f_{MCK} + 1146	ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

3.6.5 Power supply voltage rising slope characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 3.4 AC Characteristics.

3.7 RAM Data Retention Characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.