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### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

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Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-WFLGA
Supplier Device Package	36-WFLGA (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100cdala-u0

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

### Table 1-1. List of Ordering Part Numbers

-				(1/12)
Pin	Package	Data	Fields of	Ordering Part Number
count		flash	Application Note	
20 pins	20-pin plastic LSSOP	Mounted	А	R5F1006AASP#V0, R5F1006CASP#V0, R5F1006DASP#V0,
	(7.62 mm (300), 0.65			R5F1006EASP#V0
	mm pitch)			R5F1006AASP#X0, R5F1006CASP#X0, R5F1006DASP#X0,
				R5F1006EASP#X0
			D	R5F1006ADSP#V0, R5F1006CDSP#V0, R5F1006DDSP#V0,
				R5F1006EDSP#V0
				R5F1006ADSP#X0, R5F1006CDSP#X0, R5F1006DDSP#X0,
				R5F1006EDSP#X0
			G	R5F1006AGSP#V0, R5F1006CGSP#V0, R5F1006DGSP#V0,
				R5F1006EGSP#V0
				R5F1006AGSP#X0, R5F1006CGSP#X0, R5F1006DGSP#X0,
				R5F1006EGSP#X0
		Not	А	R5F1016AASP#V0, R5F1016CASP#V0, R5F1016DASP#V0,
		mounted		R5F1016EASP#V0
				R5F1016AASP#X0, R5F1016CASP#X0, R5F1016DASP#X0,
				R5F1016EASP#X0
			D	R5F1016ADSP#V0, R5F1016CDSP#V0, R5F1016DDSP#V0,
				R5F1016EDSP#V0
				R5F1016ADSP#X0, R5F1016CDSP#X0, R5F1016DDSP#X0,
				R5F1016EDSP#X0
24 pins	24-pin plastic	Mounted	А	R5F1007AANA#U0, R5F1007CANA#U0, R5F1007DANA#U0,
	HWQFN (4 $\times$ 4mm,			R5F1007EANA#U0
	0.5 mm pitch)			R5F1007AANA#W0, R5F1007CANA#W0, R5F1007DANA#W0,
				R5F1007EANA#W0
			D	R5F1007ADNA#U0, R5F1007CDNA#U0, R5F1007DDNA#U0,
				R5F1007EDNA#U0
				R5F1007ADNA#W0, R5F1007CDNA#W0, R5F1007DDNA#W0,
				R5F1007EDNA#W0
			G	R5F1007AGNA#U0, R5F1007CGNA#U0, R5F1007DGNA#U0,
				R5F1007EGNA#U0
				R5F1007AGNA#W0, R5F1007CGNA#W0, R5F1007DGNA#W0,
				R5F1007EGNA#W0
		Not	А	R5F1017AANA#U0, R5F1017CANA#U0, R5F1017DANA#U0,
		mounted		R5F1017EANA#U0
				R5F1017AANA#W0, R5F1017CANA#W0, R5F1017DANA#W0,
				R5F1017EANA#W0
			D	R5F1017ADNA#U0, R5F1017CDNA#U0, R5F1017DDNA#U0,
				R5F1017EDNA#U0
				R5F1017ADNA#W0, R5F1017CDNA#W0, R5F1017DDNA#W0,
				R5F1017EDNA#W0

Note For the fields of application, refer to Figure 1-1 Part Number, Memory Size, and Package of RL78/G13.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.



# 2. ELECTRICAL SPECIFICATIONS (TA = -40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications  $T_A = -40$  to  $+85^{\circ}C$ 

R5F100xxAxx, R5F101xxAxx

- D: Industrial applications  $T_A = -40$  to  $+85^{\circ}C$ R5F100xxDxx, R5F101xxDxx
- G: Industrial applications when  $T_A = -40$  to  $+105^{\circ}$ C products is used in the range of  $T_A = -40$  to  $+85^{\circ}$ C

R5F100xxGxx

- Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
  - 2. With products not provided with an EV<sub>DD0</sub>, EV<sub>DD1</sub>, EV<sub>SS0</sub>, or EV<sub>SS1</sub> pin, replace EV<sub>DD0</sub> and EV<sub>DD1</sub> with V<sub>DD</sub>, or replace EV<sub>SS0</sub> and EV<sub>SS1</sub> with V<sub>SS</sub>.
  - 3. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions for each product.



- **Notes 1.** Total current flowing into Vbb, EVbbb, and EVbb1, including the input leakage current flowing when the level of the input pin is fixed to Vbb, EVbb0, and EVbb1, or Vss, EVsso, and EVss1. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  - 2. When high-speed on-chip oscillator and subsystem clock are stopped.
  - 3. When high-speed system clock and subsystem clock are stopped.
  - 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  - **5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
    - HS (high-speed main) mode: 2.7 V  $\leq$  V\_{DD}  $\leq$  5.5 V@1 MHz to 32 MHz
      - 2.4 V  $\leq$  V<sub>DD</sub>  $\leq$  5.5 V@1 MHz to 16 MHz
    - LS (low-speed main) mode:  $~~1.8~V \leq V_{\text{DD}} \leq 5.5~V @\,1~\text{MHz}$  to 8 MHz
    - LV (low-voltage main) mode: 1.6 V  $\leq$  V\_DD  $\leq$  5.5 V@1 MHz to 4 MHz
- Remarks 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  - 2. fin: High-speed on-chip oscillator clock frequency
  - **3.** fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
  - 4. Except subsystem clock operation, temperature condition of the TYP. value is  $T_A = 25^{\circ}C$





TCY vs VDD (LS (low-speed main) mode)



**Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),

g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)

2. fmck: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (1/2)  $(T_A = -40 \text{ to } +85^{\circ}\text{C}, 1.6 \text{ V} \le \text{EV}_{\text{DD}} = \text{EV}_{\text{DD}} \le 5.5 \text{ V}, \text{ Vss} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0 \text{ V})$ 

Parameter	Symbol	Conditions		HS (hig main)	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode	
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	1
SCKp cycle time	tkCY2	$4.0~V \leq EV_{\text{DD0}} \leq 5.5$	20 MHz < fмск	8/fмск				_		ns
Note 5		V	fмск ≤ 20 MHz	6/fмск		6/fмск		6/fмск		ns
		$2.7~V \leq EV_{\text{DD0}} \leq 5.5$	16 MHz < fмск	8/fмск				_		ns
		V	fмск ≤ 16 MHz	6/fмск		6/fмск		6/fмск		ns
		$2.4~V \leq EV_{DD0} \leq 5.5~V$		6/fмск and 500		6/fмск and 500		6/fмск and 500		ns
		$1.8~V \leq EV_{\text{DD0}} \leq 5.5~V$		6/fмск and 750		6/fмск and 750		6/fмск and 750		ns
		$1.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V}$		6/fмск and 1500		6/fмск and 1500		6/fмск and 1500		ns
		$1.6 \text{ V} \leq EV_{\text{DD0}} \leq 5.5$	V	_		6/fмск and 1500		6/fмск and 1500		ns
SCKp high-/low- level width	tкн2, tкL2	$4.0~V \leq EV_{\text{DD0}} \leq 5.5~V$		tксү2/2 – 7		tксү2/2 - 7		tксү2/2 - 7		ns
		$2.7~V \leq EV_{\text{DD0}} \leq 5.5~V$		tксү2/2 – 8		tксү2/2 - 8		tксү2/2 - 8		ns
		$1.8~V \leq EV_{DD0} \leq 5.5~V$		tксү2/2 – 18		tксү2/2 – 18		tксү2/2 – 18		ns
		$1.7~V \leq EV_{\text{DD0}} \leq 5.5~V$		tксү2/2 – 66		tксү2/2 - 66		tксү2/2 - 66		ns
		$1.6 V \le EV_{DD0} \le 5.5$	V			tксү2/2 - 66		tксү2/2 - 66		ns

(Notes, Caution, and Remarks are listed on the next page.)



## Simplified I<sup>2</sup>C mode mode connection diagram (during communication at same potential)



### Simplified I<sup>2</sup>C mode serial transfer timing (during communication at same potential)



- **Remarks 1.** R<sub>b</sub>[Ω]:Communication line (SDAr) pull-up resistance, C<sub>b</sub>[F]: Communication line (SDAr, SCLr) load capacitance
  - r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14),
    h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)
  - 3. fmck: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),

n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)



Parameter	Symbol	-	Conditions		HS ( speed Mc	high- main) ode	LS ( speed Mo	low- main) ode	LV ( volt main)	low- age Mode	Unit
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	$4.0 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V},$ $2.7 \text{ V} \le \text{V}_{\text{b}} \le 4.0 \text{ V}$			Note 1		Note 1		Note 1	bps
				Theoretical value of the maximum transfer rate $C_b = 50 \text{ pF}, \text{ R}_b =$ 1.4 k $\Omega$ , V <sub>b</sub> = 2.7 V		2.8 Note 2		2.8 Note 2		2.8 Note 2	Mbps
			$2.7 V \le EV_{DD0} < 4.0 V,$			Note		Note		Note	bps
			2.3 V ≤ Vb ≤ 2.7 V	Theoretical value of the maximum transfer rate $C_b = 50 \text{ pF}, R_b =$ $2.7 \text{ k}\Omega, V_b = 2.3$ V		1.2 Note 4		1.2 Note 4		1.2 Note 4	Mbps
			$1.8 V \le EV_{DD0} < 3.3 V,$			Notes 5.6		Notes 5.6		Notes 5.6	bps
			1.0 V 2 VI 2 L.0 V	Theoretical value of the maximum transfer rate $C_b = 50 \text{ pF}, R_b =$ $5.5 \text{ k}\Omega, V_b = 1.6$ V		0.43 Note 7		0.43 Note 7		0.43 Note 7	Mbps

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2) (T<sub>A</sub> = -40 to +85°C. 1.8 V  $\leq$  EV<sub>DD0</sub> = EV<sub>DD1</sub>  $\leq$  V<sub>DD</sub>  $\leq$  5.5 V. Vss = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

**Notes 1.** The smaller maximum transfer rate derived by using fMck/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V  $\leq$  EV  $_{DD0} \leq$  5.5 V and 2.7 V  $\leq$  V  $_{b} \leq$  4.0 V

Maximum transfer rate = 
$$\frac{1}{\{-C_b \times R_b \times \ln (1 - \frac{2.2}{V_b})\} \times 3}$$
 [bps]

Baud rate error (theoretical value) = 
$$\frac{\frac{1}{|\text{Transfer rate} \times 2|} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{|\text{Transfer rate}|}) \times \text{Number of transferred bits}} \times 100 [\%]$$

- \* This value is the theoretical value of the relative difference between the transmission and reception sides.
- This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.



(7)	Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp internal clock output,
	corresponding CSI00 only) (2/2)

	<i>,</i>								
Parameter	Symbol	Conditions	HS (hig main)	h-speed Mode	LS (low main)	/-speed Mode	LV (low main)	-voltage Mode	Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) <sup>Note 2</sup>	tsıkı	$\begin{array}{l} 4.0 \ V \leq EV_{DD0} \leq 5.5 \ V, \\ 2.7 \ V \leq V_b \leq 4.0 \ V, \end{array}$	23		110		110		ns
		$C_b = 20 \text{ pF},  \text{R}_b = 1.4  \text{k}\Omega$							
		$\label{eq:2.7} \begin{array}{l} 2.7 \ V \leq EV_{\text{DD0}} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V, \end{array}$	33		110		110		ns
		$C_b = \underline{20 \text{ pF}},  \text{R}_b = 2.7  \text{k}\Omega$							
Slp hold time (from SCKp↓) <sup>Note 2</sup>	tksi1		10		10		10		ns
		$C_b = 20 \text{ pF},  \text{R}_b = 1.4  \text{k}\Omega$							
		$\label{eq:2.7} \begin{array}{l} 2.7 \ V \leq EV_{\text{DD0}} < 4.0 \ V, \\ 2.3 \ V \leq V_{\text{b}} \leq 2.7 \ V, \end{array}$	10		10		10		ns
		$C_b=20 \text{ pF},  \text{R}_b=2.7  \text{k}\Omega$							
Delay time from SCKp↑ to	tkso1	$\begin{array}{l} 4.0 \ V \leq EV_{\text{DD0}} \leq 5.5 \ V, \\ 2.7 \ V \leq V_b \leq 4.0 \ V, \end{array}$		10		10		10	ns
SOp output Note 2		$C_b = 20 \text{ pF}, \text{ R}_b = 1.4 \text{ k}\Omega$							
		$\label{eq:2.7} \begin{array}{l} 2.7 \ V \leq EV_{\text{DD0}} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V, \end{array}$		10		10		10	ns
		$C_{\text{b}} = 20 \text{ pF}, \text{ R}_{\text{b}} = 2.7 \text{ k}\Omega$							

 $(T_A = -40 \text{ to } +85^{\circ}\text{C}, 2.7 \text{ V} \le \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0 \text{ V})$ 

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

- Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 20- to 52-pin products)/EV<sub>DD</sub> tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.
- **Remarks 1.** R<sub>b</sub>[Ω]:Communication line (SCKp, SOp) pull-up resistance, C<sub>b</sub>[F]: Communication line (SCKp, SOp) load capacitance, V<sub>b</sub>[V]: Communication line voltage
  - p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
    g: PIM and POM number (g = 1)
  - 3. fmck: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

- n: Channel number (mn = 00))
- 4. This value is valid only when CSI00's peripheral I/O redirect function is not used.



## (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	tксүı	tксү1 ≥ 4/fc∟к	$4.0 V \le EV_{DD0} \le 5.5 V$ , $2.7 V \le V_b \le 4.0 V$ , $C_{1} = 20 pE_{1} P_{2} = 1.4 kC$	300		1150		1150		ns
			$C_0 = 30 \text{ pr}$ , $H_0 = 1.4 \text{ KS2}$ 2.7 V $\leq$ EV <sub>DD0</sub> < 4.0 V, 2.3 V $\leq$ V <sub>b</sub> $\leq$ 2.7 V, C <sub>b</sub> = 30 pE B <sub>b</sub> = 2.7 kQ	500		1150		1150		ns
			$\begin{split} & 0.5 = 0.0 \ \text{pr} \ \text{, the} = 2.0 \ \text{Nat} \\ & 1.8 \ \text{V} \leq \text{EV}_{\text{DD0}} < 3.3 \ \text{V}, \\ & 1.6 \ \text{V} \leq \text{V}_{\text{b}} \leq 2.0 \ \text{V}^{\text{Note}}, \end{split}$	1150		1150		1150		ns
			$C_{\text{b}}=30 \text{ pF},  \text{R}_{\text{b}}=5.5  \text{k}\Omega$							
SCKp high-level width	tкнı	$\begin{array}{l} 4.0 \ V \leq EV_{\text{DD}} \\ 2.7 \ V \leq V_{\text{b}} \leq \end{array}$	∞ ≤ 5.5 V, 4.0 V,	tксү1/2 – 75		tксү1/2 – 75		tксү1/2 – 75		ns
		$C_b = 30 \text{ pF}, I$	R <sub>b</sub> = 1.4 kΩ							
		$\begin{array}{l} 2.7 \ V \leq EV_{DD} \\ 2.3 \ V \leq V_b \leq \\ C_b = 30 \ pF, \ l \end{array}$	∞ < 4.0 V, 2.7 V, R₀ = 2.7 kΩ	tксү1/2 – 170		tксү1/2 – 170		tксү1/2 – 170		ns
		$1.8 V \le EV_{DE}$ $1.6 V \le V_b \le C_b = 30 \text{ pE}.$	∞ < 3.3 V, 2.0 V <sup>Note</sup> , Bb = 5.5 kΩ	tксү1/2 – 458		tксү1/2 – 458		tксү1/2 – 458		ns
SCKp low-level width	tĸ∟1	$4.0 V \le EV_{DE}$ $2.7 V \le V_b \le C_b = 30 pF, I$	∞ ≤ 5.5 V, 4.0 V, Rь = 1.4 kΩ	tксү1/2 – 12		tксү1/2 – 50		tксү1/2 – 50		ns
		$2.7 \text{ V} \leq \text{EV}_{\text{DE}}$ $2.3 \text{ V} \leq \text{V}_{\text{b}} \leq$ $C_{\text{b}} = 30 \text{ pF}, \text{ I}$	∞ < 4.0 V, 2.7 V, R₀ = 2.7 kΩ	tксү1/2 – 18		tксү1/2 – 50		tксү1/2 – 50		ns
		$\label{eq:linear} \begin{array}{l} 1.8 \ V \leq EV_{DL} \\ 1.6 \ V \leq V_b \leq \\ C_b = 30 \ pF, \end{array}$	∞ < 3.3 V, 2.0 V <sup>Note</sup> , R⊳ = 5.5 kΩ	tксү1/2 – 50		tксү1/2 – 50		tксү1/2 – 50		ns

 $(T_A = -40 \text{ to } +85^{\circ}\text{C}, 1.8 \text{ V} \le \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0 \text{ V})$ 

Note Use it with  $EV_{DD0} \ge V_b$ .

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (VDD tolerance (When 20- to 52-pin products)/EVDD tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)



# (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

$(T_A = -40 \text{ to } +85^\circ C)$	, 1.8 V ≤ EVDD0 =	$=$ EVDD1 $\leq$ VDD $\leq$ 5.5 V, V	Vss = EVsso = EVss1 = 0 V	) (2/2)
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Parameter	Symbol	Conditions	HS ( speed Mo	high- main) ode	LS (low main)	/-speed Mode	LV (low main)	-voltage Mode	Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp high-/low-level width	tкн2, tкL2	$\begin{array}{l} 4.0 \ V \leq EV_{DD0} \leq 5.5 \ V, \\ 2.7 \ V \leq V_b \leq 4.0 \ V \end{array}$	tксү2/2 - 12		tксү2/2 - 50		tксү2/2 - 50		ns
		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V \end{array}$	tксү2/2 – 18		tксү2/2 - 50		tксү2/2 - 50		ns
		$\begin{array}{l} 1.8 \ V \leq EV_{DD0} < 3.3 \ V, \\ 1.6 \ V \leq V_b \leq 2.0 \ V^{\text{Note 2}} \end{array}$	tксү₂/2 − 50		tксү2/2 - 50		tксү2/2 - 50		ns
SIp setup time (to SCKp↑) <sup>№ote 3</sup>	tsık2	$\begin{array}{l} 4.0 \; V \leq E V_{DD0} \leq 5.5 \; V, \\ 2.7 \; V \leq V_b \leq 4.0 \; V \end{array}$	1/fмск + 20		1/fмск + 30		1/fмск + 30		ns
		$\begin{array}{l} 2.7 \ V \leq E V_{DD0} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V \end{array}$	1/fмск + 20		1/fмск + 30		1/fмск + 30		ns
		$\begin{array}{l} 1.8 \ V \leq EV_{DD0} < 3.3 \ V, \\ 1.6 \ V \leq V_b \leq 2.0 \ V^{\text{Note 2}} \end{array}$	1/fмск + 30		1/fмск + 30		1/fмск + 30		ns
SIp hold time (from SCKp↑) <sup>Note 4</sup>	tksi2		1/fмск + 31		1/fмск + 31		1/fмск + 31		ns
Delay time from SCKp↓ to SOp output Note 5	tĸso2	$\label{eq:VDD} \begin{array}{l} 4.0 \ V \leq EV_{\text{DD0}} \leq 5.5 \ V, \ 2.7 \ V \leq V_b \leq 4.0 \\ V, \\ C_b = 30 \ pF, \ R_b = 1.4 \ k\Omega \end{array}$		2/fмск + 120		2/fмск + 573		2/fмск + 573	ns
		$\label{eq:V_def} \begin{array}{l} 2.7 \ V \leq EV_{DD0} < 4.0 \ V, \ 2.3 \ V \leq V_b \leq 2.7 \\ V, \\ C_b = 30 \ pF, \ R_b = 2.7 \ k\Omega \end{array}$		2/fмск + 214		2/fмск + 573		2/fмск + 573	ns
		$\begin{split} & 1.8 \ V \leq E V_{DD0} < 3.3 \ V, \\ & 1.6 \ V \leq V_b \leq 2.0 \ V^{\text{Note 2}}, \\ & C_b = 30 \ pF, \ R_b = 5.5 \ k\Omega \end{split}$		2/fмск + 573		2/fмск + 573		2/fмск + 573	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

- **2.** Use it with  $EV_{DD0} \ge V_b$ .
- 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- 5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp<sup>↑</sup>" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V<sub>DD</sub> tolerance (for the 20- to 52-pin products)/EV<sub>DD</sub> tolerance (for the 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)



### (3) I<sup>2</sup>C fast mode plus

 $(T_A = -40 \text{ to } +85^{\circ}C, 1.6 \text{ V} \le EV_{DD0} = EV_{DD1} \le V_{DD} \le 5.5 \text{ V}, \text{ Vss} = EV_{SS0} = EV_{SS1} = 0 \text{ V})$ 

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fsc∟	Fast mode plus: fc∟κ≥ 10 MHz	$2.7~V \le EV_{\text{DD0}} \le 5.5~V$	0	1000		_		-	kHz
Setup time of restart condition	tsu:sta	$2.7 \text{ V} \leq EV_{DD0} \leq 5.5$	5 V	0.26		_	-	_	-	μs
Hold time <sup>Note 1</sup>	thd:sta	$2.7 V \le EV_{DD0} \le 5.5$	5 V	0.26			-		_	μS
Hold time when SCLA0 = "L"	t∟ow	$2.7 \text{ V} \leq EV_{\text{DD0}} \leq 5.5$	5 V	0.5		_	-	_	-	μs
Hold time when SCLA0 = "H"	tніgн	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5$	5 V	0.26		_	_		-	μs
Data setup time (reception)	tsu:dat	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5$	5 V	50		_	-		-	μS
Data hold time (transmission) <sup>Note 2</sup>	thd:dat	$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5$	5 V	0	0.45		_		-	μs
Setup time of stop condition	tsu:sto	$2.7 \text{ V} \leq EV_{DD0} \leq 5.5$	5 V	0.26			-		-	μS
Bus-free time	tbur	$2.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5$	5 V	0.5			_	_	_	μs

<R>

**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

- 2. The maximum value (MAX.) of the during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.
- Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.
- **Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus:  $C_b = 120 \text{ pF}, R_b = 1.1 \text{ k}\Omega$ 

### **IICA** serial transfer timing



**Remark** n = 0, 1



- **Notes 1.** Excludes quantization error ( $\pm 1/2$  LSB).
  - 2. This value is indicated as a ratio (%FSR) to the full-scale value.
  - $\label{eq:scalar} \begin{array}{l} \textbf{3. When } AV_{\text{REFP}} < V_{\text{DD}} \text{, the MAX. values are as follows.} \\ \text{Overall error: } Add \pm 1.0 \ \text{LSB} \ \text{to the MAX. value when } AV_{\text{REFP}} = V_{\text{DD}} \text{.} \\ \text{Zero-scale error/Full-scale error: } Add \pm 0.05\%\text{FSR} \ \text{to the MAX. value when } AV_{\text{REFP}} = V_{\text{DD}} \text{.} \\ \text{Integral linearity error/ Differential linearity error: } Add \pm 0.5 \ \text{LSB} \ \text{to the MAX. value when } AV_{\text{REFP}} = V_{\text{DD}} \text{.} \\ \end{array}$
  - 4. Values when the conversion time is set to 57  $\mu s$  (min.) and 95  $\mu s$  (max.).
  - 5. Refer to 2.6.2 Temperature sensor/internal reference voltage characteristics.



- **Notes 1.** Total current flowing into V<sub>DD</sub> and EV<sub>DD0</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub> or Vss, EV<sub>SS0</sub>. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  - 2. During HALT instruction execution by flash memory.
  - 3. When high-speed on-chip oscillator and subsystem clock are stopped.
  - 4. When high-speed system clock and subsystem clock are stopped.
  - When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  - 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  - 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:  $2.7 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}@1 \text{ MHz}$  to 32 MHz

2.4 V 
$$\leq$$
 V<sub>DD</sub>  $\leq$  5.5 V@1 MHz to 16 MHz

- 8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remarks 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  - 2. file: High-speed on-chip oscillator clock frequency
  - 3. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
  - 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^{\circ}C$



- **Notes 1.** Total current flowing into VDD, EVDDD, and EVDD1, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDDD, and EVDD1, or Vss, EVsso, and EVss1. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  - 2. When high-speed on-chip oscillator and subsystem clock are stopped.
  - 3. When high-speed system clock and subsystem clock are stopped.
  - 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  - **5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V  $\leq$  V\_DD  $\leq$  5.5 V@1 MHz to 32 MHz

2.4 V  $\leq$  V<sub>DD</sub>  $\leq$  5.5 V@1 MHz to 16 MHz

- **Remarks 1.** fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  - 2. fin: High-speed on-chip oscillator clock frequency
  - 3. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
  - 4. Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C



- **Notes 1.** Excludes quantization error ( $\pm 1/2$  LSB).
  - 2. This value is indicated as a ratio (%FSR) to the full-scale value.
  - $\label{eq:scalar} \begin{array}{l} \textbf{3. When } AV_{\text{REFP}} < V_{\text{DD}} \text{, the MAX. values are as follows.} \\ \text{Overall error: } Add \pm 1.0 \ \text{LSB} \ \text{to the MAX. value when } AV_{\text{REFP}} = V_{\text{DD}} \text{.} \\ \text{Zero-scale error/Full-scale error: } Add \pm 0.05\%\text{FSR} \ \text{to the MAX. value when } AV_{\text{REFP}} = V_{\text{DD}} \text{.} \\ \text{Integral linearity error/ Differential linearity error: } Add \pm 0.5 \ \text{LSB} \ \text{to the MAX. value when } AV_{\text{REFP}} = V_{\text{DD}} \text{.} \\ \end{array}$
  - 4. Refer to 3.6.2 Temperature sensor/internal reference voltage characteristics.



(2) When reference voltage (+) = AV<sub>REFP</sub>/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV<sub>REFM</sub>/ANI1 (ADREFM = 1), target pin : ANI16 to ANI26

 $(T_{A} = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, 2.4 \text{ V} \le \text{AV}_{\text{REFP}} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0 \text{ V},$ Reference voltage (+) = AV\_{\text{REFP}}, Reference voltage (-) = AV\_{\text{REFM}} = 0 \text{ V})

Parameter	Symbol	Conditior	าร	MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error <sup>Note 1</sup>	AINL	$\begin{array}{l} \mbox{10-bit resolution} \\ EV_{DD0} \leq AV_{\text{REFP}} = V_{\text{DD}}  {}^{\text{Notes 3, 4}} \end{array}$	$\begin{array}{l} 2.4 \ V \leq AV_{\text{REFP}} \leq 5.5 \\ V \end{array}$		1.2	±5.0	LSB
Conversion time	<b>t</b> CONV	10-bit resolution	$3.6~V \leq V \text{DD} \leq 5.5~V$	2.125		39	μs
		Target pin : ANI16 to ANI26	$2.7~V \leq V\text{DD} \leq 5.5~V$	3.1875		39	μS
			$2.4~V \leq V\text{DD} \leq 5.5~V$	17		39	μS
Zero-scale error <sup>Notes 1, 2</sup>	Ezs	$\begin{array}{l} 10\text{-bit resolution} \\ EV\text{DD0} \leq AV_{\text{REFP}} = V_{\text{DD}} \\ \end{array} \end{array} \label{eq:expansion}$	$\begin{array}{l} 2.4 \hspace{0.1 cm} V \leq AV_{\text{REFP}} \leq 5.5 \\ V \end{array}$			±0.35	%FSR
Full-scale error <sup>Notes 1, 2</sup>	Efs	$\begin{array}{l} \text{10-bit resolution} \\ \text{EVDD0} \leq AV_{\text{REFP}} = V_{\text{DD}} \\ \end{array} \end{array}$	$\begin{array}{l} 2.4 \hspace{0.1 cm} V \leq AV_{\text{REFP}} \leq 5.5 \\ V \end{array}$			±0.35	%FSR
Integral linearity error <sup>Note 1</sup>	ILE	$\begin{array}{l} \mbox{10-bit resolution} \\ EV \mbox{DD0} \leq A V_{\text{REFP}} = V_{\text{DD}} ^{\text{Notes 3, 4}} \end{array}$	$\begin{array}{l} 2.4 \ V \leq AV_{\text{REFP}} \leq 5.5 \\ V \end{array}$			±3.5	LSB
Differential linearity error	DLE	$\label{eq:loss} \begin{array}{l} 10\text{-bit resolution} \\ EV \text{DD0} \leq AV_{\text{REFP}} = V_{\text{DD}} \\ \end{array} \end{array}$	$\begin{array}{l} 2.4 \hspace{0.1 cm} V \leq AV_{\text{REFP}} \leq 5.5 \\ V \end{array}$			±2.0	LSB
Analog input voltage	Vain	ANI16 to ANI26		0		AVREFP and EVDD0	V

**Notes 1.** Excludes quantization error ( $\pm 1/2$  LSB).

- 2. This value is indicated as a ratio (%FSR) to the full-scale value.
- When AV<sub>REFP</sub> < V<sub>DD</sub>, the MAX. values are as follows. Overall error: Add ±1.0 LSB to the MAX. value when AV<sub>REFP</sub> = V<sub>DD</sub>. Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV<sub>REFP</sub> = V<sub>DD</sub>. Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV<sub>REFP</sub> = V<sub>DD</sub>.
   When AV<sub>REFP</sub> < EV<sub>DD0</sub> ≤ V<sub>DD</sub>, the MAX. values are as follows.
- 4. When AVREFP < EVDDO S VDD, the MAX. values are as follows. Overall error: Add ±4.0 LSB to the MAX. value when AVREFP = VDD. Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AVREFP = VDD. Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AVREFP = VDD.



# 4. PACKAGE DRAWINGS

### 4.1 20-pin Products

R5F1006AASP, R5F1006CASP, R5F1006DASP, R5F1006EASP R5F1016AASP, R5F1016CASP, R5F1016DASP, R5F1016EASP R5F1006ADSP, R5F1006CDSP, R5F1006DDSP, R5F1006EDSP R5F1016ADSP, R5F1016CDSP, R5F1016DDSP, R5F1016EDSP R5F1006AGSP, R5F1006CGSP, R5F1006DGSP, R5F1006EGSP

° I		
P-LSSOP20-0300-0.65 PLS	SP0020JC-A S20MC-	65-5A4-3 0.12



Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

D	$0.24^{+0.08}_{-0.07}$
Е	0.1±0.05
F	1.3±0.1
G	1.2
Н	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
М	0.13
Ν	0.10
Ρ	3° <sup>+5°</sup> -3°
Т	0.25
U	0.6±0.15

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## 4.4 30-pin Products

R5F100AAASP, R5F100ACASP, R5F100ADASP, R5F100AEASP, R5F100AFASP, R5F100AGASP R5F101AAASP, R5F101ACASP, R5F101ADASP, R5F101AEASP, R5F101AFASP, R5F101AGASP R5F100AADSP, R5F100ACDSP, R5F100ADDSP, R5F100AEDSP, R5F100AFDSP, R5F100AGDSP R5F101AADSP, R5F101ACDSP, R5F101ADDSP, R5F101AEDSP, R5F101AFDSP, R5F101AGDSP R5F100AAGSP, R5F100ACGSP, R5F100ADGSP, R5F100AEGSP, R5F100AFGSP, R5F100AGGSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18





0.5

0.13

0.10 3°+5°

0.25

0.6±0.15

L

M

P T

U

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## 4.7 40-pin Products

R5F100EAANA, R5F100ECANA, R5F100EDANA, R5F100EEANA, R5F100EFANA, R5F100EGANA, R5F100EHANA R5F101EAANA, R5F101ECANA, R5F101EDANA, R5F101EEANA, R5F101EFANA, R5F101EGANA, R5F101EHANA R5F100EADNA, R5F100ECDNA, R5F100EDDNA, R5F100EEDNA, R5F100EFDNA, R5F100EGDNA, R5F100EHDNA

R5F101EADNA, R5F101ECDNA, R5F101EDDNA, R5F101EEDNA, R5F101EFDNA, R5F101EGDNA, R5F101EHDNA

R5F100EAGNA, R5F100ECGNA, R5F100EDGNA, R5F100EEGNA, R5F100EFGNA, R5F100EGGNA, R5F100EHGNA

JEITA Package code	RENESAS code	Previous code	MASS (TYP.) [g]
P-HWQFN40-6x6-0.50	PWQN0040KC-A	P40K8-50-4B4-5	0.09



Detail of (A) Part







Referance	Dimension in Millimeters		
Symbol	Min	Nom	Max
D	5.95	6.00	6.05
E	5.95	6.00	6.05
А			0.80
A <sub>1</sub>	0.00		
b	0.18	0.25	0.30
е	—	0.50	
Lp	0.30	0.40	0.50
х			0.05
у			0.05
ZD		0.75	
Z <sub>E</sub>		0.75	
C2	0.15	0.20	0.25
D <sub>2</sub>		4.50	
E <sub>2</sub>		4.50	

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		Description	
Rev.	Date	Page	Summary
3.00	Aug 02, 2013	81	Modification of figure of AC Timing Test Points
		81	Modification of description and note 3 in (1) During communication at same potential (UART mode)
		83	Modification of description in (2) During communication at same potential (CSI mode)
		84	Modification of description in (3) During communication at same potential (CSI mode)
		85	Modification of description in (4) During communication at same potential (CSI mode) (1/2)
		86	Modification of description in (4) During communication at same potential (CSI mode) (2/2)
		88	Modification of table in (5) During communication at same potential (simplified I <sup>2</sup> C mode) (1/2)
		89	Modification of table and caution in (5) During communication at same potential (simplified I <sup>2</sup> C mode) (2/2)
		91	Modification of table and notes 1 and 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)
		92, 93	Modification of table and notes 2 to 7 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		94	Modification of remarks 1 to 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		95	Modification of table in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (1/2)
	96	Modification of table and caution in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (2/2)	
	97	Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3)	
	98	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3)	
		99	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		100	Modification of remarks 3 and 4 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		102	Modification of table in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/2)
		103	Modification of table and caution in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/2)
		106	Modification of table in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified $I^2C$ mode) (1/2)
		107	Modification of table, note 1, and caution in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified $I^2C$ mode) (2/2)
		109	Addition of (1) I <sup>2</sup> C standard mode
		111	Addition of (2) I <sup>2</sup> C fast mode
	112	Addition of (3) I <sup>2</sup> C fast mode plus	
	112	Modification of IICA serial transfer timing	
	113	Addition of table in 2.6.1 A/D converter characteristics	
	113	Modification of description in 2.6.1 (1)	
		114	Modification of notes 3 to 5 in 2.6.1 (1)
		115	Modification of description and notes 2, 4, and 5 in 2.6.1 (2)
		116	Modification of description and notes 3 and 4 in 2.6.1 (3)
	117	Modification of description and notes 3 and 4 in 2.6.1 (4)	