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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 9x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-HWQFN (6x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100ecgna-u0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100ecgna-u0</a>

Table 1-1. List of Ordering Part Numbers

(1/12)

Pin count	Package	Data flash	Fields of Application <sup>Note</sup>	Ordering Part Number
20 pins	20-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	Mounted	A	R5F1006AASP#V0, R5F1006CASP#V0, R5F1006DASP#V0, R5F1006EASP#V0 R5F1006AASP#X0, R5F1006CASP#X0, R5F1006DASP#X0, R5F1006EASP#X0
			D	R5F1006ADSP#V0, R5F1006CDSP#V0, R5F1006DDSP#V0, R5F1006EDSP#V0 R5F1006ADSP#X0, R5F1006CDSP#X0, R5F1006DDSP#X0, R5F1006EDSP#X0
			G	R5F1006AGSP#V0, R5F1006CGSP#V0, R5F1006DGSP#V0, R5F1006EGSP#V0 R5F1006AGSP#X0, R5F1006CGSP#X0, R5F1006DGSP#X0, R5F1006EGSP#X0
		Not mounted	A	R5F1016AASP#V0, R5F1016CASP#V0, R5F1016DASP#V0, R5F1016EASP#V0 R5F1016AASP#X0, R5F1016CASP#X0, R5F1016DASP#X0, R5F1016EASP#X0
			D	R5F1016ADSP#V0, R5F1016CDSP#V0, R5F1016DDSP#V0, R5F1016EDSP#V0 R5F1016ADSP#X0, R5F1016CDSP#X0, R5F1016DDSP#X0, R5F1016EDSP#X0
			G	R5F1016AGSP#V0, R5F1016CGSP#V0, R5F1016DGSP#V0, R5F1016EGSP#V0 R5F1016AGSP#X0, R5F1016CGSP#X0, R5F1016DGSP#X0, R5F1016EGSP#X0
24 pins	24-pin plastic HWQFN (4 × 4mm, 0.5 mm pitch)	Mounted	A	R5F1007AANA#U0, R5F1007CANA#U0, R5F1007DANA#U0, R5F1007EANA#U0 R5F1007AANA#W0, R5F1007CANA#W0, R5F1007DANA#W0, R5F1007EANA#W0
			D	R5F1007ADNA#U0, R5F1007CDNA#U0, R5F1007DDNA#U0, R5F1007EDNA#U0 R5F1007ADNA#W0, R5F1007CDNA#W0, R5F1007DDNA#W0, R5F1007EDNA#W0
			G	R5F1007AGNA#U0, R5F1007CGNA#U0, R5F1007DGNA#U0, R5F1007EGNA#U0 R5F1007AGNA#W0, R5F1007CGNA#W0, R5F1007DGNA#W0, R5F1007EGNA#W0
		Not mounted	A	R5F1017AANA#U0, R5F1017CANA#U0, R5F1017DANA#U0, R5F1017EANA#U0 R5F1017AANA#W0, R5F1017CANA#W0, R5F1017DANA#W0, R5F1017EANA#W0
			D	R5F1017ADNA#U0, R5F1017CDNA#U0, R5F1017DDNA#U0, R5F1017EDNA#U0 R5F1017ADNA#W0, R5F1017CDNA#W0, R5F1017DDNA#W0, R5F1017EDNA#W0
			G	R5F1017AGNA#U0, R5F1017CGNA#U0, R5F1017DGNA#U0, R5F1017EGNA#U0 R5F1017AGNA#W0, R5F1017CGNA#W0, R5F1017DGNA#W0, R5F1017EGNA#W0

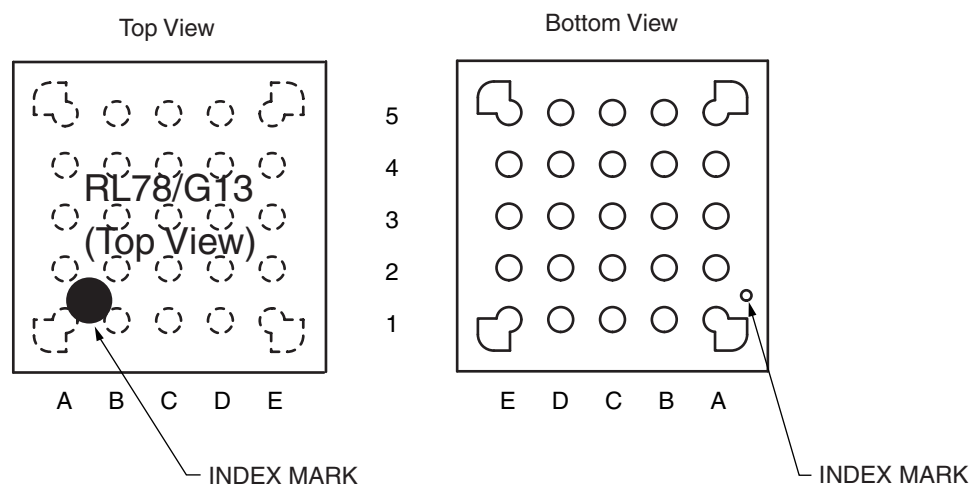
**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

**Caution** The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

## 1.3.3 25-pin products

- 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch)

&lt;R&gt;

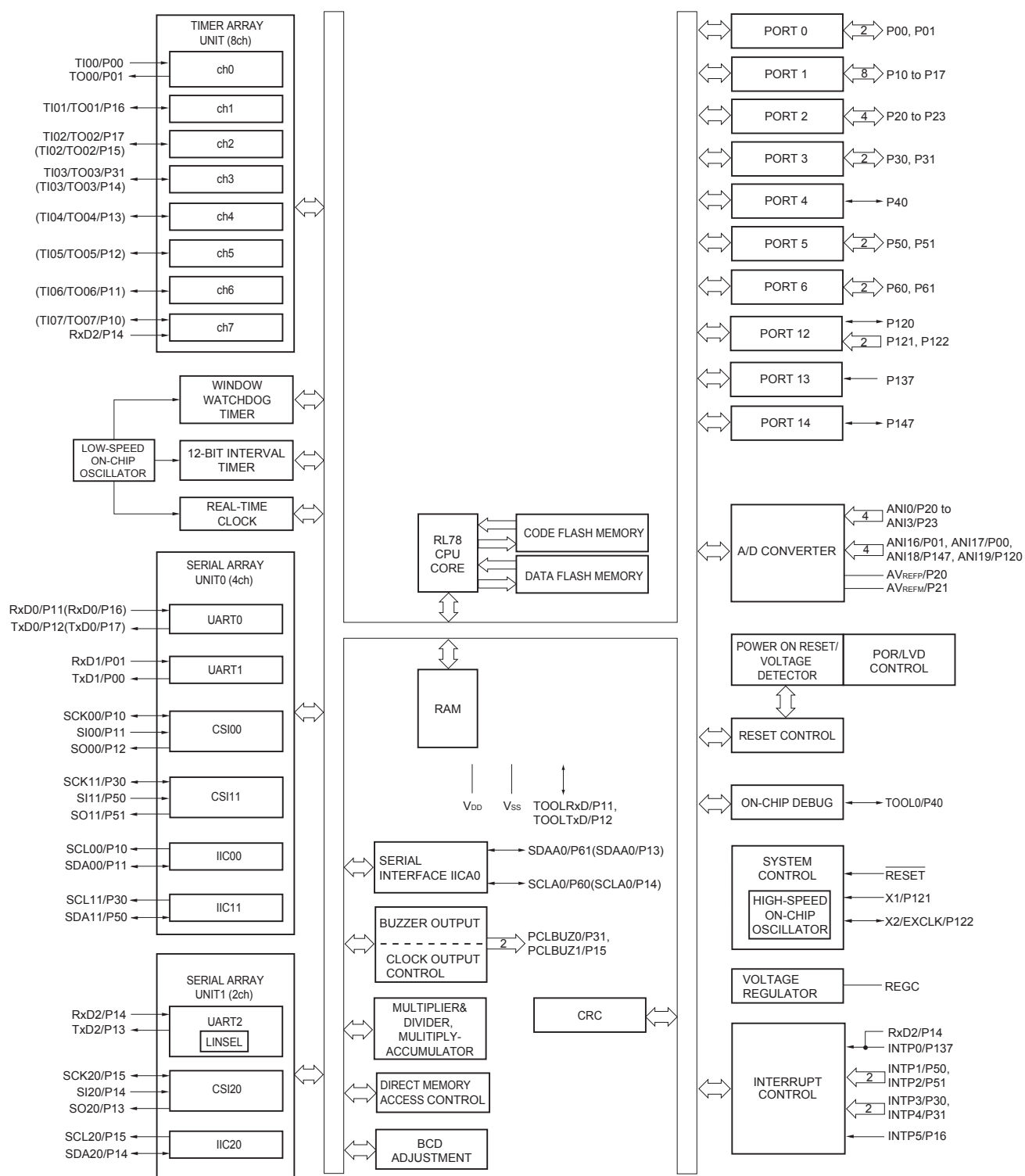


	A	B	C	D	E	
5	P40/TOOL0	RESET	P01/ANI16/ TO00/RxD1	P22/ANI2	P147/ANI18	5
4	P122/X2/ EXCLK	P137/INTP0	P00/ANI17/ TI00/TxD1	P21/ANI1/ AV <sub>REFM</sub>	P10/SCK00/ SCL00	4
3	P121/X1	V <sub>DD</sub>	P20/ANI0/ AV <sub>REFP</sub>	P12/SO00/ TxD0/ TOOLTxD	P11/SI00/ RxD0/ TOOLRxD/ SDA00	3
2	REGC	V <sub>SS</sub>	P30/INTP3/ SCK11/SCL11	P17/TI02/ TO02/SO11	P50/INTP1/ SI11/SDA11	2
1	P60/SCLA0	P61/SDAA0	P31/TI03/ TO03/INTP4/ PCLBUZ0	P16/TI01/ TO01/INTP5	P130	1
	A	B	C	D	E	

**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F).

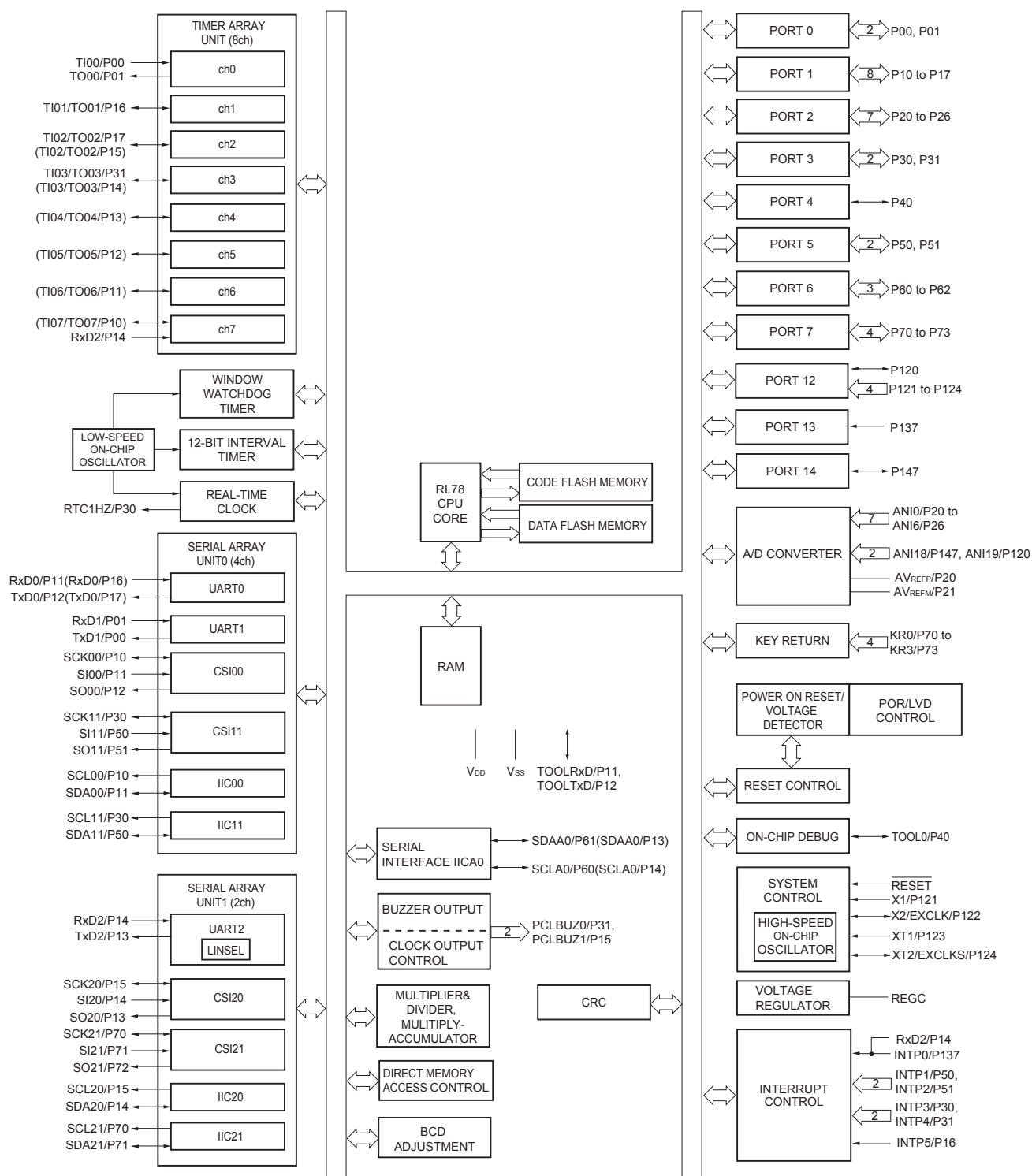
**Remark** For pin identification, see 1.4 Pin Identification.

## 1.5.4 30-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.5.7 40-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T<sub>A</sub> = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V <sub>DD</sub>		-0.5 to +6.5	V
	EV <sub>DD0</sub> , EV <sub>DD1</sub>	EV <sub>DD0</sub> = EV <sub>DD1</sub>	-0.5 to +6.5	V
	EV <sub>SS0</sub> , EV <sub>SS1</sub>	EV <sub>SS0</sub> = EV <sub>SS1</sub>	-0.5 to +0.3	V
REGC pin input voltage	V <sub>IREGC</sub>	REGC	-0.3 to +2.8 and -0.3 to V <sub>DD</sub> + 0.3 <sup>Note 1</sup>	V
Input voltage	V <sub>I1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	-0.3 to EV <sub>DD0</sub> + 0.3 and -0.3 to V <sub>DD</sub> + 0.3 <sup>Note 2</sup>	V
	V <sub>I2</sub>	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V <sub>I3</sub>	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, RESET	-0.3 to V <sub>DD</sub> + 0.3 <sup>Note 2</sup>	V
Output voltage	V <sub>O1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-0.3 to EV <sub>DD0</sub> + 0.3 and -0.3 to V <sub>DD</sub> + 0.3 <sup>Note 2</sup>	V
	V <sub>O2</sub>	P20 to P27, P150 to P156	-0.3 to V <sub>DD</sub> + 0.3 <sup>Note 2</sup>	V
Analog input voltage	V <sub>AI1</sub>	ANI16 to ANI26	-0.3 to EV <sub>DD0</sub> + 0.3 and -0.3 to AV <sub>REF</sub> (+) + 0.3 <sup>Notes 2, 3</sup>	V
	V <sub>AI2</sub>	ANI0 to ANI14	-0.3 to V <sub>DD</sub> + 0.3 and -0.3 to AV <sub>REF</sub> (+) + 0.3 <sup>Notes 2, 3</sup>	V

**Notes 1.** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**2.** Must be 6.5 V or lower.

**3.** Do not exceed AV<sub>REF</sub>(+) + 0.3 V in case of A/D conversion target pin.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**2.** AV<sub>REF</sub>(+) : + side reference voltage of the A/D converter.

**3.** V<sub>SS</sub> : Reference voltage

**(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products****(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (1/2)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I <sub>DD1</sub>	Operating mode	HS (high-speed main) mode Note 5	f <sub>IH</sub> = 32 MHz Note 3	Basic operation	V <sub>DD</sub> = 5.0 V		2.3		mA
						V <sub>DD</sub> = 3.0 V		2.3		mA
					Normal operation	V <sub>DD</sub> = 5.0 V		5.2	8.5	mA
						V <sub>DD</sub> = 3.0 V		5.2	8.5	mA
				f <sub>IH</sub> = 24 MHz Note 3	Normal operation	V <sub>DD</sub> = 5.0 V		4.1	6.6	mA
						V <sub>DD</sub> = 3.0 V		4.1	6.6	mA
				f <sub>IH</sub> = 16 MHz Note 3	Normal operation	V <sub>DD</sub> = 5.0 V		3.0	4.7	mA
						V <sub>DD</sub> = 3.0 V		3.0	4.7	mA
			LS (low-speed main) mode Note 5	f <sub>IH</sub> = 8 MHz Note 3	Normal operation	V <sub>DD</sub> = 3.0 V		1.3	2.1	mA
						V <sub>DD</sub> = 2.0 V		1.3	2.1	mA
			LV (low-voltage main) mode Note 5	f <sub>IH</sub> = 4 MHz Note 3	Normal operation	V <sub>DD</sub> = 3.0 V		1.3	1.8	mA
						V <sub>DD</sub> = 2.0 V		1.3	1.8	mA
			HS (high-speed main) mode Note 5	f <sub>MX</sub> = 20 MHz Note 2, V <sub>DD</sub> = 5.0 V	Normal operation	Square wave input		3.4	5.5	mA
						Resonator connection		3.6	5.7	mA
				f <sub>MX</sub> = 20 MHz Note 2, V <sub>DD</sub> = 3.0 V	Normal operation	Square wave input		3.4	5.5	mA
						Resonator connection		3.6	5.7	mA
				f <sub>MX</sub> = 10 MHz Note 2, V <sub>DD</sub> = 5.0 V	Normal operation	Square wave input		2.1	3.2	mA
						Resonator connection		2.1	3.2	mA
				f <sub>MX</sub> = 10 MHz Note 2, V <sub>DD</sub> = 3.0 V	Normal operation	Square wave input		2.1	3.2	mA
						Resonator connection		2.1	3.2	mA
			LS (low-speed main) mode Note 5	f <sub>MX</sub> = 8 MHz Note 2, V <sub>DD</sub> = 3.0 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.2	2.0	mA
				f <sub>MX</sub> = 8 MHz Note 2, V <sub>DD</sub> = 2.0 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.2	2.0	mA
			Subsystem clock operation	f <sub>SUB</sub> = 32.768 kHz Note 4 T <sub>A</sub> = -40°C	Normal operation	Square wave input		4.8	5.9	μA
						Resonator connection		4.9	6.0	μA
				f <sub>SUB</sub> = 32.768 kHz Note 4 T <sub>A</sub> = +25°C	Normal operation	Square wave input		4.9	5.9	μA
						Resonator connection		5.0	6.0	μA
				f <sub>SUB</sub> = 32.768 kHz Note 4 T <sub>A</sub> = +50°C	Normal operation	Square wave input		5.0	7.6	μA
						Resonator connection		5.1	7.7	μA
				f <sub>SUB</sub> = 32.768 kHz Note 4 T <sub>A</sub> = +70°C	Normal operation	Square wave input		5.2	9.3	μA
						Resonator connection		5.3	9.4	μA
				f <sub>SUB</sub> = 32.768 kHz Note 4 T <sub>A</sub> = +85°C	Normal operation	Square wave input		5.7	13.3	μA
						Resonator connection		5.8	13.4	μA

(Notes and Remarks are listed on the next page.)

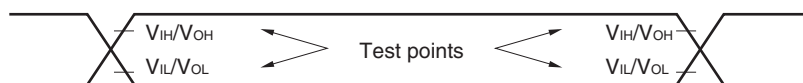
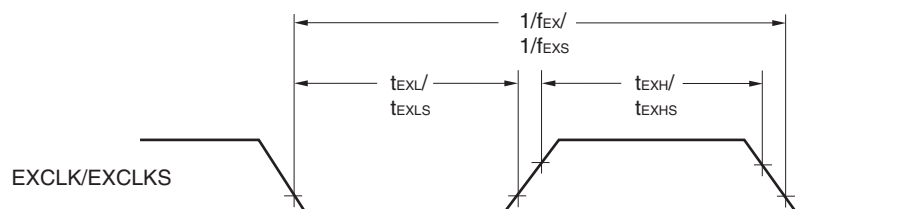
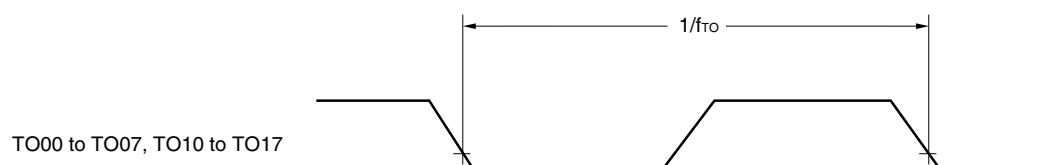
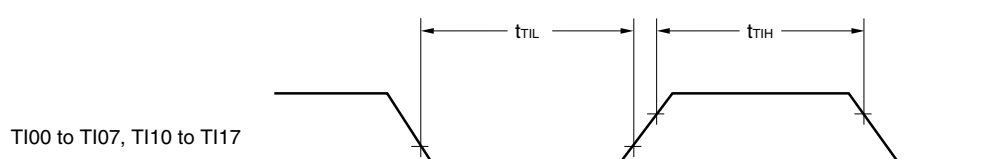
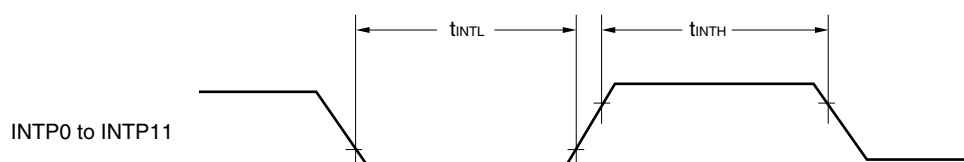
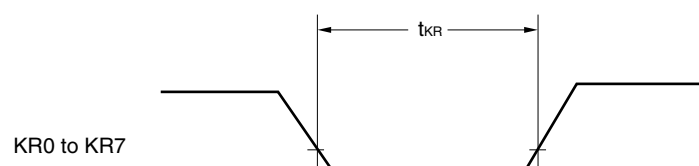
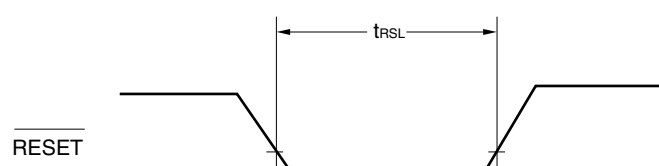
- Notes**
1. Total current flowing into  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , or  $V_{SS}$ ,  $EV_{SS0}$ , and  $EV_{SS1}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. During HALT instruction execution by flash memory.
  3. When high-speed on-chip oscillator and subsystem clock are stopped.
  4. When high-speed system clock and subsystem clock are stopped.
  5. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $RTCLPC = 1$  and setting ultra-low current consumption ( $AMPHS1 = 1$ ). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
    - HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 32 MHz  
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 16 MHz
    - LS (low-speed main) mode:  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 8 MHz
    - LV (low-voltage main) mode:  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 4 MHz
  8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks 1.** f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
3. f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T<sub>A</sub> = 25°C



- Notes**
1. Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, or V<sub>SS</sub>, EV<sub>SS0</sub>, and EV<sub>SS1</sub>. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. When high-speed on-chip oscillator and subsystem clock are stopped.
  3. When high-speed system clock and subsystem clock are stopped.
  4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
    - HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 32 MHz
    - $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 16 MHz
    - LS (low-speed main) mode:  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 8 MHz
    - LV (low-voltage main) mode:  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 4 MHz

- Remarks**
1. f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2. f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
  3. f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

**AC Timing Test Points****External System Clock Timing****TI/TO Timing****Interrupt Request Input Timing****Key Interrupt Input Timing****RESET Input Timing**

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)****(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V		<b>Note 1</b>		<b>Note 1</b>		<b>Note 1</b>	bps
					2.8 Note 2		2.8 Note 2		2.8 Note 2	Mbps
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V		<b>Note 3</b>		<b>Note 3</b>		<b>Note 3</b>	bps
					1.2 Note 4		1.2 Note 4		1.2 Note 4	Mbps
			1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V		<b>Notes 5, 6</b>		<b>Notes 5, 6</b>		<b>Notes 5, 6</b>	bps
					0.43 Note 7		0.43 Note 7		0.43 Note 7	Mbps

**Notes 1.** The smaller maximum transfer rate derived by using f<sub>MCK</sub>/6 or the following expression is the valid maximum transfer rate.

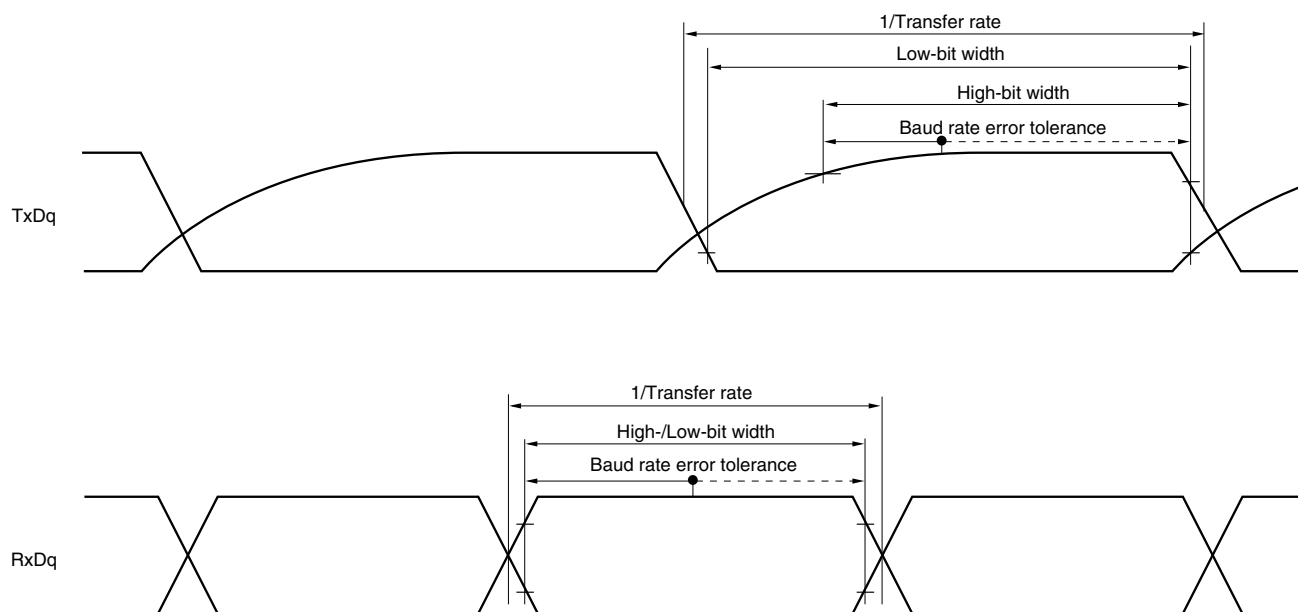
Expression for calculating the transfer rate when 4.0 V ≤ EV<sub>DD0</sub> ≤ 5.5 V and 2.7 V ≤ V<sub>b</sub> ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

**UART mode bit width (during communication at different potential) (reference)**

- Remarks**
1.  $R_b[\Omega]$ : Communication line (TxDq) pull-up resistance,  
 $C_b[\text{F}]$ : Communication line (TxDq) load capacitance,  $V_b[\text{V}]$ : Communication line voltage
  2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
  3.  $f_{\text{MCK}}$ : Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))
  4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

## 2.8 Flash Memory Programming Characteristics

(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f <sub>CLK</sub>	1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V	1		32	MHz
Number of code flash rewrites <small>Notes 1, 2, 3</small>	C <sub>erwr</sub>	Retained for 20 years T <sub>A</sub> = 85°C	1,000			Times
Number of data flash rewrites <small>Notes 1, 2, 3</small>		Retained for 1 years T <sub>A</sub> = 25°C		1,000,000		
		Retained for 5 years T <sub>A</sub> = 85°C	100,000			
		Retained for 20 years T <sub>A</sub> = 85°C	10,000			

**Notes** 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 2.9 Dedicated Flash Memory Programmer Communication (UART)

(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

- Notes**
1. Total current flowing into  $V_{DD}$  and  $EV_{DD0}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$  or  $V_{SS}$ ,  $EV_{SS0}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. When high-speed on-chip oscillator and subsystem clock are stopped.
  3. When high-speed system clock and subsystem clock are stopped.
  4. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $AMPHS1 = 1$  (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.  
HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$   
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$

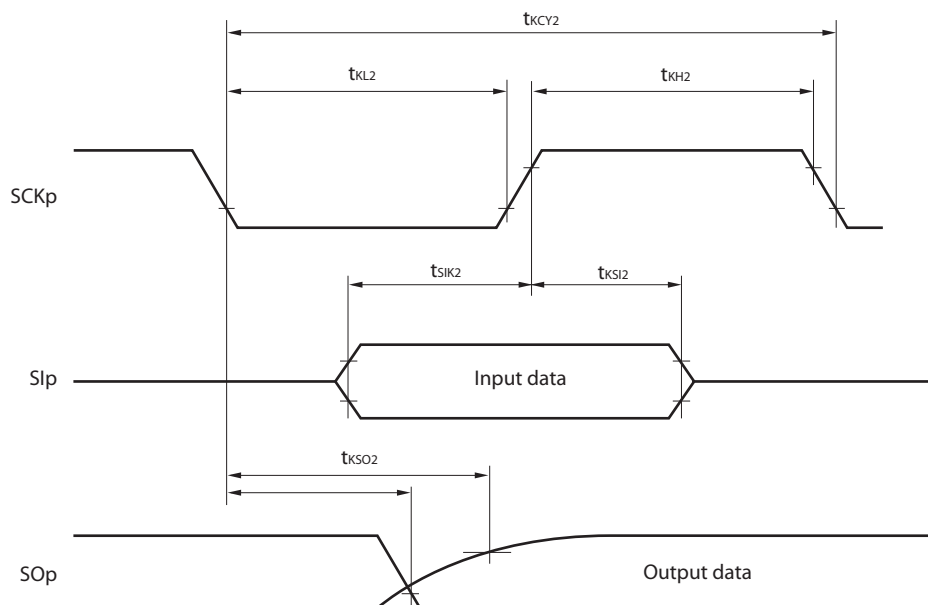
- Notes**
1. Total current flowing into  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , or  $V_{SS}$ ,  $EV_{SS0}$ , and  $EV_{SS1}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. When high-speed on-chip oscillator and subsystem clock are stopped.
  3. When high-speed system clock and subsystem clock are stopped.
  4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$

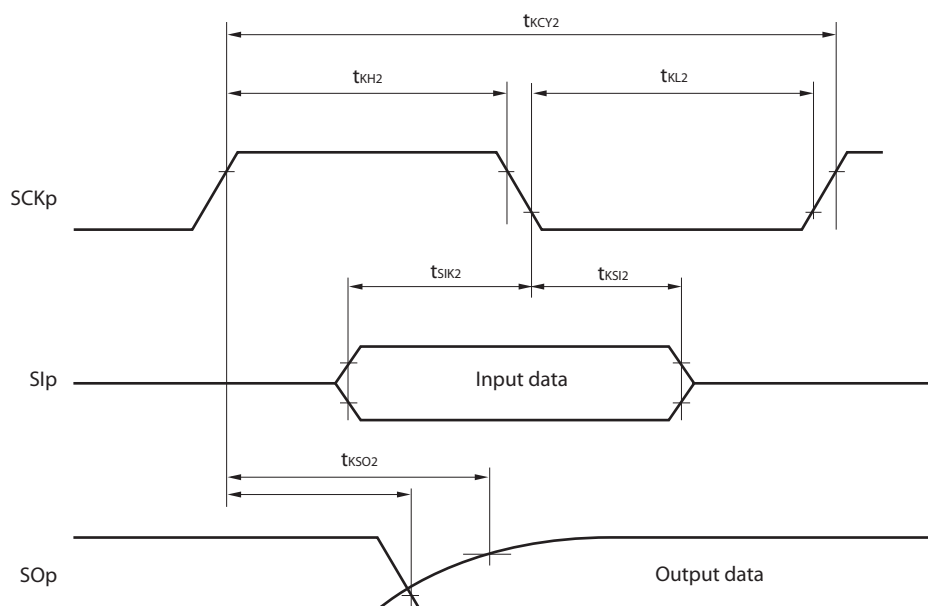
$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



- Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,  
 n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
- 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.  
 Use other CSI for communication at different potential.

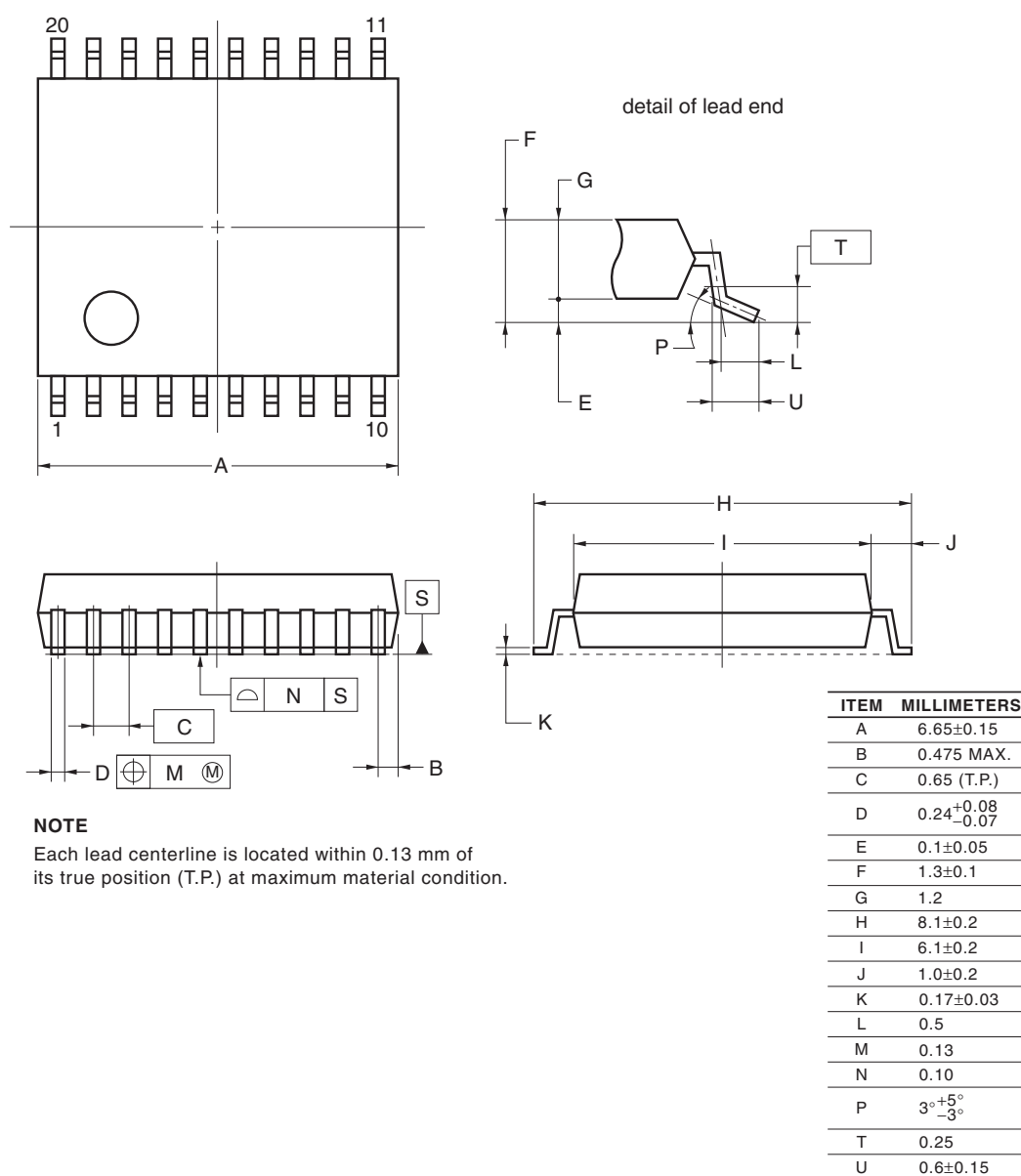


## 4. PACKAGE DRAWINGS

### 4.1 20-pin Products

R5F1006AASP, R5F1006CASP, R5F1006DASP, R5F1006EASP  
 R5F1016AASP, R5F1016CASP, R5F1016DASP, R5F1016EASP  
 R5F1006ADSP, R5F1006CDSP, R5F1006DDSP, R5F1006EDSP  
 R5F1016ADSP, R5F1016CDSP, R5F1016DDSP, R5F1016EDSP  
 R5F1006AGSP, R5F1006CGSP, R5F1006DGSP, R5F1006EGSP

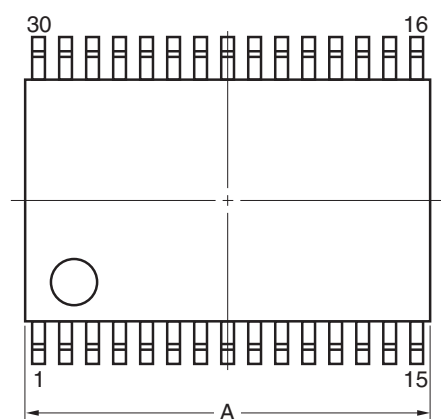
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-0300-0.65	PLSP0020JC-A	S20MC-65-5A4-3	0.12



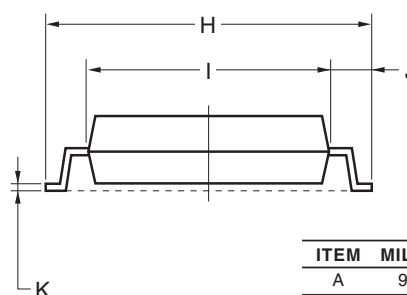
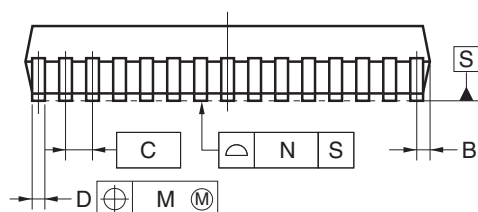
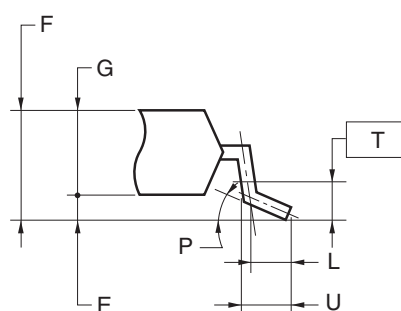
## 4.4 30-pin Products

R5F100AAASP, R5F100ACASP, R5F100ADASP, R5F100AEASP, R5F100AFASP, R5F100AGASP  
 R5F101AAASP, R5F101ACASP, R5F101ADASP, R5F101AEASP, R5F101AFASP, R5F101AGASP  
 R5F100AADSP, R5F100ACDSP, R5F100ADDSP, R5F100AEDSP, R5F100AFDSP, R5F100AGDSP  
 R5F101AADSP, R5F101ACDSP, R5F101ADDSP, R5F101AEDSP, R5F101AFDSP, R5F101AGDSP  
 R5F100AAGSP, R5F100ACGSP, R5F100ADGSP, R5F100AEGSP, R5F100AFGSP, R5F100AGGSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



detail of lead end

**NOTE**

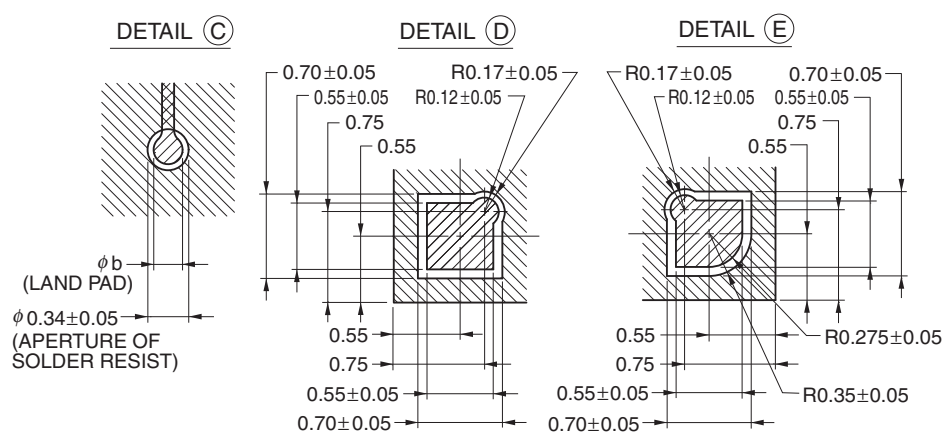
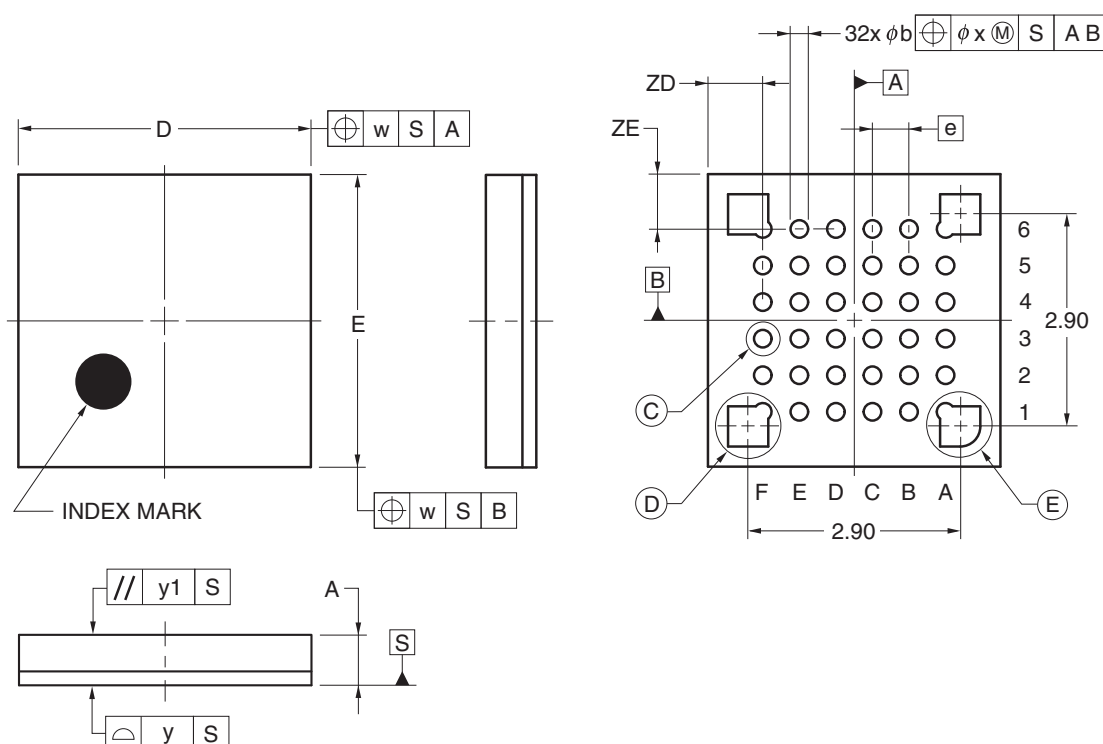
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	0.24 <sup>+0.08</sup> <sub>-0.07</sub>
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	3° <sup>+5°</sup> <sub>-3°</sub>
T	0.25
U	0.6±0.15

## 4.6 36-pin Products

R5F100CAALA, R5F100CCALA, R5F100CDALA, R5F100CEALA, R5F100CFALA, R5F100CGALA  
 R5F101CAALA, R5F101CCALA, R5F101CDALA, R5F101CEALA, R5F101CFALA, R5F101CGALA  
 R5F100CAGLA, R5F100CCGLA, R5F100CDGLA, R5F100CEGLA, R5F100CFGLA, R5F100CGGLA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA36-4x4-0.50	PWLG0036KA-A	P36FC-50-AA4-2	0.023



(UNIT:mm)

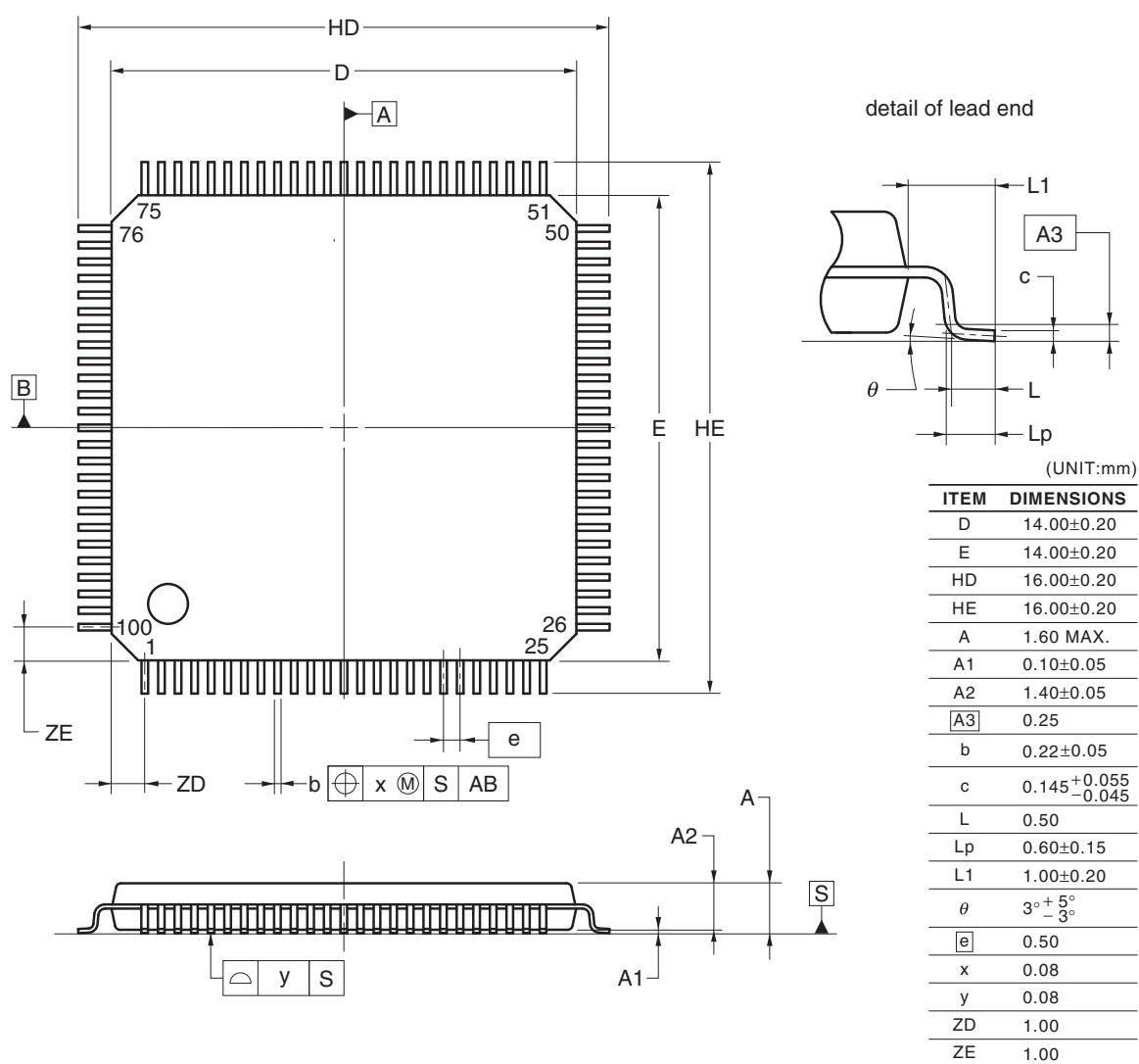
ITEM	DIMENSIONS
D	4.00±0.10
E	4.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

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## 4.13 100-pin Products

R5F100PFAFB, R5F100PGAFB, R5F100PHAFB, R5F100PJAFB, R5F100PKAFB, R5F100PLAFB  
 R5F101PFAFB, R5F101PGAFB, R5F101PHAFB, R5F101PJAFB, R5F101PKAFB, R5F101PLAFB  
 R5F100PFDDB, R5F100PGDFB, R5F100PHDFB, R5F100PJDFB, R5F100PKDFB, R5F100PLDFB  
 R5F101PFDDB, R5F101PGDFB, R5F101PHDFB, R5F101PJDFB, R5F101PKDFB, R5F101PLDFB  
 R5F100PFGFB, R5F100PGGFB, R5F100PHGFB, R5F100PJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69



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Rev.	Date	Description	
		Page	Summary
3.00	Aug 02, 2013	163	Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I <sup>2</sup> C mode) (1/2)
		164, 165	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I <sup>2</sup> C mode) (2/2)
		166	Modification of table in 3.5.2 Serial interface IICA
		166	Modification of IICA serial transfer timing
		167	Addition of table in 3.6.1 A/D converter characteristics
		167, 168	Modification of table and notes 3 and 4 in 3.6.1 (1)
		169	Modification of description in 3.6.1 (2)
		170	Modification of description and note 3 in 3.6.1 (3)
		171	Modification of description and notes 3 and 4 in 3.6.1 (4)
		172	Modification of table and note in 3.6.3 POR circuit characteristics
		173	Modification of table of LVD Detection Voltage of Interrupt & Reset Mode
		173	Modification from Supply Voltage Rise Time to 3.6.5 Power supply voltage rising slope characteristics
		174	Modification of 3.9 Dedicated Flash Memory Programmer Communication (UART)
		175	Modification of table, figure, and remark in 3.10 Timing Specs for Switching Flash Memory Programming Modes
3.10	Nov 15, 2013	123	Caution 4 added.
		125	Note for operating ambient temperature in 3.1 Absolute Maximum Ratings deleted.
3.30	Mar 31, 2016		Modification of the position of the index mark in 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch) of 1.3.3 25-pin products
			Modification of power supply voltage in 1.6 Outline of Functions [20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products]
			Modification of power supply voltage in 1.6 Outline of Functions [40-pin, 44-pin, 48-pin, 52-pin, 64-pin products]
			Modification of power supply voltage in 1.6 Outline of Functions [80-pin, 100-pin, 128-pin products]
			$\overline{\text{ACK}}$ corrected to ACK
			$\overline{\text{ACK}}$ corrected to ACK

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