What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100fadfp-50

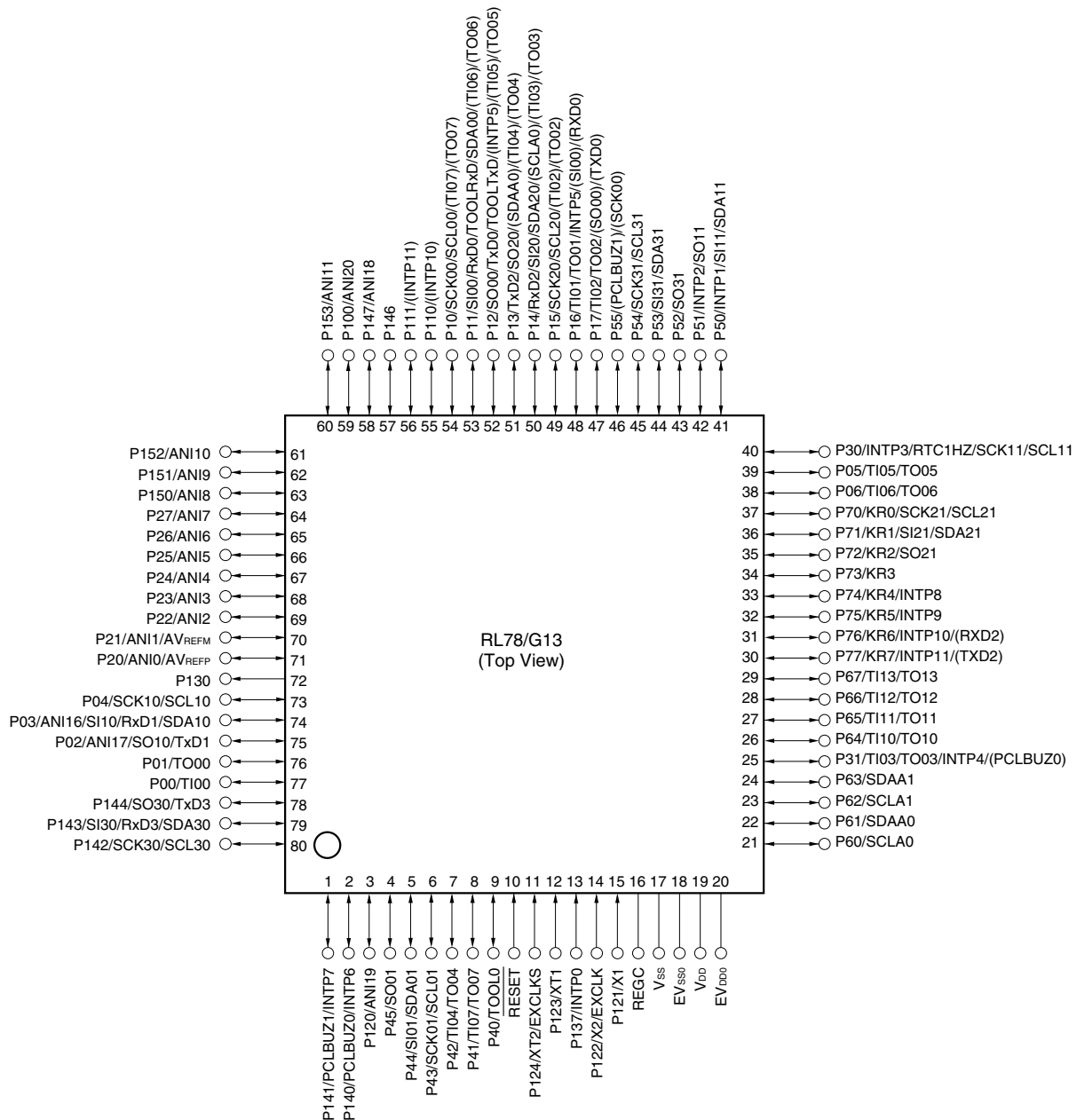**Table 1-1. List of Ordering Part Numbers**

<div align="right">(8/12)</div>

Pin count	Package	Data flash	Fields of Application [Note]	Ordering Part Number
64 pins	64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)	Mounted	A	R5F100LCAFA#V0, R5F100LDAFA#V0, R5F100LEAFA#V0, R5F100LFAFA#V0, R5F100LGAFA#V0, R5F100LHAFA#V0, R5F100LJAFA#V0, R5F100LKAFA#V0, R5F100LLAFA#V0
			D	R5F100LCAFA#X0, R5F100LDAFA#X0, R5F100LEAFA#X0, R5F100LFAFA#X0, R5F100LGAFA#X0, R5F100LHAFA#X0, R5F100LJAFA#X0, R5F100LKAFA#X0, R5F100LLAFA#X0
				R5F100LCDFA#V0, R5F100LDDFA#V0, R5F100LEDFA#V0, R5F100LFDFA#V0, R5F100LGDFA#V0, R5F100LHDFA#V0, R5F100LJDFA#V0, R5F100LKDFA#V0, R5F100LLDFA#V0
			G	R5F100LCDFA#X0, R5F100LDDFA#X0, R5F100LEDFA#X0, R5F100LFDFA#X0, R5F100LGDFA#X0, R5F100LHDFA#X0, R5F100LJDFA#X0, R5F100LKDFA#X0, R5F100LLDFA#X0
				R5F100LCGFA#V0, R5F100LDGFA#V0, R5F100LEGFA#V0, R5F100LFGFA#V0
				R5F100LCGFA#X0, R5F100LDGFA#X0, R5F100LEGFA#X0, R5F100LFGFA#X0
				R5F100LGGFA#V0, R5F100LHGFA#V0, R5F100LJGFA#V0
				R5F100LGGFA#X0, R5F100LHGFA#X0, R5F100LJGFA#X0
		Not mounted	A	R5F101LCAFA#V0, R5F101LDAFA#V0, R5F101LEAFA#V0, R5F101LFAFA#V0, R5F101LGAFA#V0, R5F101LHAFA#V0, R5F101LJAFA#V0, R5F101LKAFA#V0, R5F101LLAFA#V0
			D	R5F101LCAFA#X0, R5F101LDAFA#X0, R5F101LEAFA#X0, R5F101LFAFA#X0, R5F101LGAFA#X0, R5F101LHAFA#X0, R5F101LJAFA#X0, R5F101LKAFA#X0, R5F101LLAFA#X0
				R5F101LCDFA#V0, R5F101LDDFA#V0, R5F101LEDFA#V0, R5F101LFDFA#V0, R5F101LGDFA#V0, R5F101LHDFA#V0, R5F101LJDFA#V0, R5F101LKDFA#V0, R5F101LLDFA#V0
				R5F101LCDFA#X0, R5F101LDDFA#X0, R5F101LEDFA#X0, R5F101LFDFA#X0, R5F101LGDFA#X0, R5F101LHDFA#X0, R5F101LJDFA#X0, R5F101LKDFA#X0, R5F101LLDFA#X0

Note   For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.12 80-pin products

- 80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)

Top pins (60 → 41):

- 60 P153/ANI11
- 59 P100/ANI20
- 58 P147/ANI18
- 57 P146
- 56 P111/(INTP11)
- 55 P110/(INTP10)
- 54 P10/SCK00/SCL00/(TI07)/(TO07)
- 53 P11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
- 52 P12/SO00/TxD0/TOOLTxD/(INTP5)/(TI05)/(TO05)
- 51 P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
- 50 P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
- 49 P15/SCK20/SCL20/(TI02)/(TO02)
- 48 P16/TI01/TO01/INTP5/(SI00)/(RXD0)
- 47 P17/TI02/TO02/(SO00)/(TXD0)
- 46 P55/(PCLBUZ1)/(SCK00)
- 45 P54/SCK31/SCL31
- 44 P53/SI31/SDA31
- 43 P52/SO31
- 42 P51/INTP2/SO11
- 41 P50/INTP1/SI11/SDA11

Left pins (61 → 80):

- 61 P152/ANI10
- 62 P151/ANI9
- 63 P150/ANI8
- 64 P27/ANI7
- 65 P26/ANI6
- 66 P25/ANI5
- 67 P24/ANI4
- 68 P23/ANI3
- 69 P22/ANI2
- 70 P21/ANI1/AV$_{REFM}$
- 71 P20/ANI0/AV$_{REFP}$
- 72 P130
- 73 P04/SCK10/SCL10
- 74 P03/ANI16/SI10/RxD1/SDA10
- 75 P02/ANI17/SO10/TxD1
- 76 P01/TO00
- 77 P00/TI00
- 78 P144/SO30/TxD3
- 79 P143/SI30/RxD3/SDA30
- 80 P142/SCK30/SCL30

RL78/G13
(Top View)

Right pins (40 → 21):

- 40 P30/INTP3/RTC1HZ/SCK11/SCL11
- 39 P05/TI05/TO05
- 38 P06/TI06/TO06
- 37 P70/KR0/SCK21/SCL21
- 36 P71/KR1/SI21/SDA21
- 35 P72/KR2/SO21
- 34 P73/KR3
- 33 P74/KR4/INTP8
- 32 P75/KR5/INTP9
- 31 P76/KR6/INTP10/(RXD2)
- 30 P77/KR7/INTP11/(TXD2)
- 29 P67/TI13/TO13
- 28 P66/TI12/TO12
- 27 P65/TI11/TO11
- 26 P64/TI10/TO10
- 25 P31/TI03/TO03/INTP4/(PCLBUZ0)
- 24 P63/SDAA1
- 23 P62/SCLA1
- 22 P61/SDAA0
- 21 P60/SCLA0

Bottom pins (1 → 20):

- 1 P141/PCLBUZ1/INTP7
- 2 P140/PCLBUZ0/INTP6
- 3 P120/ANI19
- 4 P45/SO01
- 5 P44/SI01/SDA01
- 6 P43/SCK01/SCL01
- 7 P42/TI04/TO04
- 8 P41/TI07/TO07
- 9 P40/TOOL0
- 10 RESET
- 11 P124/XT2/EXCLKS
- 12 P123/XT1
- 13 P137/INTP0
- 14 P122/X2/EXCLK
- 15 P121/X1
- 16 REGC
- 17 V$_{SS}$
- 18 EV$_{SS0}$
- 19 V$_{DD}$
- 20 EV$_{DD0}$

Cautions 1. Make EV$_{SS0}$ pin the same potential as V$_{SS}$ pin.

2. Make V$_{DD}$ pin the potential that is higher than EV$_{DD0}$ pin.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V$_{DD}$ and EV$_{DD0}$ pins and connect the V$_{SS}$ and EV$_{SS0}$ pins to separate ground lines.

3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.14 128-pin products
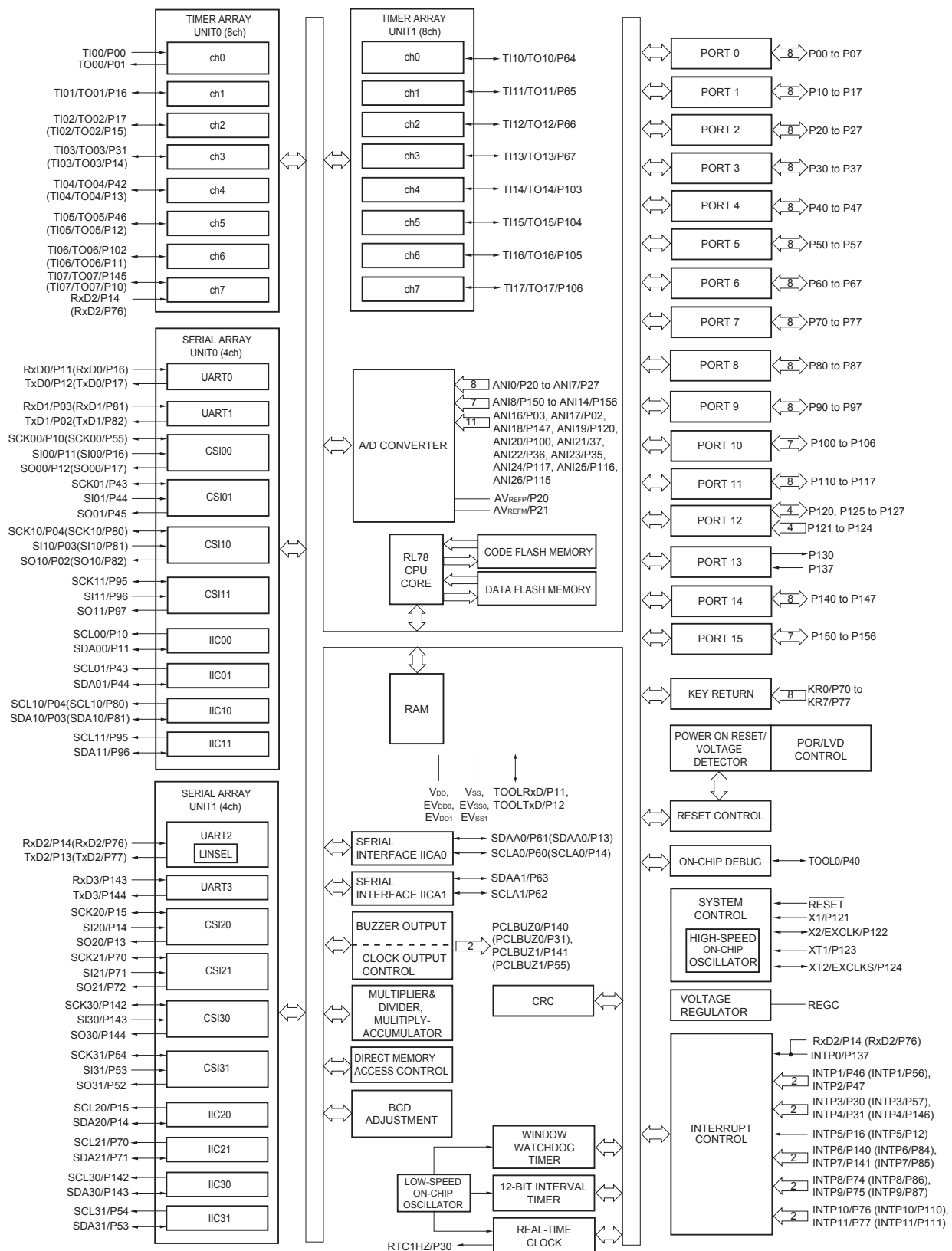
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.6　Outline of Functions

[20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products]

Caution　This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		20-pin		24-pin		25-pin		30-pin		32-pin		36-pin	
		R5F1006x	R5F1016x	R5F1007x	R5F1017x	R5F1008x	R5F1018x	R5F100Ax	R5F101Ax	R5F100Bx	R5F101Bx	R5F100Cx	R5F101Cx
Code flash memory (KB)		16 to 64		16 to 64		16 to 64		16 to 128		16 to 128		16 to 128	
Data flash memory (KB)		4	–	4	–	4	–	4 to 8	–	4 to 8	–	4 to 8	–
RAM (KB)		2 to 4 [Note1]		2 to 4 [Note1]		2 to 4 [Note1]		2 to 12 [Note1]		2 to 12 [Note1]		2 to 12 [Note1]	
Address space		1 MB											
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)											
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)											
Subsystem clock		–											
Low-speed on-chip oscillator		15 kHz (TYP.)											
General-purpose registers		(8-bit register × 8) × 4 banks											
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)											
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)											
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.											
I/O port	Total	16		20		21		26		28		32	
	CMOS I/O	13 (N-ch O.D. I/O [V_{DD} withstand voltage]: 5)		15 (N-ch O.D. I/O [V_{DD} withstand voltage]: 6)		15 (N-ch O.D. I/O [V_{DD} withstand voltage]: 6)		21 (N-ch O.D. I/O [V_{DD} withstand voltage]: 9)		22 (N-ch O.D. I/O [V_{DD} withstand voltage]: 9)		26 (N-ch O.D. I/O [V_{DD} withstand voltage]: 10)	
	CMOS input	3		3		3		3		3		3	
	CMOS output	–		–		1		–		–		–	
	N-ch O.D. I/O (withstand voltage: 6 V)	–		2		2		2		3		3	
Timer	16-bit timer	8 channels											
	Watchdog timer	1 channel											
	Real-time clock (RTC)	1 channel [Note 2]											
	12-bit interval timer (IT)	1 channel											
	Timer output	3 channels (PWM outputs: 2 [Note 3])		4 channels (PWM outputs: 3 [Note 3])				4 channels (PWM outputs: 3 [Note 3]), 8 channels (PWM outputs: 7 [Note 3]) [Note 4]					
	RTC output	–											

Notes　1.　The flash library uses RAM in self-programming and rewriting of the data flash memory.
　　　　　The target products and start address of the RAM areas used by the flash library are shown below.
　　　　　　　R5F100xD, R5F101xD (x = 6 to 8, A to C):　Start address FF300H
　　　　　　　R5F100xE, R5F101xE (x = 6 to 8, A to C):　Start address FEF00H
　　　　　For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.
　　　　2.　Only the constant-period interrupt function when the low-speed on-chip oscillator clock (f_{IL}) is selected

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	−70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	−100	mA
	I_{OH2}	Per pin	P20 to P27, P150 to P156	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
	I_{OL2}	Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			−65 to +150	°C

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

(TA = −40 to +85°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (fx)[Note]	Ceramic resonator/ crystal resonator	2.7 V ≤ VDD ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ VDD < 2.7 V	1.0		16.0	MHz
		1.8 V ≤ VDD < 2.4 V	1.0		8.0	MHz
		1.6 V ≤ VDD < 1.8 V	1.0		4.0	MHz
XT1 clock oscillation frequency (fx)[Note]	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator**.

2.2.2 On-chip oscillator characteristics

(TA = −40 to +85°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency [Notes 1, 2]	fIH			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		−20 to +85 °C	1.8 V ≤ VDD ≤ 5.5 V	−1.0		+1.0	%
			1.6 V ≤ VDD < 1.8 V	−5.0		+5.0	%
		−40 to −20 °C	1.8 V ≤ VDD ≤ 5.5 V	−1.5		+1.5	%
			1.6 V ≤ VDD < 1.8 V	−5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	fIL				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				−15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (4/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V$_{OH1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −10.0 mA	EV$_{DD0}$ − 1.5			V
			4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −3.0 mA	EV$_{DD0}$ − 0.7			V
			2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −2.0 mA	EV$_{DD0}$ − 0.6			V
			1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −1.5 mA	EV$_{DD0}$ − 0.5			V
			1.6 V ≤ EV$_{DD0}$ < 5.5 V, I$_{OH1}$ = −1.0 mA	EV$_{DD0}$ − 0.5			V
	V$_{OH2}$	P20 to P27, P150 to P156	1.6 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OH2}$ = −100 μA	V$_{DD}$ − 0.5			V
Output voltage, low	V$_{OL1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 20 mA			1.3	V
			4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 8.5 mA			0.7	V
			2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 3.0 mA			0.6	V
			2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 1.5 mA			0.4	V
			1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 0.6 mA			0.4	V
			1.6 V ≤ EV$_{DD0}$ < 5.5 V, I$_{OL1}$ = 0.3 mA			0.4	V
	V$_{OL2}$	P20 to P27, P150 to P156	1.6 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL2}$ = 400 μA			0.4	V
	V$_{OL3}$	P60 to P63	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 15.0 mA			2.0	V
			4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 5.0 mA			0.4	V
			2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 3.0 mA			0.4	V
			1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 2.0 mA			0.4	V
			1.6 V ≤ EV$_{DD0}$ < 5.5 V, I$_{OL3}$ = 1.0 mA			0.4	V

Caution **P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V $\leq$ EV$_{DD0}$ < 4.0 V and 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

*　This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

5. Use it with EV$_{DD0}$ $\geq$ V$_b$.

6. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V $\leq$ EV$_{DD0}$ < 3.3 V and 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

*　This value is the theoretical value of the relative difference between the transmission and reception sides.

7. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution　Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V$_{DD}$ tolerance (When 20- to 52-pin products)/EV$_{DD}$ tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)
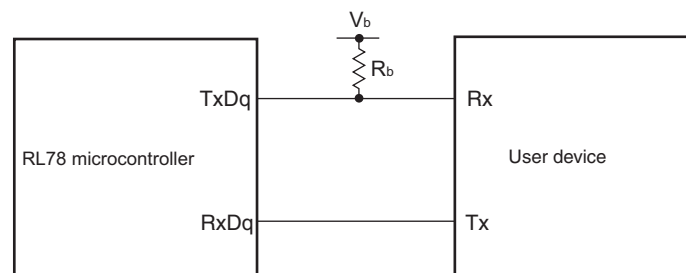
(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)

(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) [Note 1]	t$_{SIK1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	110		110		110		ns
SIp hold time (from SCKp↓) [Note 1]	t$_{KSI1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output [Note 1]	t$_{KSO1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ		25		25		25	ns

Notes 1. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. Use it with EV$_{DD0}$ ≥ V$_b$.

Caution **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V$_{DD}$ tolerance (When 20- to 52-pin products)/EV$_{DD}$ tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

(Remarks are listed on the next page.)

(9) Communication at different potential (1.8 V, 2.5 V, 3 V)　(CSI mode) (slave mode, SCKp... external clock input)

(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (1/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time [Note 1]	t$_{KCY2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V	24 MHz < f$_{MCK}$	14/ f$_{MCK}$		—		—		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	12/ f$_{MCK}$		—		—		ns
			8 MHz < f$_{MCK}$ ≤ 20 MHz	10/ f$_{MCK}$		—		—		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	8/f$_{MCK}$		16/ f$_{MCK}$		—		ns
			f$_{MCK}$ ≤ 4 MHz	6/f$_{MCK}$		10/ f$_{MCK}$		10/ f$_{MCK}$		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V	24 MHz < f$_{MCK}$	20/ f$_{MCK}$		—		—		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	16/ f$_{MCK}$		—		—		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	14/ f$_{MCK}$		—		—		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	12/ f$_{MCK}$		—		—		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	8/f$_{MCK}$		16/ f$_{MCK}$		—		ns
			f$_{MCK}$ ≤ 4 MHz	6/f$_{MCK}$		10/ f$_{MCK}$		10/ f$_{MCK}$		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]	24 MHz < f$_{MCK}$	48/ f$_{MCK}$		—		—		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	36/ f$_{MCK}$		—		—		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	32/ f$_{MCK}$		—		—		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	26/ f$_{MCK}$		—		—		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	16/ f$_{MCK}$		16/ f$_{MCK}$		—		ns
			f$_{MCK}$ ≤ 4 MHz	10/ f$_{MCK}$		10/ f$_{MCK}$		10/ f$_{MCK}$		ns

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

(2)　I²C fast mode

(TA = −40 to +85°C, 1.6 V ≤ EV_DD0 = EV_DD1 ≤ V_DD ≤ 5.5 V, V_SS = EV_SS0 = EV_SS1 = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: $f_{CLK} \geq 3.5$ MHz	2.7 V ≤ EV_DD0 ≤ 5.5 V	0	400	0	400	0	400	kHz
			1.8 V ≤ EV_DD0 ≤ 5.5 V	0	400	0	400	0	400	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_DD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV_DD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time[Note 1]	$t_{HD:STA}$	2.7 V ≤ EV_DD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV_DD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ EV_DD0 ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V ≤ EV_DD0 ≤ 5.5 V		1.3		1.3		1.3		μs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ EV_DD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV_DD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_DD0 ≤ 5.5 V		100		100		100		μs
		1.8 V ≤ EV_DD0 ≤ 5.5 V		100		100		100		μs
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	2.7 V ≤ EV_DD0 ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
		1.8 V ≤ EV_DD0 ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_DD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV_DD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Bus-free time	t_{BUF}	2.7 V ≤ EV_DD0 ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V ≤ EV_DD0 ≤ 5.5 V		1.3		1.3		1.3		μs

Notes　**1.**　The first clock pulse is generated after this period when the start/restart condition is detected.

<R>　　　　**2.**　The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution　**The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_OH1, I_OL1, V_OH1, V_OL1) must satisfy the values in the redirect destination.**

Remark　The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

　　　　Fast mode:　　　　C_b = 320 pF, R_b = 1.1 kΩ

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (−) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26

(T$_A$ = −40 to +85°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V, Reference voltage (+) = V$_{BGR}$ $^{Note\,3}$, Reference voltage (−) = AV$_{REFM}$ = 0 V $^{Note\,4}$, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t$_{CONV}$	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error$^{Notes\,1,\,2}$	E$_{ZS}$	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
Integral linearity error$^{Note\,1}$	ILE	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±2.0	LSB
Differential linearity error$^{Note\,1}$	DLE	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±1.0	LSB
Analog input voltage	V$_{AIN}$			0		V$_{BGR}$ $^{Note\,3}$	V

Notes **1.** Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (−) = V$_{SS}$, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (−) = AV$_{REFM}$.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.

2.8 Flash Memory Programming Characteristics

(T$_A$ = –40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f$_{CLK}$	1.8 V ≤ V$_{DD}$ ≤ 5.5 V	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C$_{erwr}$	Retained for 20 years T$_A$ = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 years T$_A$ = 25°C		1,000,000		
		Retained for 5 years T$_A$ = 85°C	100,000			
		Retained for 20 years T$_A$ = 85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

    The retaining years are until next rewrite after the rewrite.

  2. When using flash memory programmer and Renesas Electronics self programming library

  3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

Remark The electrical characteristics of the products G: Industrial applications (T$_A$ = -40 to +105°C) are different from those of the products "A: Consumer applications, and D: Industrial applications". For details, refer to **3.1** to **3.10**.

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T$_A$ = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V$_{DD}$		−0.5 to +6.5	V
	EV$_{DD0}$, EV$_{DD1}$	EV$_{DD0}$ = EV$_{DD1}$	−0.5 to +6.5	V
	EV$_{SS0}$, EV$_{SS1}$	EV$_{SS0}$ = EV$_{SS1}$	−0.5 to +0.3	V
REGC pin input voltage	V$_{IREGC}$	REGC	−0.3 to +2.8 and −0.3 to V$_{DD}$ +0.3[Note 1]	V
Input voltage	V$_{I1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	−0.3 to EV$_{DD0}$ +0.3 and −0.3 to V$_{DD}$ +0.3[Note 2]	V
	V$_{I2}$	P60 to P63 (N-ch open-drain)	−0.3 to +6.5	V
	V$_{I3}$	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, RESET	−0.3 to V$_{DD}$ +0.3[Note 2]	V
Output voltage	V$_{O1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−0.3 to EV$_{DD0}$ +0.3 and −0.3 to V$_{DD}$ +0.3[Note 2]	V
	V$_{O2}$	P20 to P27, P150 to P156	−0.3 to V$_{DD}$ +0.3[Note 2]	V
Analog input voltage	V$_{AI1}$	ANI16 to ANI26	−0.3 to EV$_{DD0}$ +0.3 and −0.3 to AV$_{REF}$(+) +0.3[Notes 2, 3]	V
	V$_{AI2}$	ANI0 to ANI14	−0.3 to V$_{DD}$ +0.3 and −0.3 to AV$_{REF}$(+) +0.3[Notes 2, 3]	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

    2. Must be 6.5 V or lower.

    3. Do not exceed AV$_{REF}$(+) + 0.3 V in case of A/D conversion target pin.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

    2. AV$_{REF}$ (+) : + side reference voltage of the A/D converter.

    3. V$_{SS}$: Reference voltage

(T_A = −40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/5)

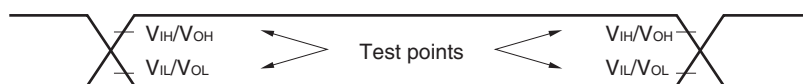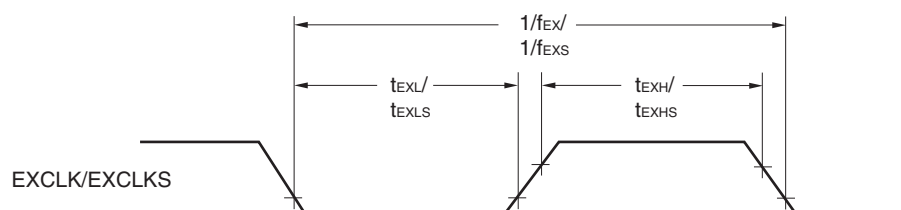| Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147				8.5 [Note 2]	mA
		Per pin for P60 to P63				15.0 [Note 2]	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			40.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			15.0	mA
			2.4 V ≤ EV_{DD0} < 2.7 V			9.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			40.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			35.0	mA
			2,4 V ≤ EV_{DD0} < 2.7 V			20.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])				80.0	mA
	I_{OL2}	Per pin for P20 to P27, P150 to P156				0.4 [Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	2,4 V ≤ V_{DD} ≤ 5.5 V			5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0}, EV_{SS1} and V_{SS} pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (5/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I$_{LIH1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V$_I$ = EV$_{DD0}$			1	μA
	I$_{LIH2}$	P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$	V$_I$ = V$_{DD}$			1	μA
	I$_{LIH3}$	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V$_I$ = V$_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I$_{LIL1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V$_I$ = EV$_{SS0}$				−1	μA
	I$_{LIL2}$	P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$	V$_I$ = V$_{SS}$				−1	μA
	I$_{LIL3}$	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V$_I$ = V$_{SS}$	In input port or external clock input			−1	μA
				In resonator connection			−10	μA
On-chip pll-up resistance	R$_U$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V$_I$ = EV$_{SS0}$, In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Minimum Instruction Execution Time during Main System Clock Operation

T$_{CY}$ vs V$_{DD}$ (HS (high-speed main) mode)

— When the high-speed on-chip oscillator clock is selected
--- During self programming
—·— When high-speed system clock is selected

AC Timing Test Points

V$_{IH}$/V$_{OH}$ Test points   V$_{IH}$/V$_{OH}$
V$_{IL}$/V$_{OL}$ V$_{IL}$/V$_{OL}$
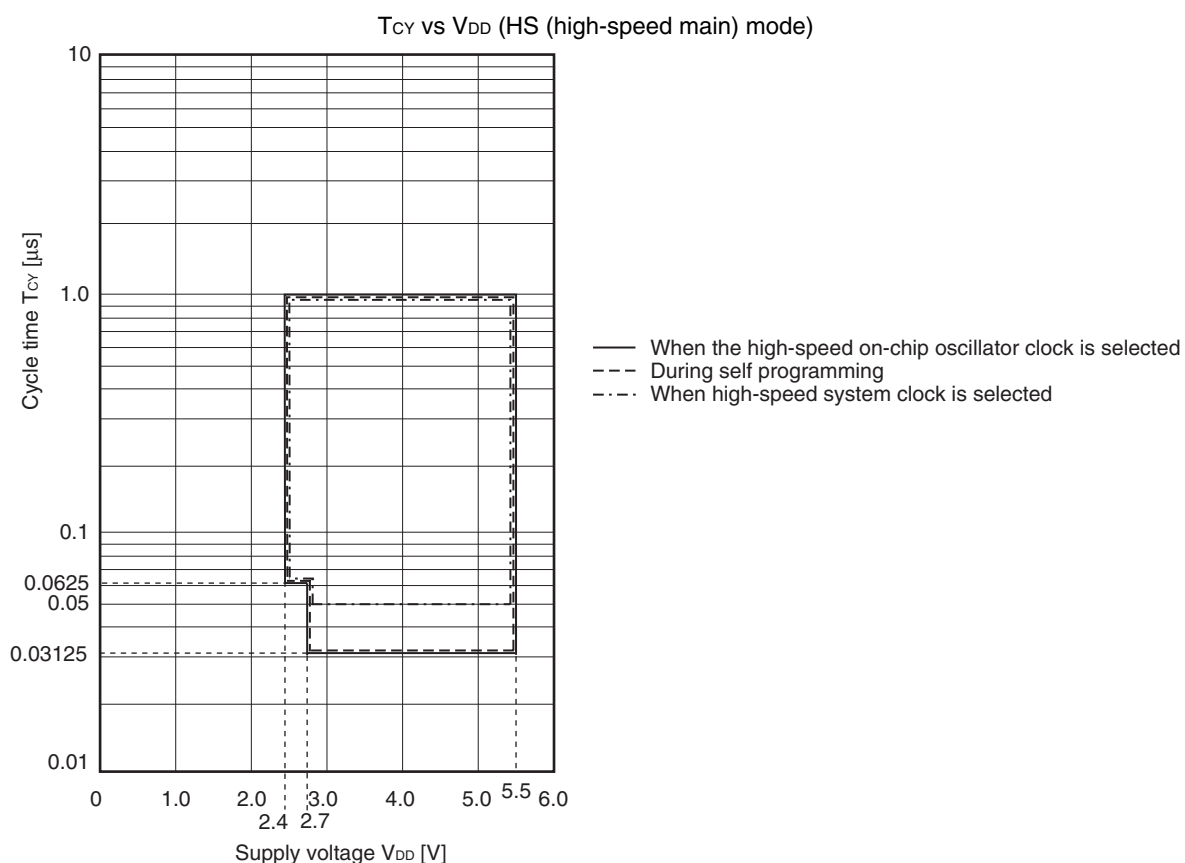
External System Clock Timing

1/f$_{EX}$/
1/f$_{EXS}$

t$_{EXL}$/   t$_{EXH}$/
t$_{EXLS}$ t$_{EXHS}$

EXCLK/EXCLKS

UART mode bit width (during communication at different potential) (reference)
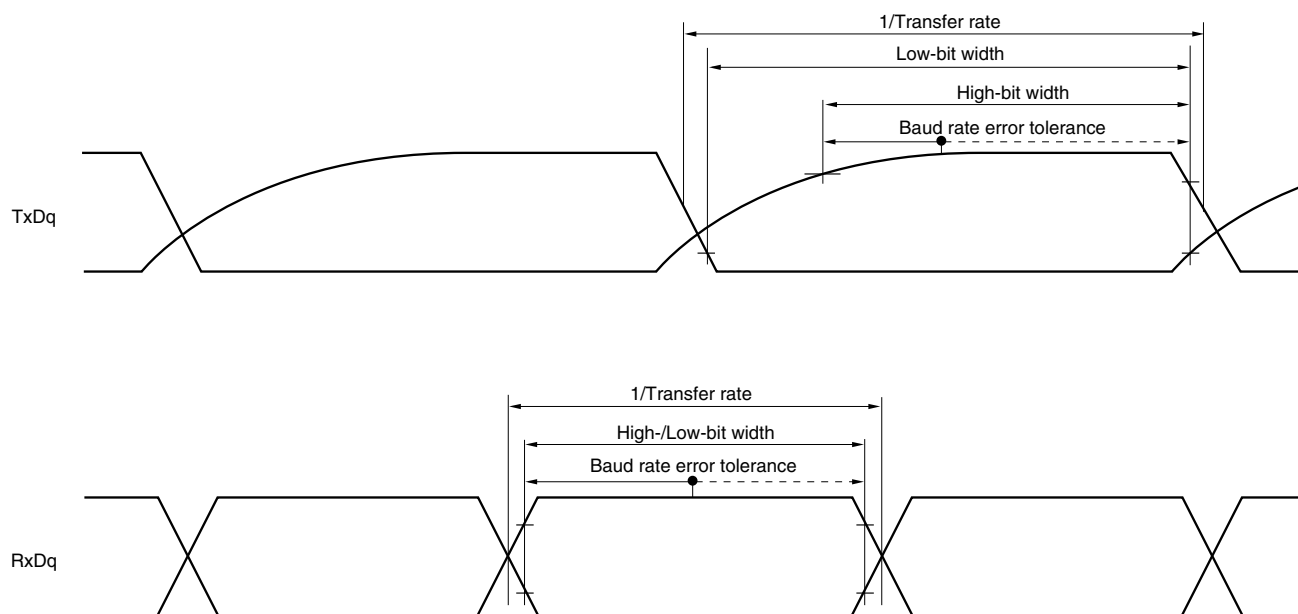
Remarks **1.** R$_b$[Ω]:Communication line (TxDq) pull-up resistance,

　　　　 C$_b$[F]: Communication line (TxDq) load capacitance, V$_b$[V]: Communication line voltage

　　　　 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

　　　　 3. f$_{MCK}$: Serial array unit operation clock frequency

　　　　 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

　　　　 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

　　　　 4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection

　　　　 register (PIOR) is 1.

(8)　Communication at different potential (1.8 V, 2.5 V, 3 V)　(simplified I^{2}C mode) (1/2)

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f$_{SCL}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		400 [Note 1]	kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		400 [Note 1]	kHz
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ		100 [Note 1]	kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ		100 [Note 1]	kHz
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ		100 [Note 1]	kHz
Hold time when SCLr = "L"	t$_{LOW}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1200		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1200		ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	4600		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	4600		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	4650		ns
Hold time when SCLr = "H"	t$_{HIGH}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	620		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	500		ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	2700		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	2400		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	1830		ns

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

4.11 64-pin Products

R5F100LCAFA, R5F100LDAFA, R5F100LEAFA, R5F100LFAFA, R5F100LGAFA, R5F100LHAFA, R5F100LJAFA,
R5F100LKAFA, R5F100LLAFA
R5F101LCAFA, R5F101LDAFA, R5F101LEAFA, R5F101LFAFA, R5F101LGAFA, R5F101LHAFA, R5F101LJAFA,
R5F101LKAFA, R5F101LLAFA
R5F100LCDFA, R5F100LDDFA, R5F100LEDFA, R5F100LFDFA, R5F100LGDFA, R5F100LHDFA, R5F100LJDFA,
R5F100LKDFA, R5F100LLDFA
R5F101LCDFA, R5F101LDDFA, R5F101LEDFA, R5F101LFDFA, R5F101LGDFA, R5F101LHDFA, R5F101LJDFA,
R5F101LKDFA, R5F101LLDFA
R5F100LCGFA, R5F100LDGFA, R5F100LEGFA, R5F100LFGFA, R5F100LGGFA, R5F100LHGFA,
R5F100LJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51

detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.32^{+0.08}_{-0.07}$
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
e	0.65
x	0.13
y	0.10
ZD	1.125
ZE	1.125
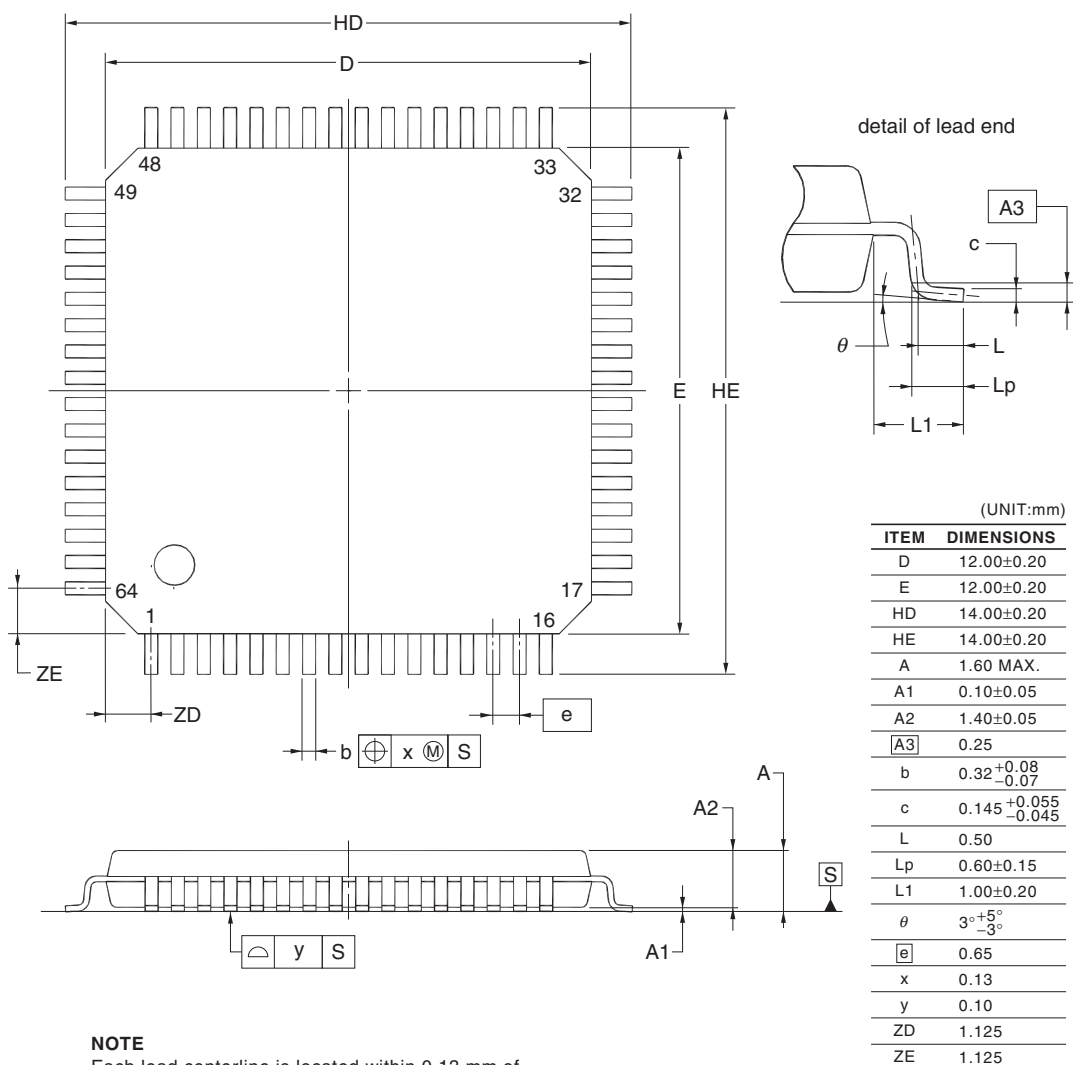
NOTE
Each lead centerline is located within 0.13 mm of
its true position at maximum material condition.