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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I ² C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 31 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 10x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LQFP |
| Supplier Device Package | 44-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100fcafp-v0 |

Table 1-1. List of Ordering Part Numbers

(3/12)

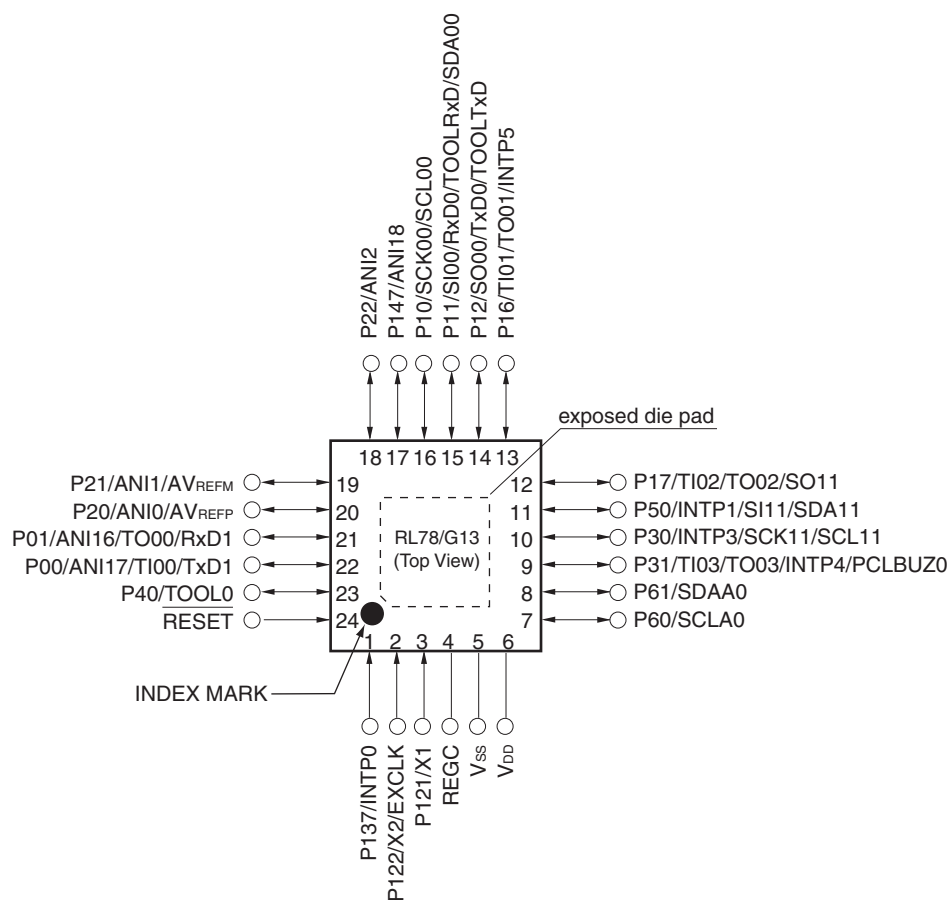
| Pin count | Package | Data flash | Fields of Application Note | Ordering Part Number |
|-----------|--|-------------|-------------------------------|--|
| 36 pins | 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch) | Mounted | A | R5F100CAALA#U0, R5F100CCALA#U0, R5F100CDALA#U0, R5F100CEALA#U0, R5F100CFALA#U0, R5F100CGALA#U0 R5F100CAALA#W0, R5F100CCALA#W0, R5F100CDALA#W0, R5F100CEALA#W0, R5F100CFALA#W0, R5F100CGALA#W0 R5F100CAGLA#U0, R5F100CCGLA#U0, R5F100CDGLA#U0, R5F100CEGLA#U0, R5F100CFGLA#U0, R5F100CGGLA#U0 R5F100CAGLA#W0, R5F100CCGLA#W0, R5F100CDGLA#W0, R5F100CEGLA#W0, R5F100CFGLA#W0, R5F100CGGLA#W0 |
| | | Not mounted | A | R5F101CAALA#U0, R5F101CCALA#U0, R5F101CDALA#U0, R5F101CEALA#U0, R5F101CFALA#U0, R5F101CGALA#U0 R5F101CAALA#W0, R5F101CCALA#W0, R5F101CDALA#W0, R5F101CEALA#W0, R5F101CFALA#W0, R5F101CGALA#W0 |
| 40 pins | 40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch) | Mounted | A | R5F100EAANA#U0, R5F100ECANA#U0, R5F100EDANA#U0, R5F100EEANA#U0, R5F100EFANA#U0, R5F100EGANA#U0, R5F100EHANA#U0 R5F100EAANA#W0, R5F100ECANA#W0, R5F100EDANA#W0, R5F100EEANA#W0, R5F100EFANA#W0, R5F100EGANA#W0, R5F100EHANA#W0 R5F100EADNA#U0, R5F100ECDNA#U0, R5F100EDDNA#U0, R5F100EEDNA#U0, R5F100EFDNA#U0, R5F100EGDNA#U0, R5F100EHDNA#U0 R5F100EADNA#W0, R5F100ECDNA#W0, R5F100EDDNA#W0, R5F100EEDNA#W0, R5F100EFDNA#W0, R5F100EGDNA#W0, R5F100EHDNA#W0 R5F100EAGNA#U0, R5F100ECGNA#U0, R5F100EDGNA#U0, R5F100EEGNA#U0, R5F100EFGNA#U0, R5F100EGGNA#U0, R5F100EHGNA#U0 R5F100EAGNA#W0, R5F100ECGNA#W0, R5F100EDGNA#W0, R5F100EEGNA#W0, R5F100EFGNA#W0, R5F100EGGNA#W0, R5F100EHGNA#W0 |
| | | Not mounted | A | R5F101EAANA#U0, R5F101ECANA#U0, R5F101EDANA#U0, R5F101EEANA#U0, R5F101EFANA#U0, R5F101EGANA#U0, R5F101EHANA#U0 R5F101EAANA#W0, R5F101ECANA#W0, R5F101EDANA#W0, R5F101EEANA#W0, R5F101EFANA#W0, R5F101EGANA#W0, R5F101EHANA#W0 R5F101EADNA#U0, R5F101ECDNA#U0, R5F101EDDNA#U0, R5F101EEDNA#U0, R5F101EFDNA#U0, R5F101EGDNA#U0, R5F101EHDNA#U0 R5F101EADNA#W0, R5F101ECDNA#W0, R5F101EDDNA#W0, R5F101EEDNA#W0, R5F101EFDNA#W0, R5F101EGDNA#W0, R5F101EHDNA#W0 |

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.2 24-pin products

- 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)



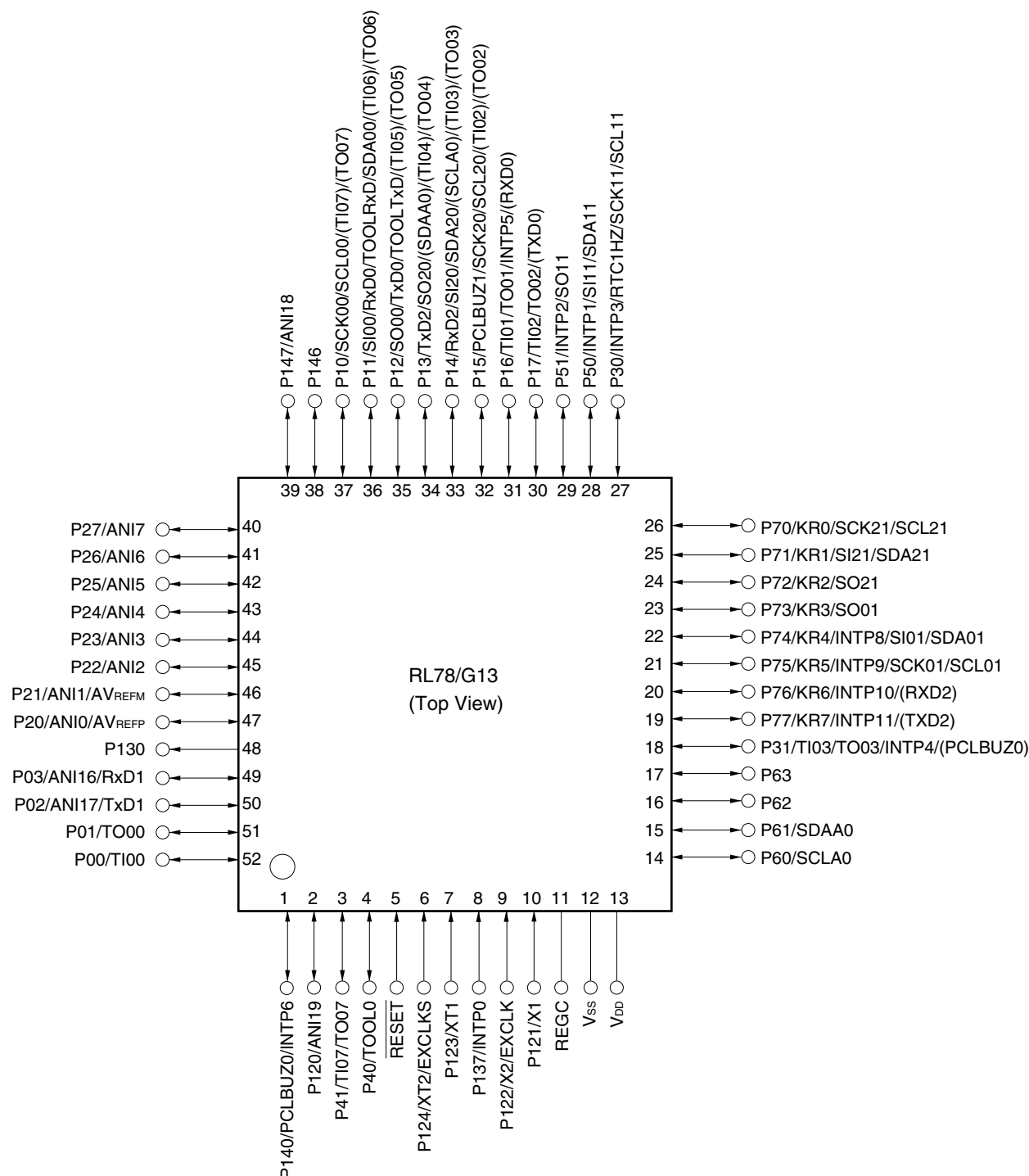
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. It is recommended to connect an exposed die pad to Vss.

1.3.10 52-pin products

- 52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)



Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

- 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

| Parameter | Symbols | Conditions | Ratings | Unit |
|------------------------|---------------------------------------|---|--|------|
| Supply voltage | V _{DD} | | -0.5 to +6.5 | V |
| | EV _{DD0} , EV _{DD1} | EV _{DD0} = EV _{DD1} | -0.5 to +6.5 | V |
| | EV _{SS0} , EV _{SS1} | EV _{SS0} = EV _{SS1} | -0.5 to +0.3 | V |
| REGC pin input voltage | V _{IREGC} | REGC | -0.3 to +2.8 and -0.3 to V _{DD} + 0.3 ^{Note 1} | V |
| Input voltage | V _{I1} | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | -0.3 to EV _{DD0} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2} | V |
| | V _{I2} | P60 to P63 (N-ch open-drain) | -0.3 to +6.5 | V |
| | V _{I3} | P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, RESET | -0.3 to V _{DD} + 0.3 ^{Note 2} | V |
| Output voltage | V _{O1} | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | -0.3 to EV _{DD0} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2} | V |
| | V _{O2} | P20 to P27, P150 to P156 | -0.3 to V _{DD} + 0.3 ^{Note 2} | V |
| Analog input voltage | V _{AI1} | ANI16 to ANI26 | -0.3 to EV _{DD0} + 0.3 and -0.3 to AV _{REF} (+) + 0.3 ^{Notes 2, 3} | V |
| | V _{AI2} | ANI0 to ANI14 | -0.3 to V _{DD} + 0.3 and -0.3 to AV _{REF} (+) + 0.3 ^{Notes 2, 3} | V |

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed AV_{REF}(+) + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. AV_{REF}(+) : + side reference voltage of the A/D converter.

3. V_{SS} : Reference voltage

- Notes**
1. Total current flowing into V_{DD} and EV_{DD0} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 32 MHz
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 16 MHz
LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 8 MHz
LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 4 MHz
 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f_{IH}: High-speed on-chip oscillator clock frequency
3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.
7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.
8. Current flowing only during data flash rewrite.
9. Current flowing only during self programming.
10. For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode**.

- Remarks**
1. f_{IL} : Low-speed on-chip oscillator clock frequency
 2. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 3. f_{CLK} : CPU/peripheral hardware clock frequency
 4. Temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

Note The following conditions are required for low voltage interface when $E_{VDD0} < V_{DD}$

$1.8\text{ V} \leq E_{VDD0} < 2.7\text{ V}$: MIN. 125 ns

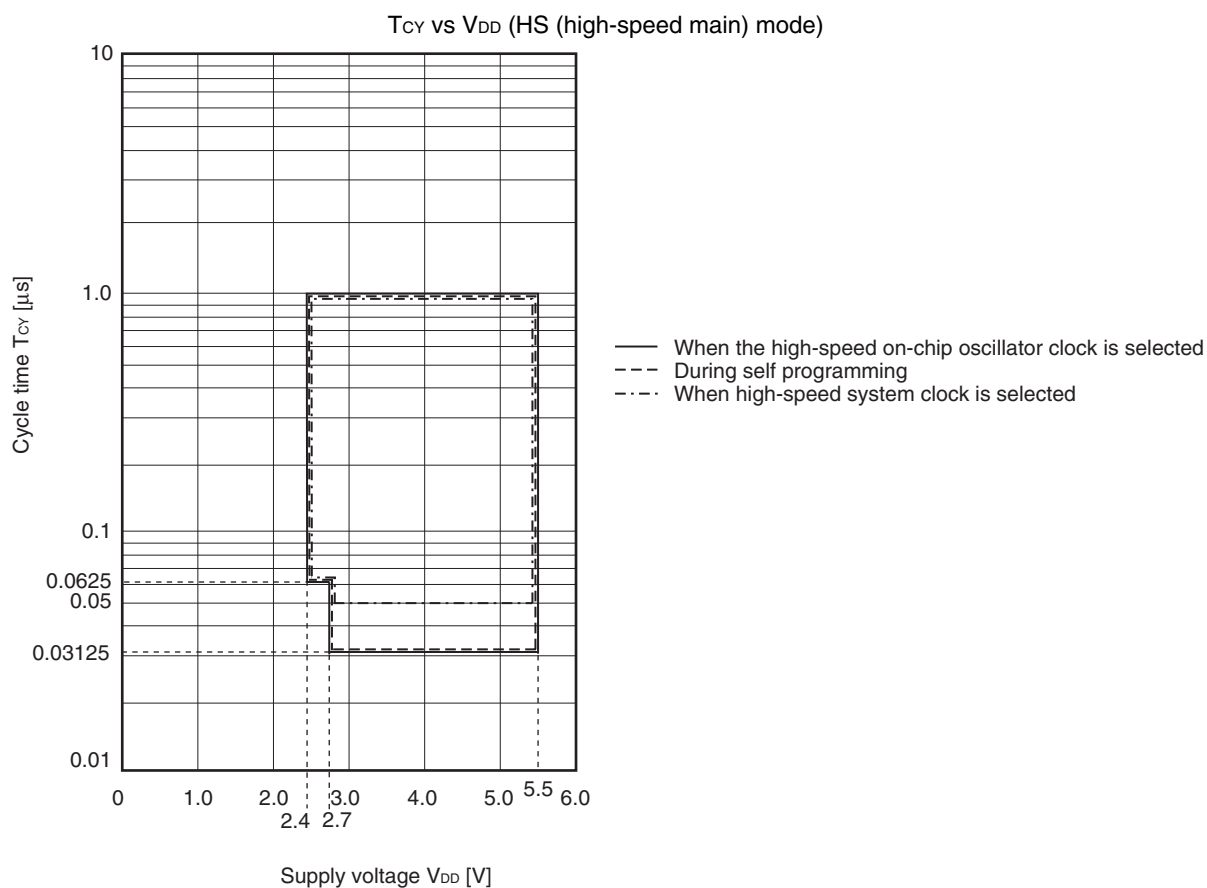
$1.6\text{ V} \leq E_{VDD0} < 1.8\text{ V}$: MIN. 250 ns

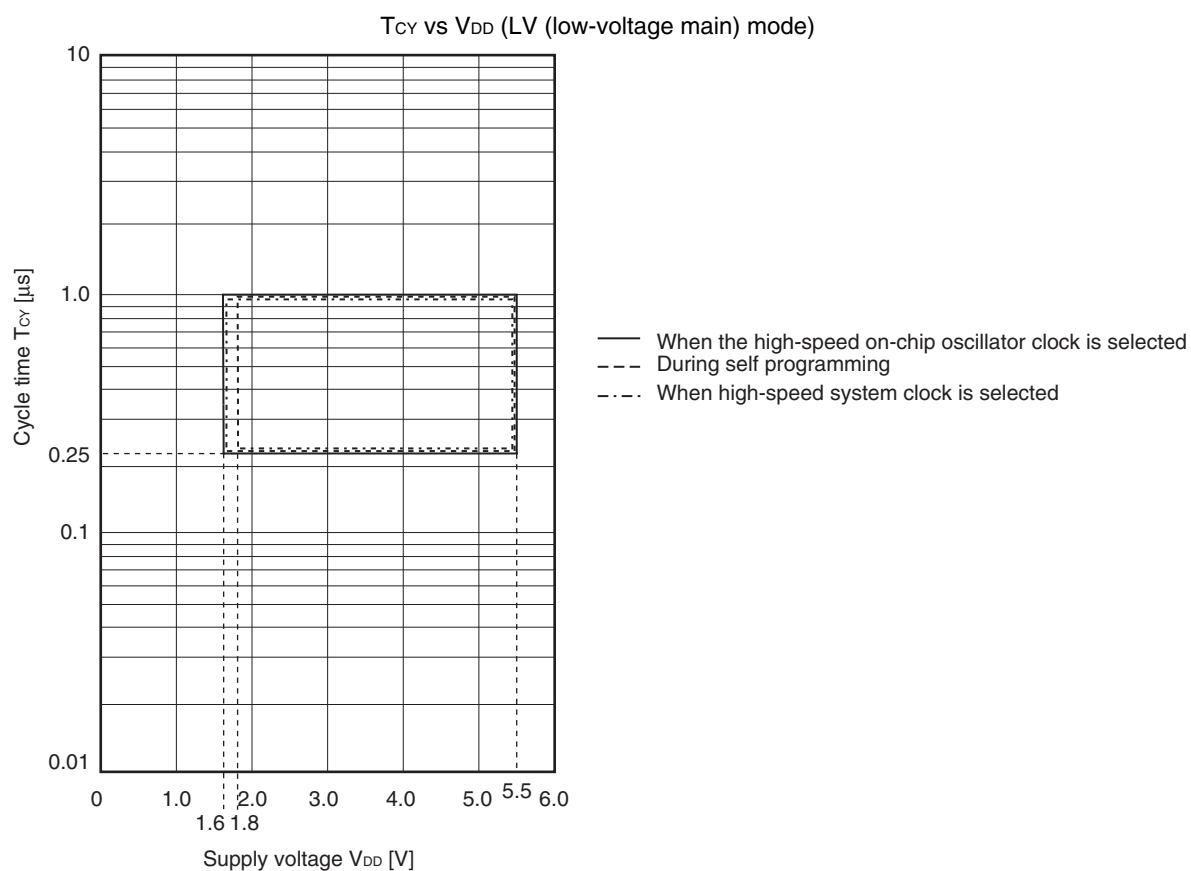
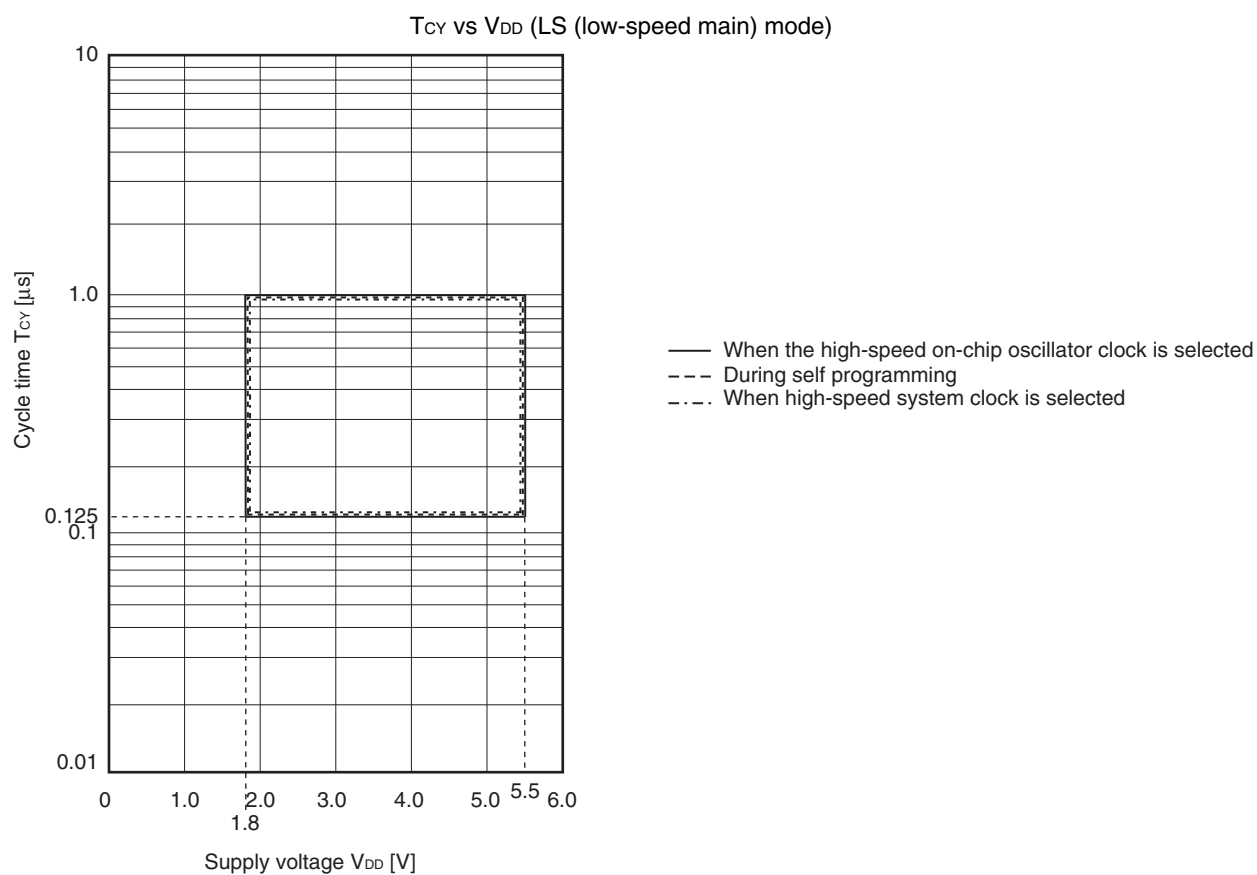
Remark f_{MCK} : Timer array unit operation clock frequency

(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn).

m: Unit number ($m = 0, 1$), n: Channel number ($n = 0$ to 7))

Minimum Instruction Execution Time during Main System Clock Operation





(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|--|-------------------|--|--|--------|------|-------------------|------|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error ^{Note 1} | AINL | 10-bit resolution | 1.8 V ≤ V _{DD} ≤ 5.5 V | | 1.2 | ±7.0 | LSB |
| | | | 1.6 V ≤ V _{DD} ≤ 5.5 V <small>Note 3</small> | | 1.2 | ±10.5 | LSB |
| Conversion time | t _{CONV} | 10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26 | 3.6 V ≤ V _{DD} ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ V _{DD} ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 1.8 V ≤ V _{DD} ≤ 5.5 V | 17 | | 39 | μs |
| | | | 1.6 V ≤ V _{DD} ≤ 5.5 V | 57 | | 95 | μs |
| Conversion time | t _{CONV} | 10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | 3.6 V ≤ V _{DD} ≤ 5.5 V | 2.375 | | 39 | μs |
| | | | 2.7 V ≤ V _{DD} ≤ 5.5 V | 3.5625 | | 39 | μs |
| | | | 2.4 V ≤ V _{DD} ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error ^{Notes 1, 2} | E _{ZS} | 10-bit resolution | 1.8 V ≤ V _{DD} ≤ 5.5 V | | | ±0.60 | %FSR |
| | | | 1.6 V ≤ V _{DD} ≤ 5.5 V <small>Note 3</small> | | | ±0.85 | %FSR |
| Full-scale error ^{Notes 1, 2} | E _{FS} | 10-bit resolution | 1.8 V ≤ V _{DD} ≤ 5.5 V | | | ±0.60 | %FSR |
| | | | 1.6 V ≤ V _{DD} ≤ 5.5 V <small>Note 3</small> | | | ±0.85 | %FSR |
| Integral linearity error ^{Note 1} | ILE | 10-bit resolution | 1.8 V ≤ V _{DD} ≤ 5.5 V | | | ±4.0 | LSB |
| | | | 1.6 V ≤ V _{DD} ≤ 5.5 V <small>Note 3</small> | | | ±6.5 | LSB |
| Differential linearity error ^{Note 1} | DLE | 10-bit resolution | 1.8 V ≤ V _{DD} ≤ 5.5 V | | | ±2.0 | LSB |
| | | | 1.6 V ≤ V _{DD} ≤ 5.5 V <small>Note 3</small> | | | ±2.5 | LSB |
| Analog input voltage | V _{AIN} | ANI0 to ANI14 | 0 | | | V _{DD} | V |
| | | ANI16 to ANI26 | 0 | | | EV _{DD0} | V |
| | | Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode) | V _{BGR} ^{Note 4} | | | | V |
| | | Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode) | V _{TMPS25} ^{Note 4} | | | | V |

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

4. Refer to 2.6.2 Temperature sensor/internal reference voltage characteristics.

2.8 Flash Memory Programming Characteristics

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|-------------------|--|---------|-----------|------|-------|
| CPU/peripheral hardware clock frequency | f _{CLK} | 1.8 V ≤ V _{DD} ≤ 5.5 V | 1 | | 32 | MHz |
| Number of code flash rewrites <small>Notes 1, 2, 3</small> | C _{erwr} | Retained for 20 years T _A = 85°C | 1,000 | | | Times |
| Number of data flash rewrites <small>Notes 1, 2, 3</small> | | Retained for 1 years T _A = 25°C | | 1,000,000 | | |
| | | Retained for 5 years T _A = 85°C | 100,000 | | | |
| | | Retained for 20 years T _A = 85°C | 10,000 | | | |

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

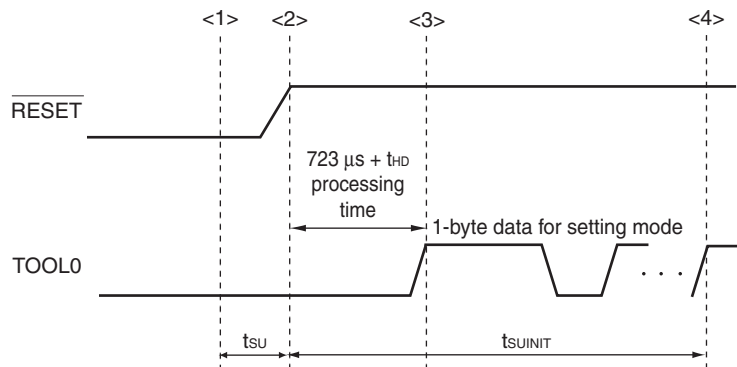
(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------|--------|---------------------------|---------|------|-----------|------|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

2.10 Timing of Entry to Flash Memory Programming Modes

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|---------------------|---|------|------|------|------|
| Time to complete the communication for the initial setting after the external reset is released | t _{SUINIT} | POR and LVD reset must be released before the external reset is released. | | | 100 | ms |
| Time to release the external reset after the TOOL0 pin is set to the low level | t _{SU} | POR and LVD reset must be released before the external reset is released. | 10 | | | μs |
| Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory) | t _{HD} | POR and LVD reset must be released before the external reset is released. | 1 | | | ms |



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

3.3 DC Characteristics

3.3.1 Pin characteristics

(T_A = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$) (1/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|------------------|--|--|------|------------------------|------|
| Output current, high ^{Note 1} | I _{OH1} | Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | | -3.0 ^{Note 2} | mA |
| | | Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty $\leq 70\%$ ^{Note 3}) | $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | | -30.0 | mA |
| | | | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$ | | -10.0 | mA |
| | | | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 2.7\text{ V}$ | | -5.0 | mA |
| | | Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty $\leq 70\%$ ^{Note 3}) | $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | | -30.0 | mA |
| | | | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$ | | -19.0 | mA |
| | | | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 2.7\text{ V}$ | | -10.0 | mA |
| | | Total of all pins (When duty $\leq 70\%$ ^{Note 3}) | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | | -60.0 | mA |
| | I _{OH2} | Per pin for P20 to P27, P150 to P156 | $2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ | | -0.1 ^{Note 2} | mA |
| | | Total of all pins (When duty $\leq 70\%$ ^{Note 3}) | $2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ | | -1.5 | mA |

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0}, EV_{DD1}, V_{DD} pins to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor $\leq 70\%$.

The output current value that has changed to the duty factor $> 70\%$ the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = $(I_{\text{OH}} \times 0.7)/(n \times 0.01)$

<Example> Where $n = 80\%$ and $I_{\text{OH}} = -10.0\text{ mA}$

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

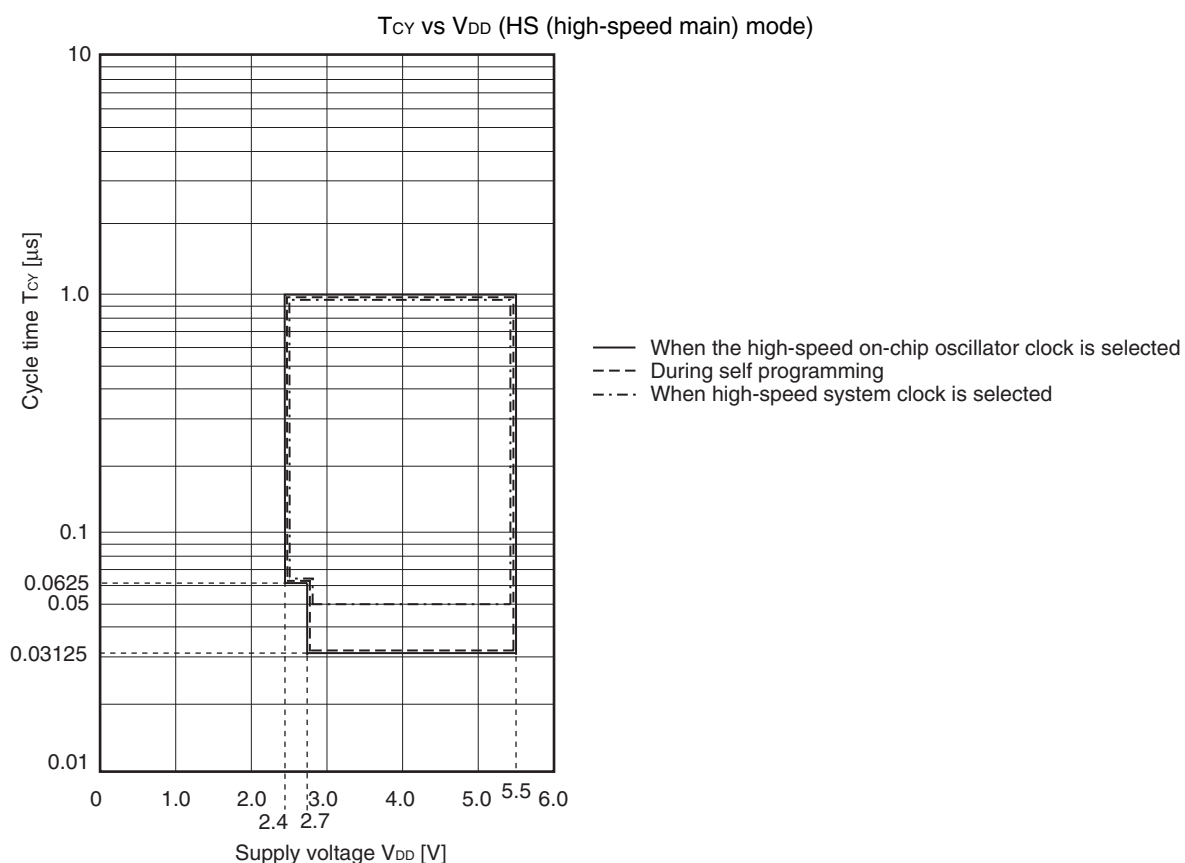
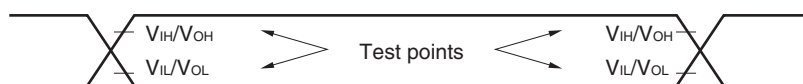
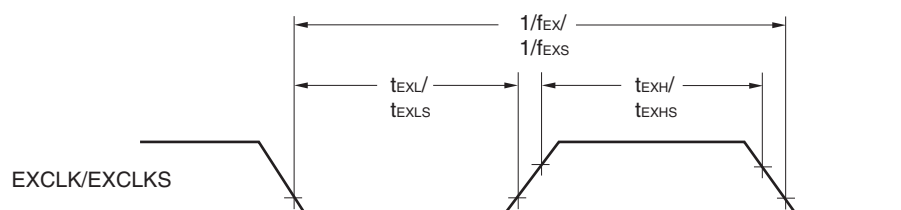
A current higher than the absolute maximum rating must not flow into one pin.

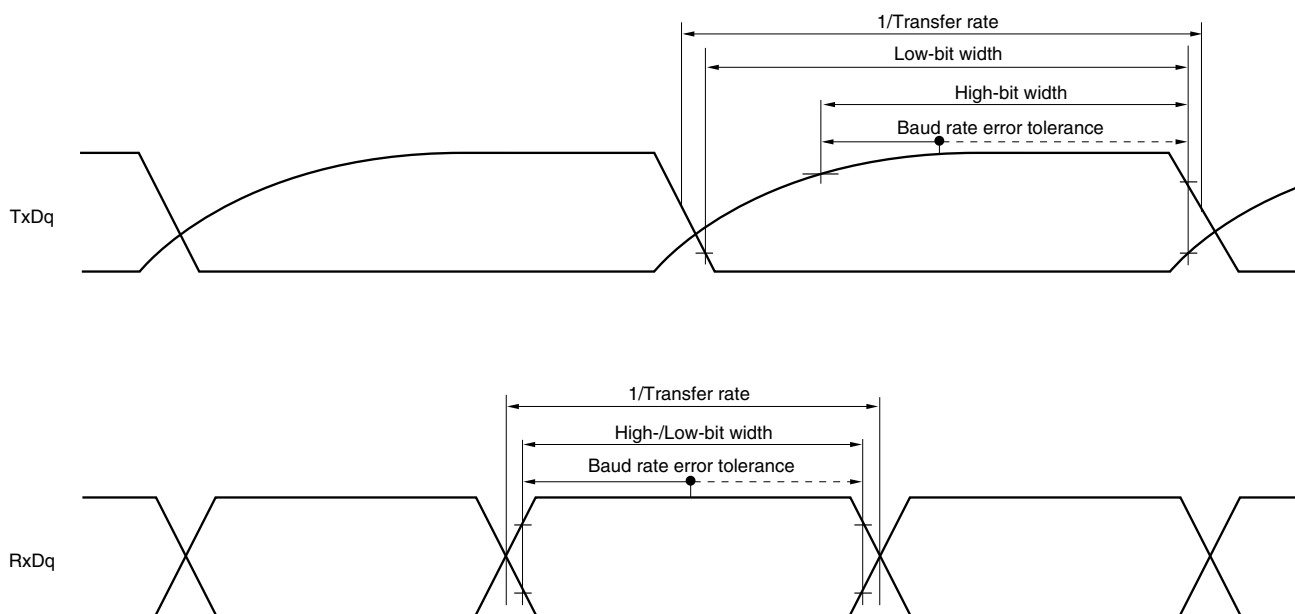
Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- Notes**
1. Total current flowing into V_{DD} and EV_{DD0} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When $AMPHS1 = 1$ (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 32 MHz
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 16 MHz

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

Minimum Instruction Execution Time during Main System Clock Operation**AC Timing Test Points****External System Clock Timing**

UART mode bit width (during communication at different potential) (reference)

- Remarks**
1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance,
 $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage
 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))
 4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|--|------------|---|---------------------------|------|------|
| | | | MIN. | MAX. | |
| Slp setup time (to SCKp↓) ^{Note} | t_{SIK1} | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 88 | | ns |
| | | $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 88 | | ns |
| | | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$ | 220 | | ns |
| Slp hold time (from SCKp↓) ^{Note} | t_{KSI1} | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 38 | | ns |
| | | $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 38 | | ns |
| | | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$ | 38 | | ns |
| Delay time from SCKp↑ to SOp output ^{Note} | t_{KSO1} | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | | 50 | ns |
| | | $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | | 50 | ns |
| | | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$ | | 50 | ns |

Note When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

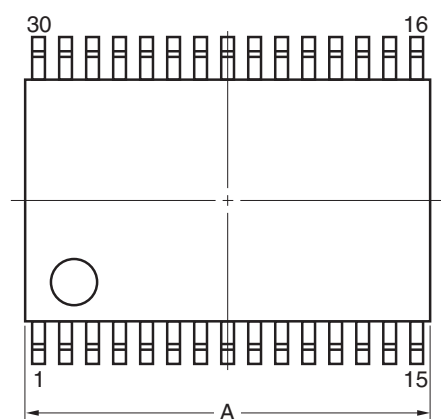
Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

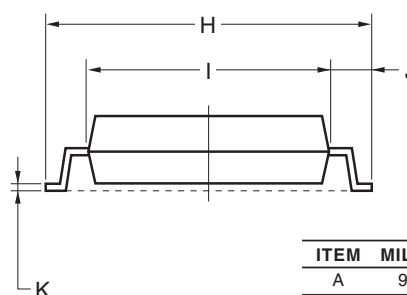
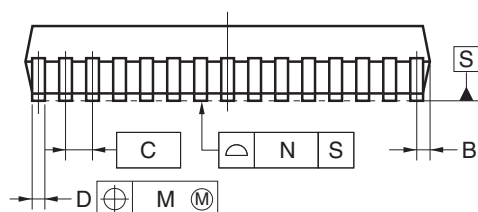
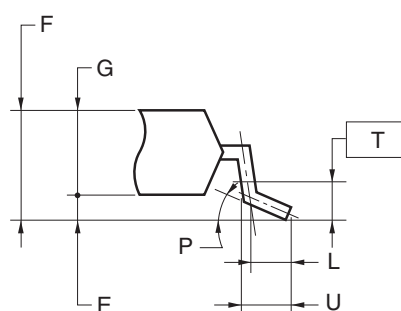
4.4 30-pin Products

R5F100AAASP, R5F100ACASP, R5F100ADASP, R5F100AEASP, R5F100AFASP, R5F100AGASP
 R5F101AAASP, R5F101ACASP, R5F101ADASP, R5F101AEASP, R5F101AFASP, R5F101AGASP
 R5F100AADSP, R5F100ACDSP, R5F100ADDSP, R5F100AEDSP, R5F100AFDSP, R5F100AGDSP
 R5F101AADSP, R5F101ACDSP, R5F101ADDSP, R5F101AEDSP, R5F101AFDSP, R5F101AGDSP
 R5F100AAGSP, R5F100ACGSP, R5F100ADGSP, R5F100AEGSP, R5F100AFGSP, R5F100AGGSP

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---------------------|--------------|----------------|-----------------|
| P-LSSOP30-0300-0.65 | PLSP0030JB-B | S30MC-65-5A4-3 | 0.18 |



detail of lead end

**NOTE**

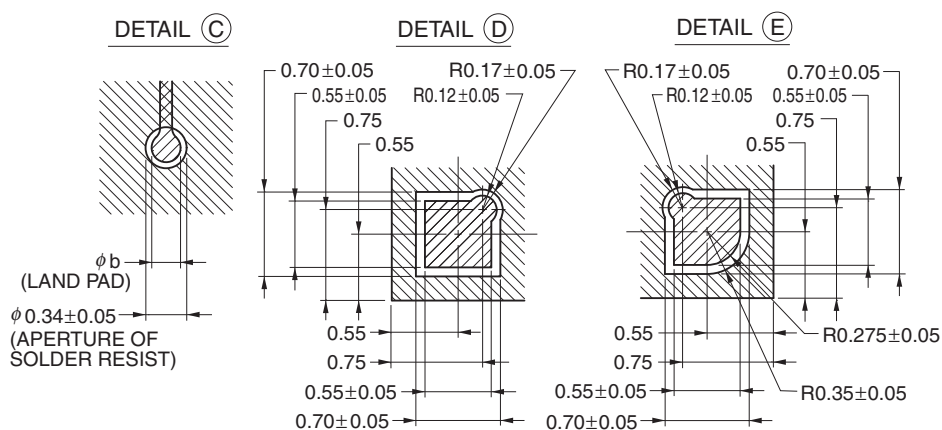
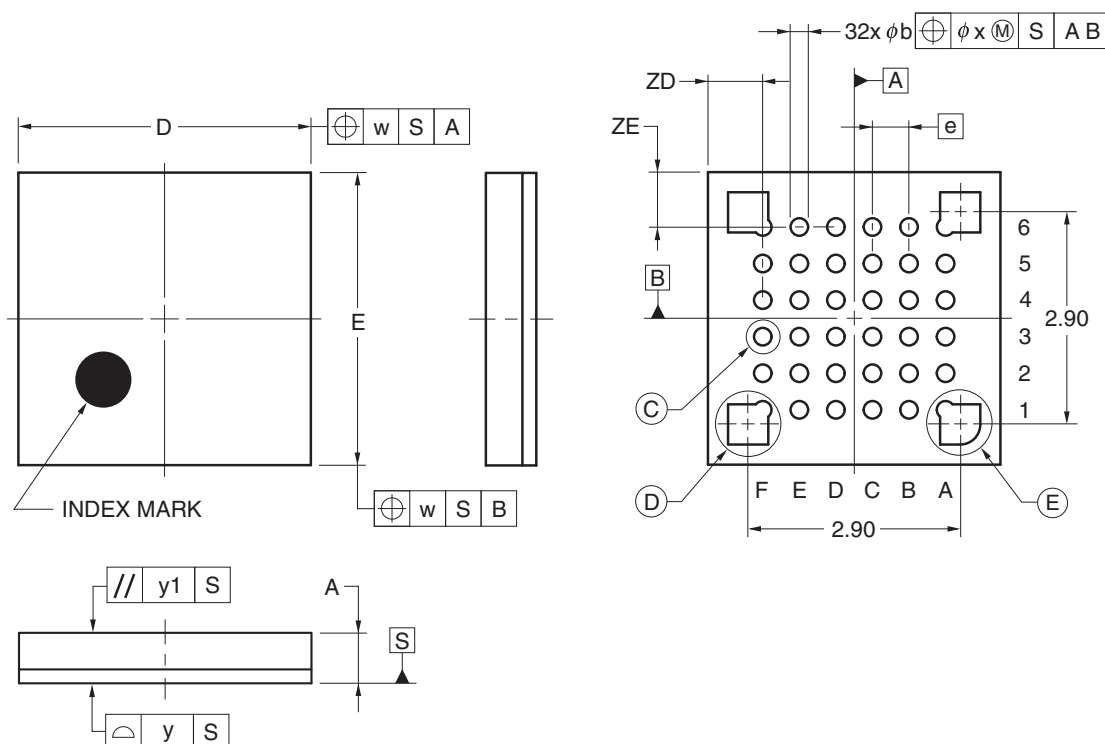
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|------|--|
| A | 9.85±0.15 |
| B | 0.45 MAX. |
| C | 0.65 (T.P.) |
| D | 0.24 ^{+0.08} _{-0.07} |
| E | 0.1±0.05 |
| F | 1.3±0.1 |
| G | 1.2 |
| H | 8.1±0.2 |
| I | 6.1±0.2 |
| J | 1.0±0.2 |
| K | 0.17±0.03 |
| L | 0.5 |
| M | 0.13 |
| N | 0.10 |
| P | 3° ^{+5°} _{-3°} |
| T | 0.25 |
| U | 0.6±0.15 |

4.6 36-pin Products

R5F100CAALA, R5F100CCALA, R5F100CDALA, R5F100CEALA, R5F100CFALA, R5F100CGALA
 R5F101CAALA, R5F101CCALA, R5F101CDALA, R5F101CEALA, R5F101CFALA, R5F101CGALA
 R5F100CAGLA, R5F100CCGLA, R5F100CDGLA, R5F100CEGLA, R5F100CFGLA, R5F100CGGLA

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|--------------------|--------------|----------------|-----------------|
| P-WFLGA36-4x4-0.50 | PWLG0036KA-A | P36FC-50-AA4-2 | 0.023 |



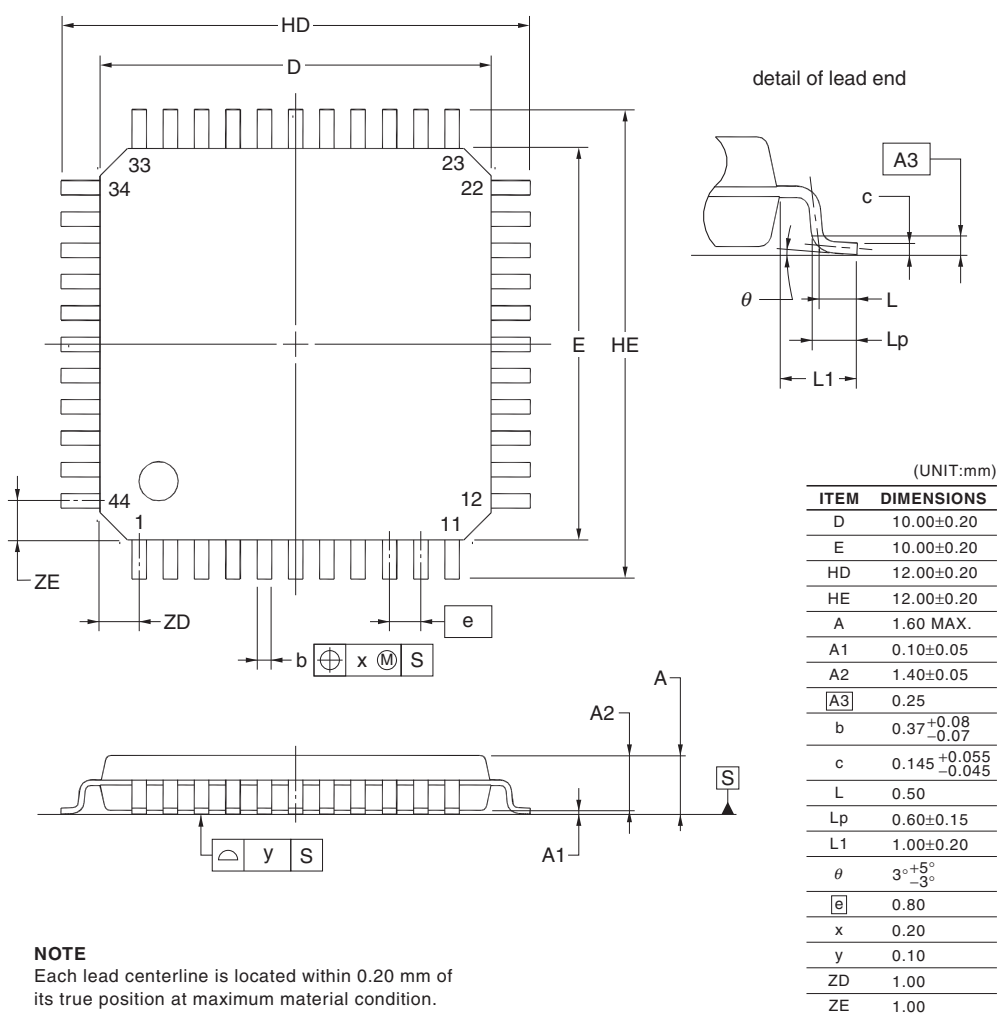
| (UNIT:mm) | |
|-----------|------------|
| ITEM | DIMENSIONS |
| D | 4.00±0.10 |
| E | 4.00±0.10 |
| w | 0.20 |
| e | 0.50 |
| A | 0.69±0.07 |
| b | 0.24±0.05 |
| x | 0.05 |
| y | 0.08 |
| y1 | 0.20 |
| ZD | 0.75 |
| ZE | 0.75 |

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4.8 44-pin Products

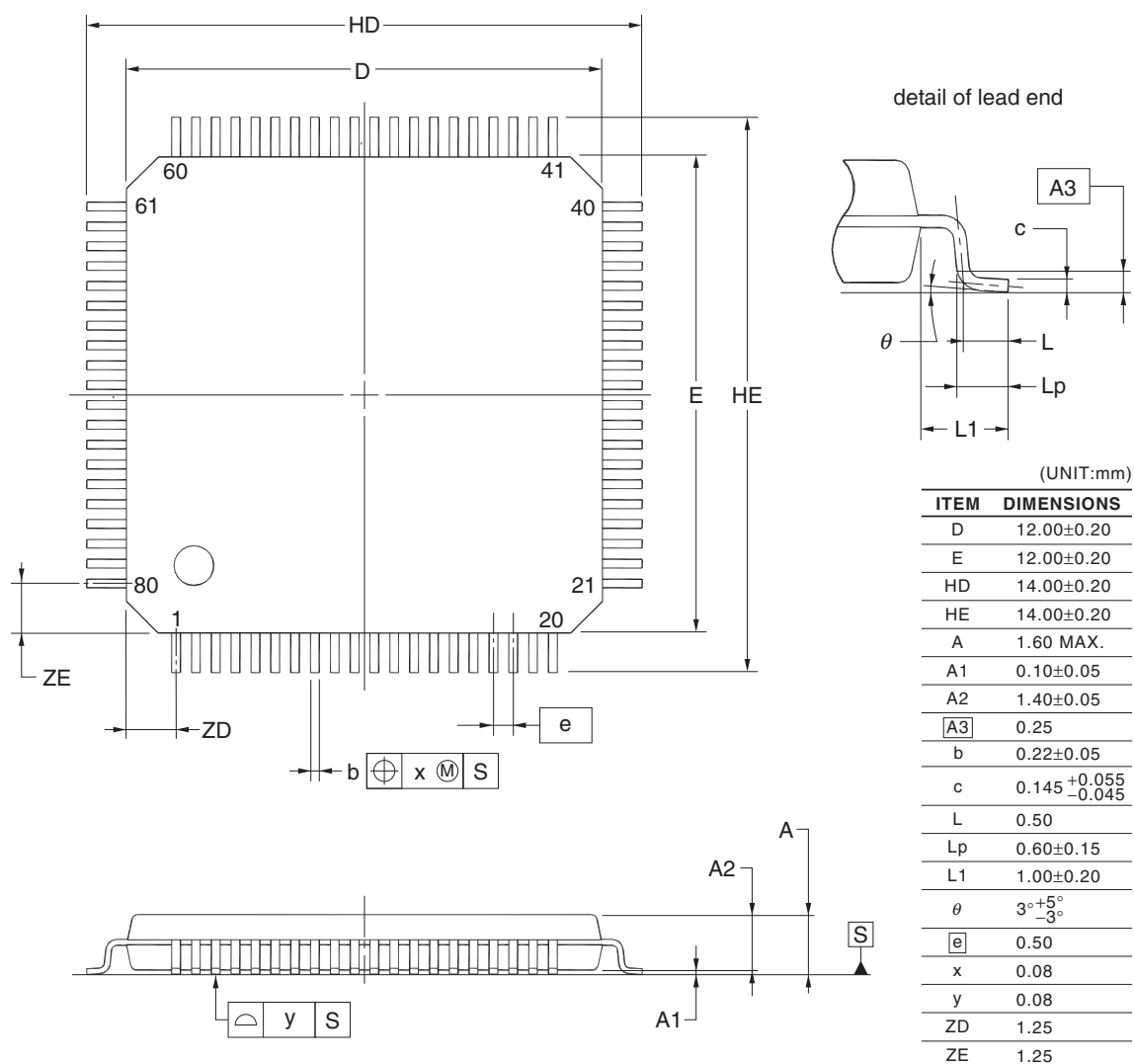
R5F100FAAFP, R5F100FCAFP, R5F100FDAFP, R5F100FEAFP, R5F100FFAFP, R5F100FGAFP,
 R5F100FHAFP, R5F100FJAFP, R5F100FKAFP, R5F100FLAFP
 R5F101FAAFP, R5F101FCAFP, R5F101FDAFP, R5F101FEAFP, R5F101FFAFP, R5F101FGAFP,
 R5F101FHAFP, R5F101FJAFP, R5F101FKAFP, R5F101FLAFP
 R5F100FADFP, R5F100FCDFP, R5F100FDDFP, R5F100FEDFP, R5F100FFDFP, R5F100FGDFP,
 R5F100FHDFP, R5F100FJDFP, R5F100FKDFP, R5F100FLDFP
 R5F101FADFP, R5F101FCDFP, R5F101FDDFP, R5F101FEDFP, R5F101FFDFP, R5F101FGDFP,
 R5F101FHDFP, R5F101FJDFP, R5F101FKDFP, R5F101FLDFP
 R5F100FAGFP, R5F100FCGFP, R5F100FDGFP, R5F100FEGFP, R5F100FFGFP, R5F100FGGFP,
 R5F100FHGFP, R5F100FJGFP

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---------------------|--------------|----------------|-----------------|
| P-LQFP44-10x10-0.80 | PLQP0044GC-A | P44GB-80-UES-2 | 0.36 |



R5F100MFAFB, R5F100MGAFB, R5F100MHAFB, R5F100MJAFB, R5F100MKAFB, R5F100MLAFB
 R5F101MFAFB, R5F101MGAFB, R5F101MHAFB, R5F101MJAFB, R5F101MKAFB, R5F101MLAFB
 R5F100MFDDB, R5F100MGDFB, R5F100MHDFB, R5F100MJDFB, R5F100MKDFB, R5F100MLDFB
 R5F101MFDDB, R5F101MGDFB, R5F101MHDFB, R5F101MJDFB, R5F101MKDFB, R5F101MLDFB
 R5F100MFGFB, R5F100MGGB, R5F100MHGFB, R5F100MJGFB

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|----------------------|--------------|----------------|-----------------|
| P-LFQFP80-12x12-0.50 | PLQP0080KE-A | P80GK-50-8EU-2 | 0.53 |

**NOTE**

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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