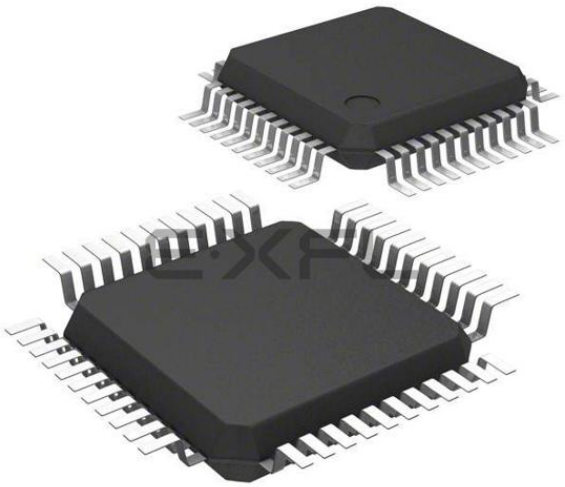
Renesas Electronics America Inc - R5F100FEAFP#V0 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100feafp-v0

Table 1-1. List of Ordering Part Numbers

(3/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
36 pins	36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)	Mounted	A	R5F100CAALA#U0, R5F100CCALA#U0, R5F100CDALA#U0, R5F100CEALA#U0, R5F100CFALA#U0, R5F100CGALA#U0 R5F100CAALA#W0, R5F100CCALA#W0, R5F100CDALA#W0, R5F100CEALA#W0, R5F100CFALA#W0, R5F100CGALA#W0
			G	R5F100CAGLA#U0, R5F100CCGLA#U0, R5F100CDGLA#U0, R5F100CEGLA#U0, R5F100CFGLA#U0, R5F100CGGLA#U0 R5F100CAGLA#W0, R5F100CCGLA#W0, R5F100CDGLA#W0, R5F100CEGLA#W0, R5F100CFGLA#W0, R5F100CGGLA#W0
		Not mounted	A	R5F101CAALA#U0, R5F101CCALA#U0, R5F101CDALA#U0, R5F101CEALA#U0, R5F101CFALA#U0, R5F101CGALA#U0 R5F101CAALA#W0, R5F101CCALA#W0, R5F101CDALA#W0, R5F101CEALA#W0, R5F101CFALA#W0, R5F101CGALA#W0
40 pins	40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)	Mounted	A	R5F100EAANA#U0, R5F100ECANA#U0, R5F100EDANA#U0, R5F100EEANA#U0, R5F100EFANA#U0, R5F100EGANA#U0, R5F100EHANA#U0 R5F100EAANA#W0, R5F100ECANA#W0, R5F100EDANA#W0, R5F100EEANA#W0, R5F100EFANA#W0, R5F100EGANA#W0, R5F100EHANA#W0
			D	R5F100EADNA#U0, R5F100ECDNA#U0, R5F100EDDNA#U0, R5F100EEDNA#U0, R5F100EFDNA#U0, R5F100EGDNA#U0, R5F100EHDNA#U0 R5F100EADNA#W0, R5F100ECDNA#W0, R5F100EDDNA#W0, R5F100EEDNA#W0, R5F100EFDNA#W0, R5F100EGDNA#W0, R5F100EHDNA#W0
			G	R5F100EAGNA#U0, R5F100ECGNA#U0, R5F100EDGNA#U0, R5F100EEGNA#U0, R5F100EFGNA#U0, R5F100EGGNA#U0, R5F100EHGNA#U0 R5F100EAGNA#W0, R5F100ECGNA#W0, R5F100EDGNA#W0, R5F100EEGNA#W0, R5F100EFGNA#W0, R5F100EGGNA#W0, R5F100EHGNA#W0
		Not mounted	A	R5F101EAANA#U0, R5F101ECANA#U0, R5F101EDANA#U0, R5F101EEANA#U0, R5F101EFANA#U0, R5F101EGANA#U0, R5F101EHANA#U0 R5F101EAANA#W0, R5F101ECANA#W0, R5F101EDANA#W0, R5F101EEANA#W0, R5F101EFANA#W0, R5F101EGANA#W0, R5F101EHANA#W0
			D	R5F101EADNA#U0, R5F101ECDNA#U0, R5F101EDDNA#U0, R5F101EEDNA#U0, R5F101EFDNA#U0, R5F101EGDNA#U0, R5F101EHDNA#U0 R5F101EADNA#W0, R5F101ECDNA#W0, R5F101EDDNA#W0, R5F101EEDNA#W0, R5F101EFDNA#W0, R5F101EGDNA#W0, R5F101EHDNA#W0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

(8/12)

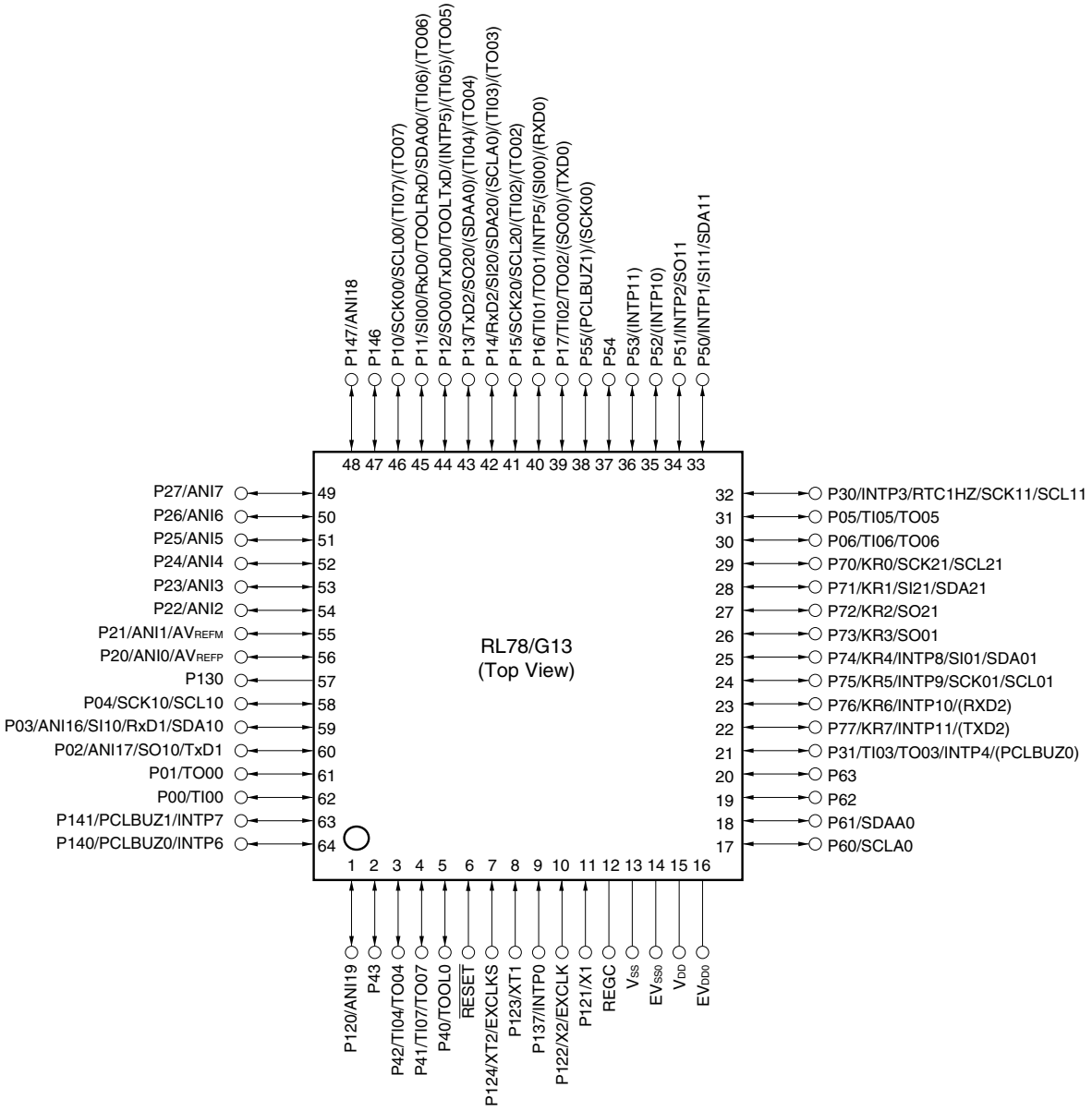
Pin count	Package	Data flash	Fields of Application [Note]	Ordering Part Number
64 pins	64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)	Mounted	A	R5F100LCAFA#V0, R5F100LDAFA#V0, R5F100LEAFA#V0, R5F100LFAFA#V0, R5F100LGAFA#V0, R5F100LHAFA#V0, R5F100LJAFA#V0, R5F100LKAFA#V0, R5F100LLAFA#V0 R5F100LCAFA#X0, R5F100LDAFA#X0, R5F100LEAFA#X0, R5F100LFAFA#X0,
			D	R5F100LGAFA#X0, R5F100LHAFA#X0, R5F100LJAFA#X0, R5F100LKAFA#X0, R5F100LLAFA#X0 R5F100LCDFA#V0, R5F100LDDFA#V0, R5F100LEDFA#V0, R5F100LFDFA#V0, R5F100LGDFA#V0, R5F100LHDFA#V0, R5F100LJDFA#V0, R5F100LKDFA#V0, R5F100LLDFA#V0
			G	R5F100LCDFA#X0, R5F100LDDFA#X0, R5F100LEDFA#X0, R5F100LFDFA#X0, R5F100LGDFA#X0, R5F100LHDFA#X0, R5F100LJDFA#X0, R5F100LKDFA#X0, R5F100LLDFA#X0 R5F100LCGFA#V0, R5F100LDGFA#V0, R5F100LEGFA#V0, R5F100LFGFA#V0 R5F100LCGFA#X0, R5F100LDGFA#X0, R5F100LEGFA#X0, R5F100LFGFA#X0 R5F100LGGFA#V0, R5F100LHGFA#V0, R5F100LJGFA#V0 R5F100LGGFA#X0, R5F100LHGFA#X0, R5F100LJGFA#X0
		Not mounted	A	R5F101LCAFA#V0, R5F101LDAFA#V0, R5F101LEAFA#V0, R5F101LFAFA#V0, R5F101LGAFA#V0, R5F101LHAFA#V0, R5F101LJAFA#V0, R5F101LKAFA#V0, R5F101LLAFA#V0 R5F101LCAFA#X0, R5F101LDAFA#X0, R5F101LEAFA#X0, R5F101LFAFA#X0,
			D	R5F101LGAFA#X0, R5F101LHAFA#X0, R5F101LJAFA#X0, R5F101LKAFA#X0, R5F101LLAFA#X0 R5F101LCDFA#V0, R5F101LDDFA#V0, R5F101LEDFA#V0, R5F101LFDFA#V0, R5F101LGDFA#V0, R5F101LHDFA#V0, R5F101LJDFA#V0, R5F101LKDFA#V0, R5F101LLDFA#V0 R5F101LCDFA#X0, R5F101LDDFA#X0, R5F101LEDFA#X0, R5F101LFDFA#X0, R5F101LGDFA#X0, R5F101LHDFA#X0, R5F101LJDFA#X0, R5F101LKDFA#X0, R5F101LLDFA#X0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.11 64-pin products

- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)



Cautions 1. Make EV_{SS0} pin the same potential as V_{SS} pin.

2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.

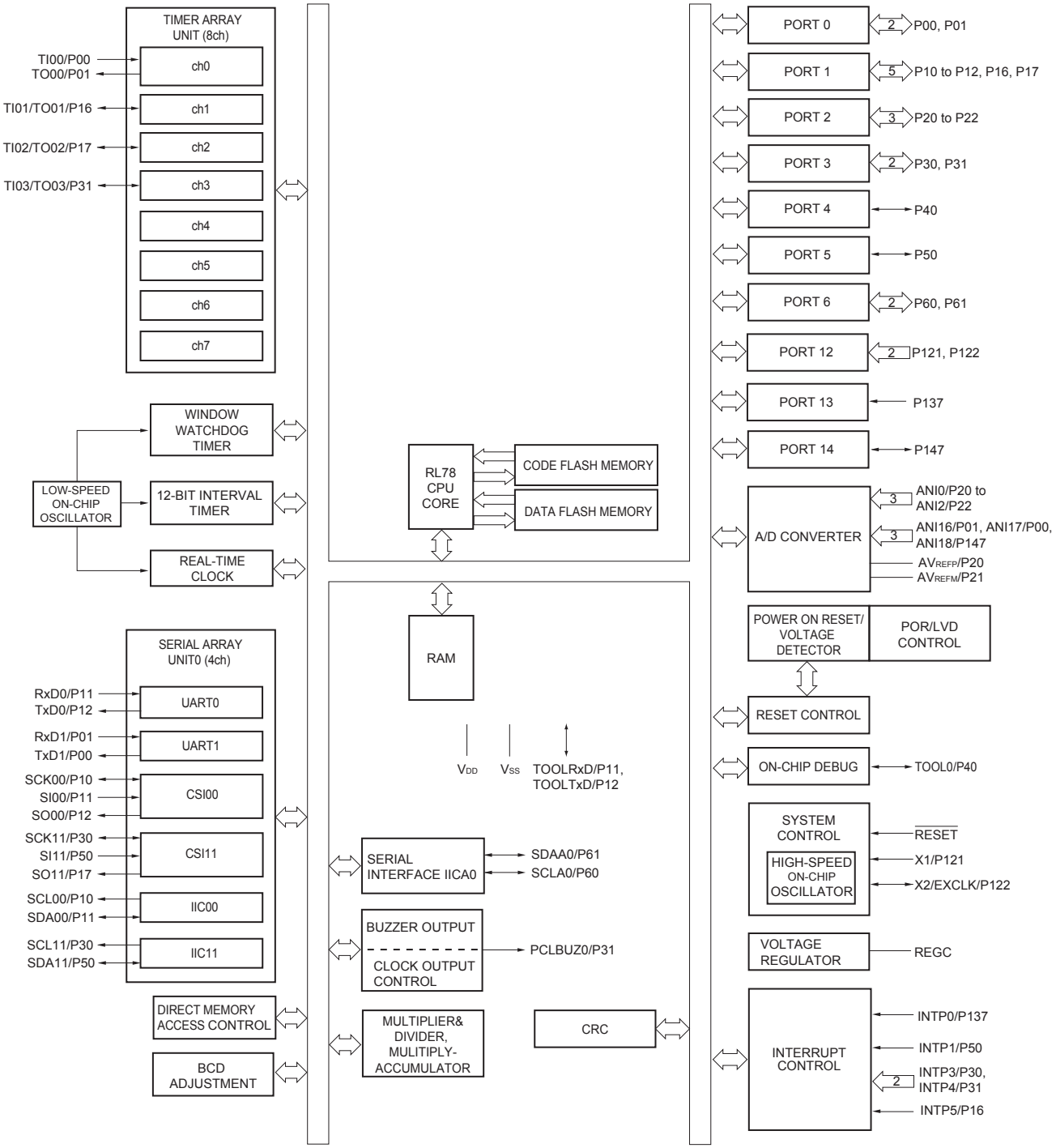
3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

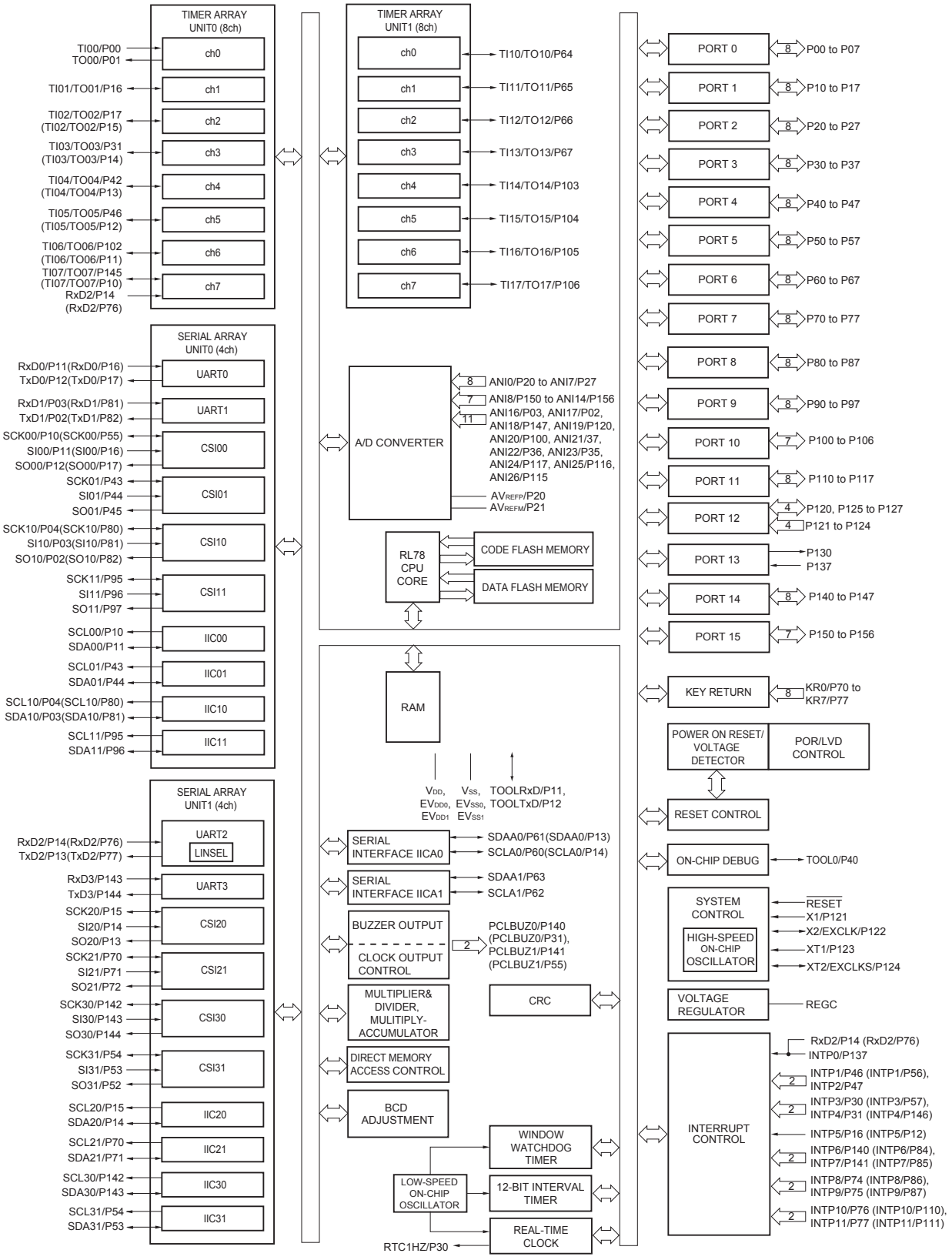
2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.

3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.2 24-pin products



1.5.14 128-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).
4. When setting to PIOR = 1

(2/2)

Item		20-pin		24-pin		25-pin		30-pin		32-pin		36-pin	
		R5F1006x	R5F1016x	R5F1007x	R5F1017x	R5F1008x	R5F1018x	R5F100Ax	R5F101Ax	R5F100Bx	R5F101Bx	R5F100Cx	R5F101Cx
Clock output/buzzer output		–		1		1		2		2		2	
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation)											
8/10-bit resolution A/D converter		6 channels		6 channels		6 channels		8 channels		8 channels		8 channels	
Serial interface		[20-pin, 24-pin, 25-pin products] • CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel [30-pin, 32-pin products] • CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I^2C: 1 channel/UART (UART supporting LIN-bus): 1 channel [36-pin products] • CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I^2C: 2 channels/UART (UART supporting LIN-bus): 1 channel											
	I^2C bus	–		1 channel		1 channel		1 channel		1 channel		1 channel	
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)											
DMA controller		2 channels											
Vectored interrupt sources	Internal	23		24		24		27		27		27	
	External	3		5		5		6		6		6	
Key interrupt		–											
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note • Internal reset by RAM parity error • Internal reset by illegal-memory access											
Power-on-reset circuit		• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)											
Voltage detector		• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)											
On-chip debug function		Provided											
<R> Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = -40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = -40 to +105°C)											
Operating ambient temperature		T_A = 40 to +85°C (A: Consumer applications, D: Industrial applications) T_A = 40 to +105°C (G: Industrial applications)											

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f_{IH} = 32 MHz Note 4	V_{DD} = 5.0 V		0.54	1.63	mA
					V_{DD} = 3.0 V		0.54	1.63	mA
				f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.44	1.28	mA
					V_{DD} = 3.0 V		0.44	1.28	mA
				f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.40	1.00	mA
					V_{DD} = 3.0 V		0.40	1.00	mA
			LS (low-speed main) mode Note 7	f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V		260	530	μA
					V_{DD} = 2.0 V		260	530	μA
			LV (low-voltage main) mode Note 7	f_{IH} = 4 MHz Note 4	V_{DD} = 3.0 V		420	640	μA
					V_{DD} = 2.0 V		420	640	μA
			HS (high-speed main) mode Note 7	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.45	1.17	mA
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.45	1.17	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.19	0.60	mA
					Resonator connection		0.26	0.67	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.19	0.60	mA
					Resonator connection		0.26	0.67	mA
			LS (low-speed main) mode Note 7	f_{MX} = 8 MHz Note 3, V_{DD} = 3.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	μA
				f_{MX} = 8 MHz Note 3, V_{DD} = 2.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	μA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5 T_A = −40°C	Square wave input		0.25	0.57	μA
					Resonator connection		0.44	0.76	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +25°C	Square wave input		0.30	0.57	μA
					Resonator connection		0.49	0.76	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +50°C	Square wave input		0.37	1.17	μA
					Resonator connection		0.56	1.36	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +70°C	Square wave input		0.53	1.97	μA
					Resonator connection		0.72	2.16	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +85°C	Square wave input		0.82	3.37	μA
					Resonator connection		1.01	3.56	μA
	I_{DD3} Note 6	STOP mode Note 8	T_A = −40°C				0.18	0.50	μA
			T_A = +25°C				0.23	0.50	μA
			T_A = +50°C				0.30	1.10	μA
			T_A = +70°C				0.46	1.90	μA
			T_A = +85°C				0.75	3.30	μA

(**Notes** and **Remarks** are listed on the next page.)

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.3		mA
						V_{DD} = 3.0 V		2.3		mA
					Normal operation	V_{DD} = 5.0 V		5.2	8.5	mA
						V_{DD} = 3.0 V		5.2	8.5	mA
				f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.1	6.6	mA
						V_{DD} = 3.0 V		4.1	6.6	mA
				f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		3.0	4.7	mA
						V_{DD} = 3.0 V		3.0	4.7	mA
			LS (low-speed main) mode Note 5	f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.3	2.1	mA
						V_{DD} = 2.0 V		1.3	2.1	mA
			LV (low-voltage main) mode Note 5	f_{IH} = 4 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.3	1.8	mA
						V_{DD} = 2.0 V		1.3	1.8	mA
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.4	5.5	mA
						Resonator connection		3.6	5.7	mA
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.4	5.5	mA
						Resonator connection		3.6	5.7	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.1	3.2	mA
						Resonator connection		2.1	3.2	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.1	3.2	mA
						Resonator connection		2.1	3.2	mA
			LS (low-speed main) mode Note 5	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.2	2.0	mA
				f_{MX} = 8 MHz Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.2	2.0	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = −40°C	Normal operation	Square wave input		4.8	5.9	μA
						Resonator connection		4.9	6.0	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		4.9	5.9	μA
						Resonator connection		5.0	6.0	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		5.0	7.6	μA
						Resonator connection		5.1	7.7	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		5.2	9.3	μA
						Resonator connection		5.3	9.4	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		5.7	13.3	μA
						Resonator connection		5.8	13.4	μA

(**Notes** and **Remarks** are listed on the next page.)

6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.

8. Current flowing only during data flash rewrite.

9. Current flowing only during self programming.

10. For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode.**

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK}: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T_A = 25°C

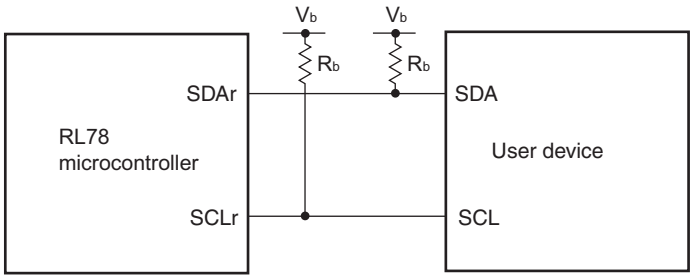
(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

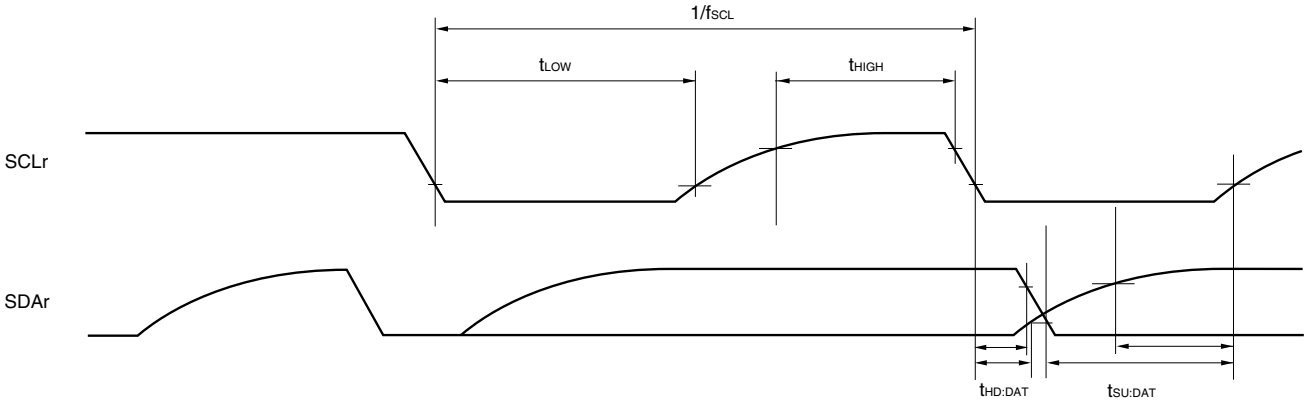
Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	24 MHz < f_{MCK}	14/f_{MCK}		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}		—		—		ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	24 MHz < f_{MCK}	20/f_{MCK}		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}		—		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}		—		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	24 MHz < f_{MCK}	48/f_{MCK}		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}		—		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}		—		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		16/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

Simplified I^2C mode connection diagram (during communication at different potential)



Simplified I^2C mode serial transfer timing (during communication at different potential)



Remarks 1. R_b[Ω]:Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13)

Remark The electrical characteristics of the products G: Industrial applications (T_A = -40 to +105°C) are different from those of the products "A: Consumer applications, and D: Industrial applications". For details, refer to **3.1** to **3.10**.

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
	EV_{DD0}, EV_{DD1}	EV_{DD0} = EV_{DD1}	−0.5 to +6.5	V
	EV_{SS0}, EV_{SS1}	EV_{SS0} = EV_{SS1}	−0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to +2.8 and −0.3 to V_{DD} +0.3 Note 1	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	−0.3 to EV_{DD0} +0.3 and −0.3 to V_{DD} +0.3 Note 2	V
	V_{I2}	P60 to P63 (N-ch open-drain)	−0.3 to +6.5	V
	V_{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$	−0.3 to V_{DD} +0.3 Note 2	V
Output voltage	V_{O1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−0.3 to EV_{DD0} +0.3 and −0.3 to V_{DD} +0.3 Note 2	V
	V_{O2}	P20 to P27, P150 to P156	−0.3 to V_{DD} +0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI16 to ANI26	−0.3 to EV_{DD0} +0.3 and −0.3 to AV_{REF}(+) +0.3 Notes 2, 3	V
	V_{AI2}	ANI0 to ANI14	−0.3 to V_{DD} +0.3 and −0.3 to AV_{REF}(+) +0.3 Notes 2, 3	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed AV_{REF}(+) + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. AV_{REF}(+) : + side reference voltage of the A/D converter.

3. V_{SS} : Reference voltage

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

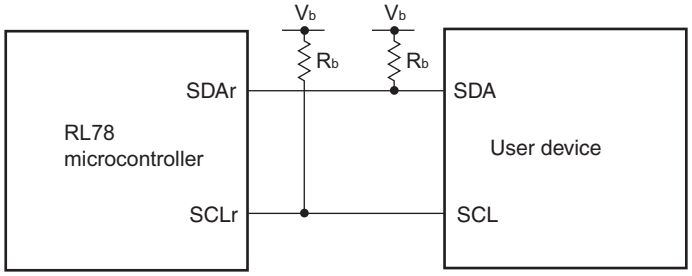
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SIp setup time (to SCKp↓) Note	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	88		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	88		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	220		ns
SIp hold time (from SCKp↓) Note	t_{KSI1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	38		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	38		ns
Delay time from SCKp↑ to SOp output Note	t_{KSO1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		50	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		50	ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		50	ns

Note When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

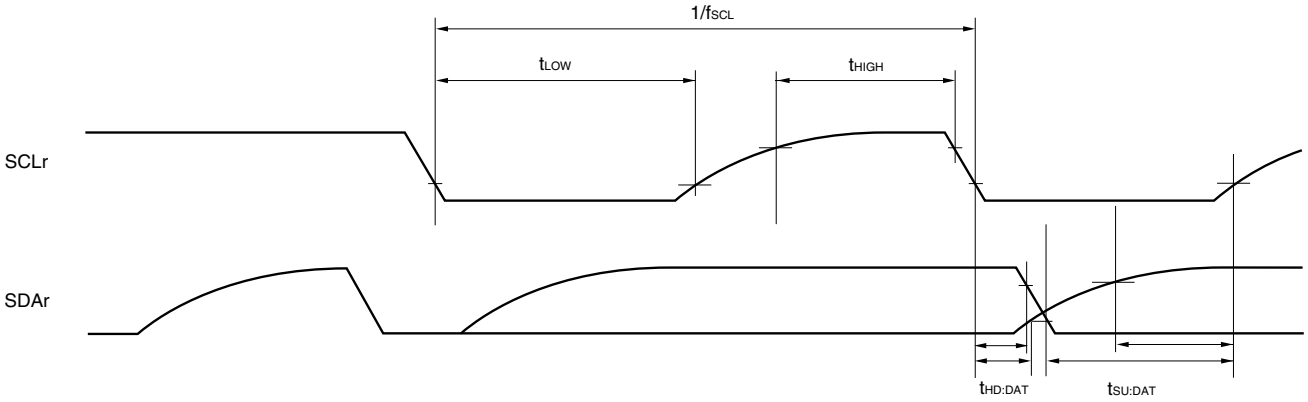
Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

Simplified I^2C mode connection diagram (during communication at different potential)



Simplified I^2C mode serial transfer timing (during communication at different potential)



Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. R_b[Ω]:Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)

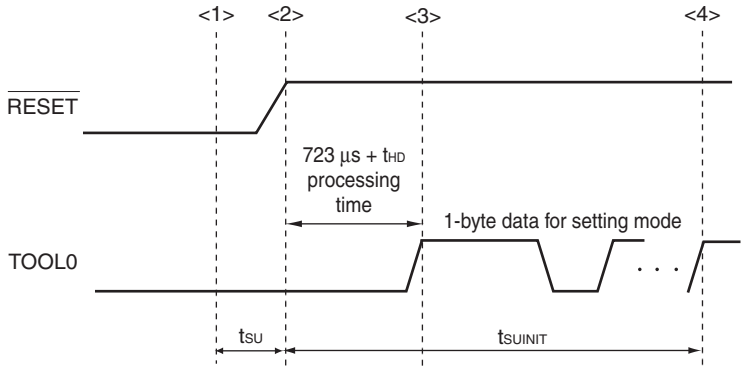
3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13)

3.10 Timing of Entry to Flash Memory Programming Modes

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

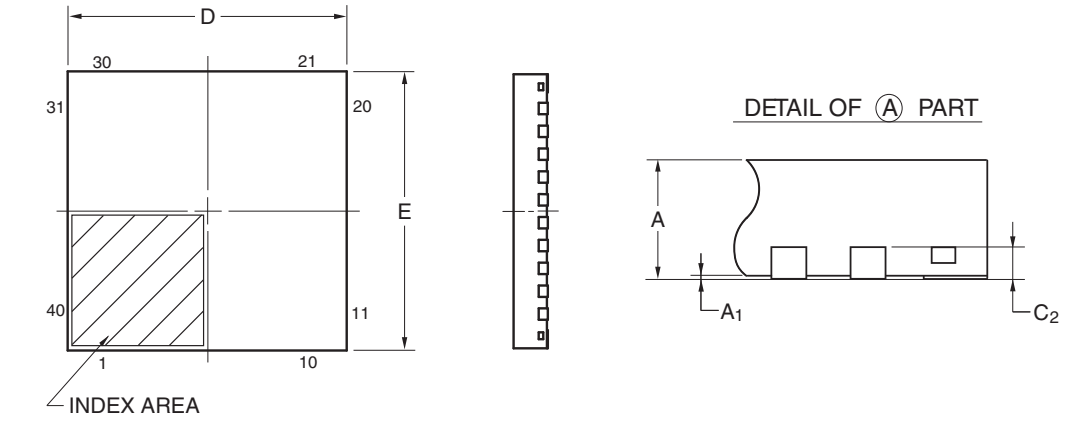
t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

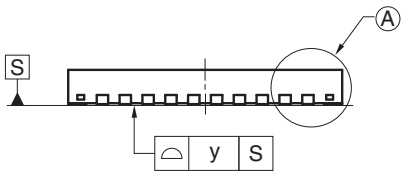
t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

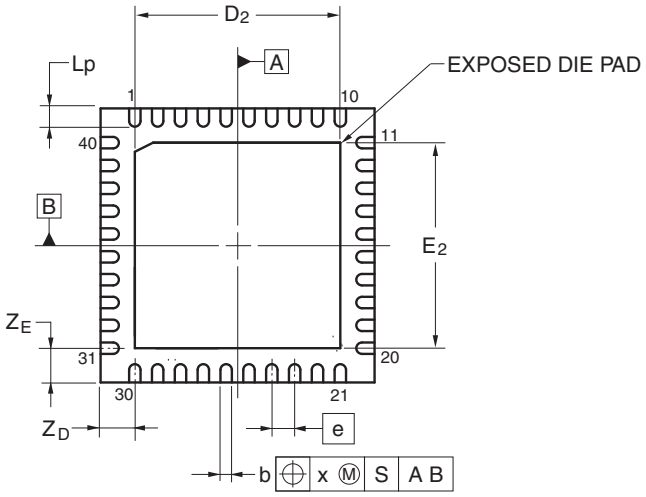
4.7 40-pin Products

R5F100EAANA, R5F100ECANA, R5F100EDANA, R5F100EEANA, R5F100EFANA, R5F100EGANA, R5F100EHANA
R5F101EAANA, R5F101ECANA, R5F101EDANA, R5F101EEANA, R5F101EFANA, R5F101EGANA, R5F101EHANA
R5F100EADNA, R5F100ECDNA, R5F100EDDNA, R5F100EEDNA, R5F100EFDNA, R5F100EGDNA,
R5F100EHDNA
R5F101EADNA, R5F101ECDNA, R5F101EDDNA, R5F101EEDNA, R5F101EFDNA, R5F101EGDNA,
R5F101EHDNA
R5F100EAGNA, R5F100ECGNA, R5F100EDGNA, R5F100EEGNA, R5F100EFGNA, R5F100EGGNA,
R5F100EHGNA

JEITA Package code	RENESAS code	Previous code	MASS (TYP.) [g]
P-HWQFN40-6x6-0.50	PWQN0040KC-A	P40K8-50-4B4-5	0.09







Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	5.95	6.00	6.05
E	5.95	6.00	6.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	4.50	—
E_2	—	4.50	—

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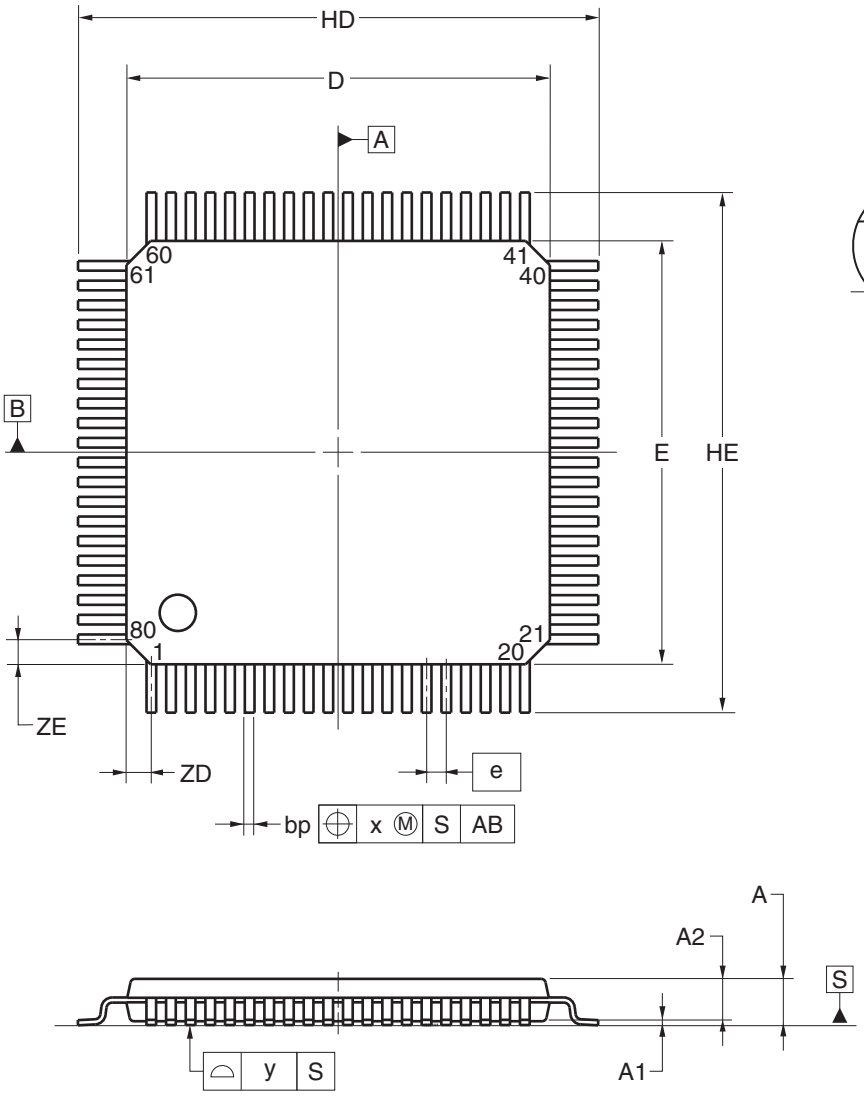
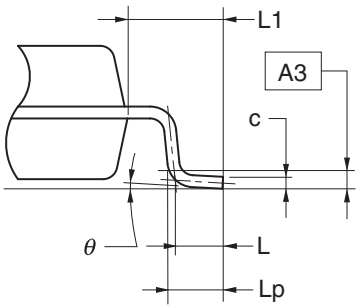
4.12 80-pin Products

R5F100MFAFA, R5F100MGAFA, R5F100MHAFA, R5F100MJAFA, R5F100MKAFA, R5F100MLAFA
R5F101MFAFA, R5F101MGAFA, R5F101MHAFA, R5F101MJAFA, R5F101MKAFA, R5F101MLAFA
R5F100MFDFA, R5F100MGDFA, R5F100MHDFA, R5F100MJDFA, R5F100MKDFA, R5F100MLDFA
R5F101MFDFA, R5F101MGDFA, R5F101MHDFA, R5F101MJDFA, R5F101MKDFA, R5F101MLDFA
R5F100MFGFA, R5F100MGGFA, R5F100MHGFA, R5F100MJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP80-14x14-0.65	PLQP0080JB-E	P80GC-65-UBT-2	0.69



detail of lead end



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.80	14.00	14.20
E	13.80	14.00	14.20
HD	17.00	17.20	17.40
HE	17.00	17.20	17.40
A	—	—	1.70
A1	0.05	0.125	0.20
A2	1.35	1.40	1.45
A3	—	0.25	—
bp	0.26	0.32	0.38
c	0.10	0.145	0.20
L	—	0.80	—
Lp	0.736	0.886	1.036
L1	1.40	1.60	1.80
θ	0°	3°	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
ZD	—	0.825	—
ZE	—	0.825	—

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Rev.	Date	Description	
		Page	Summary
3.00	Aug 02, 2013	118	Modification of table in 2.6.2 Temperature sensor/internal reference voltage characteristics
		118	Modification of table and note in 2.6.3 POR circuit characteristics
		119	Modification of table in 2.6.4 LVD circuit characteristics
		120	Modification of table of LVD Detection Voltage of Interrupt & Reset Mode
		120	Renamed to 2.6.5 Power supply voltage rising slope characteristics
		122	Modification of table, figure, and remark in 2.10 Timing Specs for Switching Flash Memory Programming Modes
		123	Modification of caution 1 and description
		124	Modification of table and remark 3 in Absolute Maximum Ratings (T_A = 25°C)
		126	Modification of table, note, caution, and remark in 3.2.1 X1, XT1 oscillator characteristics
		126	Modification of table in 3.2.2 On-chip oscillator characteristics
		127	Modification of note 3 in 3.3.1 Pin characteristics (1/5)
		128	Modification of note 3 in 3.3.1 Pin characteristics (2/5)
		133	Modification of notes 1 and 4 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products (1/2)
		135	Modification of notes 1, 5, and 6 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products (2/2)
		137	Modification of notes 1 and 4 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products (1/2)
		139	Modification of notes 1, 5, and 6 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products (2/2)
		140	Modification of (3) Peripheral Functions (Common to all products)
		142	Modification of table in 3.4 AC Characteristics
		143	Addition of Minimum Instruction Execution Time during Main System Clock Operation
		143	Modification of figure of AC Timing Test Points
		143	Modification of figure of External System Clock Timing
		145	Modification of figure of AC Timing Test Points
		145	Modification of description, note 1, and caution in (1) During communication at same potential (UART mode)
		146	Modification of description in (2) During communication at same potential (CSI mode)
		147	Modification of description in (3) During communication at same potential (CSI mode)
		149	Modification of table, note 1, and caution in (4) During communication at same potential (simplified I^2C mode)
		151	Modification of table, note 1, and caution in (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)
		152 to 154	Modification of table, notes 2 to 6, caution, and remarks 1 to 4 in (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		155	Modification of table in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3)
		156	Modification of table and caution in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3)
		157, 158	Modification of table, caution, and remarks 3 and 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		160, 161	Modification of table and caution in (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode)

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