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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

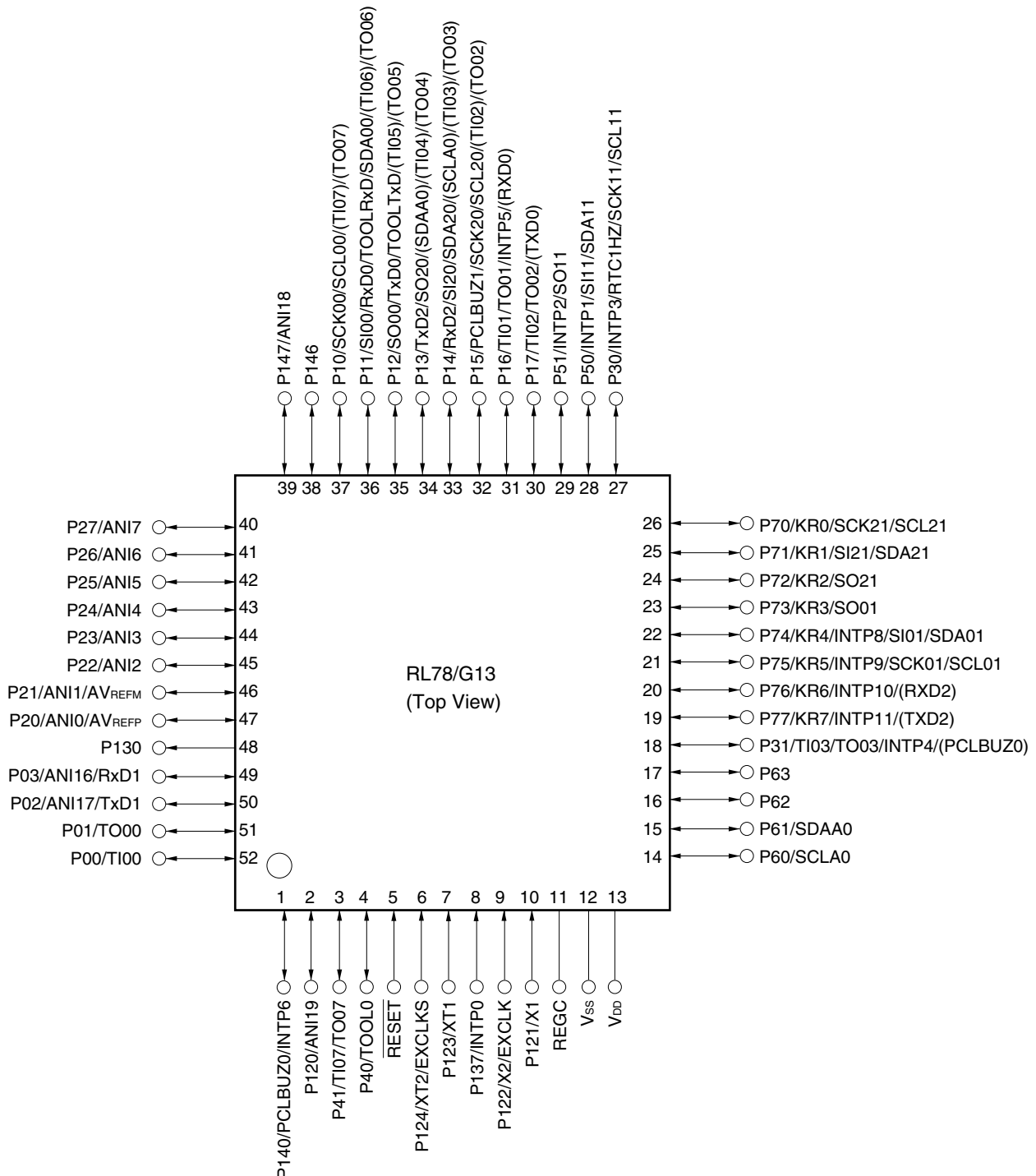
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100fegfp-v0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100fegfp-v0</a>

## 1.3.10 52-pin products

- 52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)



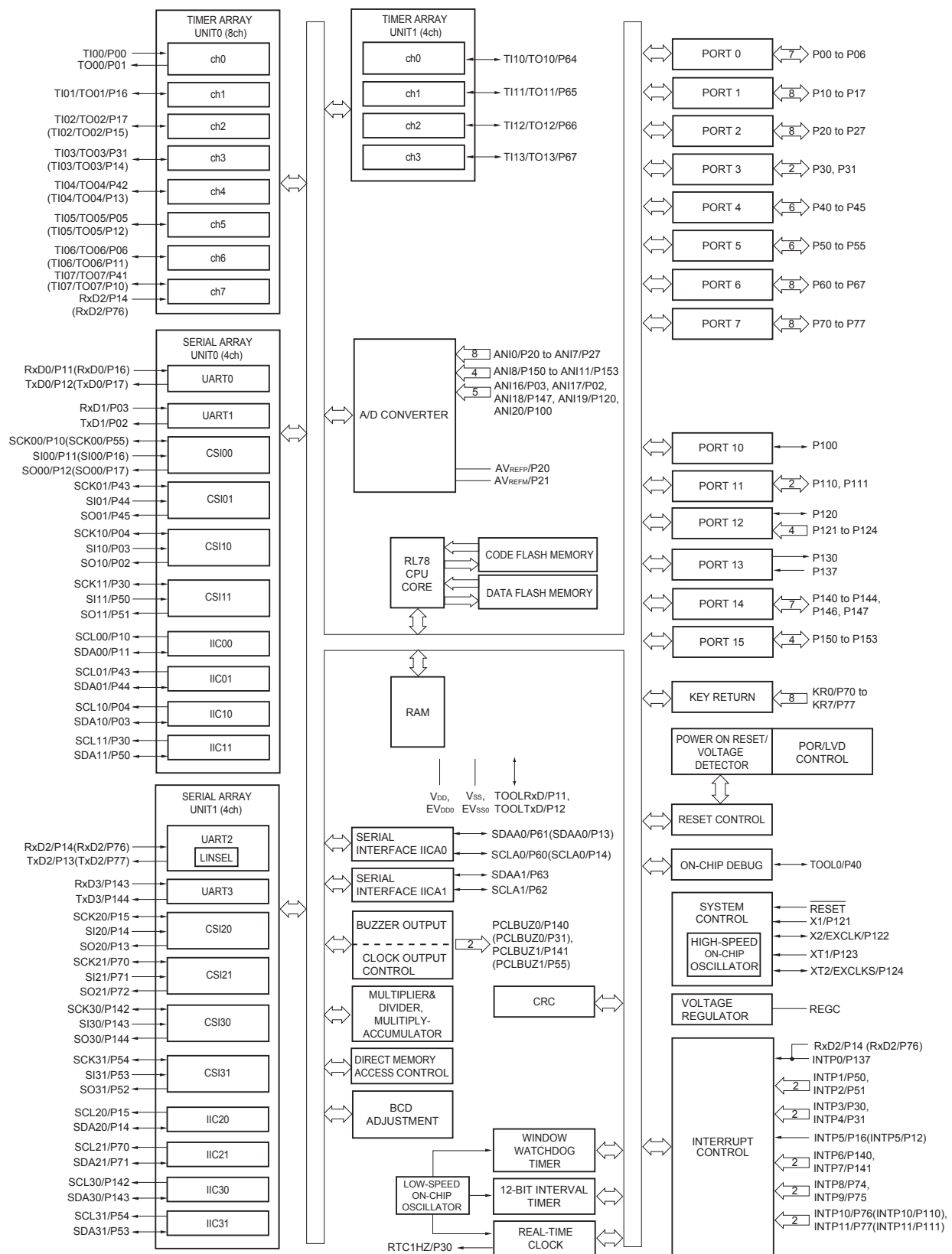
**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F).

**Remarks 1.** For pin identification, see 1.4 Pin Identification.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.



## 1.5.12 80-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).
4. When setting to PIOR = 1

(2/2)

Item	20-pin		24-pin		25-pin		30-pin		32-pin		36-pin	
	R5F1006x	R5F1016x	R5F1007x	R5F1017x	R5F1008x	R5F1018x	R5F100Ax	R5F101Ax	R5F100Bx	R5F101Bx	R5F100Cx	R5F101Cx
Clock output/buzzer output	—		1		1		2		2		2	
	• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f <sub>MAIN</sub> = 20 MHz operation)											
8/10-bit resolution A/D converter	6 channels		6 channels		6 channels		8 channels		8 channels		8 channels	
Serial interface	[20-pin, 24-pin, 25-pin products] • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel [30-pin, 32-pin products] • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART (UART supporting LIN-bus): 1 channel [36-pin products] • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I <sup>2</sup> C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I <sup>2</sup> C: 2 channels/UART (UART supporting LIN-bus): 1 channel											
	I <sup>2</sup> C bus	—	1 channel		1 channel		1 channel		1 channel		1 channel	
Multiplier and divider/multiply-accumulator	• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)											
DMA controller	2 channels											
Vectored interrupt sources	Internal	23	24		24		27		27		27	
	External	3	5		5		6		6		6	
Key interrupt	—											
Reset	• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution <sup>Note</sup> • Internal reset by RAM parity error • Internal reset by illegal-memory access											
Power-on-reset circuit	• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)											
Voltage detector	• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)											
On-chip debug function	Provided											
Power supply voltage	V <sub>DD</sub> = 1.6 to 5.5 V (T <sub>A</sub> = -40 to +85°C) V <sub>DD</sub> = 2.4 to 5.5 V (T <sub>A</sub> = -40 to +105°C)											
Operating ambient temperature	T <sub>A</sub> = 40 to +85°C (A: Consumer applications, D: Industrial applications ) T <sub>A</sub> = 40 to +105°C (G: Industrial applications)											

**Note** The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

## 2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T<sub>A</sub> = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V <sub>DD</sub>		-0.5 to +6.5	V
	EV <sub>DD0</sub> , EV <sub>DD1</sub>	EV <sub>DD0</sub> = EV <sub>DD1</sub>	-0.5 to +6.5	V
	EV <sub>SS0</sub> , EV <sub>SS1</sub>	EV <sub>SS0</sub> = EV <sub>SS1</sub>	-0.5 to +0.3	V
REGC pin input voltage	V <sub>IREGC</sub>	REGC	-0.3 to +2.8 and -0.3 to V <sub>DD</sub> + 0.3 <sup>Note 1</sup>	V
Input voltage	V <sub>I1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	-0.3 to EV <sub>DD0</sub> + 0.3 and -0.3 to V <sub>DD</sub> + 0.3 <sup>Note 2</sup>	V
	V <sub>I2</sub>	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V <sub>I3</sub>	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, RESET	-0.3 to V <sub>DD</sub> + 0.3 <sup>Note 2</sup>	V
Output voltage	V <sub>O1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-0.3 to EV <sub>DD0</sub> + 0.3 and -0.3 to V <sub>DD</sub> + 0.3 <sup>Note 2</sup>	V
	V <sub>O2</sub>	P20 to P27, P150 to P156	-0.3 to V <sub>DD</sub> + 0.3 <sup>Note 2</sup>	V
Analog input voltage	V <sub>AI1</sub>	ANI16 to ANI26	-0.3 to EV <sub>DD0</sub> + 0.3 and -0.3 to AV <sub>REF</sub> (+) + 0.3 <sup>Notes 2, 3</sup>	V
	V <sub>AI2</sub>	ANI0 to ANI14	-0.3 to V <sub>DD</sub> + 0.3 and -0.3 to AV <sub>REF</sub> (+) + 0.3 <sup>Notes 2, 3</sup>	V

**Notes 1.** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**2.** Must be 6.5 V or lower.

**3.** Do not exceed AV<sub>REF</sub>(+) + 0.3 V in case of A/D conversion target pin.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**2.** AV<sub>REF</sub>(+) : + side reference voltage of the A/D converter.

**3.** V<sub>SS</sub> : Reference voltage

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ E<sub>VDD0</sub> = E<sub>VDD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = E<sub>VSS0</sub> = E<sub>VSS1</sub> = 0 V) (4/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V <sub>OH1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OH1</sub> = -10.0 mA	E <sub>VDD0</sub> - 1.5		V
			4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OH1</sub> = -3.0 mA	E <sub>VDD0</sub> - 0.7		V
			2.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OH1</sub> = -2.0 mA	E <sub>VDD0</sub> - 0.6		V
			1.8 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OH1</sub> = -1.5 mA	E <sub>VDD0</sub> - 0.5		V
			1.6 V ≤ E <sub>VDD0</sub> < 5.5 V, I <sub>OH1</sub> = -1.0 mA	E <sub>VDD0</sub> - 0.5		V
	V <sub>OH2</sub>	P20 to P27, P150 to P156	1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V, I <sub>OH2</sub> = -100 μA	V <sub>DD</sub> - 0.5		V
Output voltage, low	V <sub>OL1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 20 mA		1.3	V
			4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 8.5 mA		0.7	V
			2.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 3.0 mA		0.6	V
			2.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 1.5 mA		0.4	V
			1.8 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 0.6 mA		0.4	V
			1.6 V ≤ E <sub>VDD0</sub> < 5.5 V, I <sub>OL1</sub> = 0.3 mA		0.4	V
	V <sub>OL2</sub>	P20 to P27, P150 to P156	1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V, I <sub>OL2</sub> = 400 μA		0.4	V
	V <sub>OL3</sub>	P60 to P63	4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL3</sub> = 15.0 mA		2.0	V
			4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL3</sub> = 5.0 mA		0.4	V
			2.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL3</sub> = 3.0 mA		0.4	V
			1.8 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL3</sub> = 2.0 mA		0.4	V
			1.6 V ≤ E <sub>VDD0</sub> < 5.5 V, I <sub>OL3</sub> = 1.0 mA		0.4	V

**Caution** P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 2.3.2 Supply current characteristics

## (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ E<sub>VDD0</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = E<sub>VSS0</sub> = 0 V) (1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit		
Supply current <sup>Note 1</sup>	I <sub>DD1</sub>	Operating mode	HS (high-speed main) mode <sup>Note 5</sup>	f <sub>IH</sub> = 32 MHz <sup>Note 3</sup>	Basic operation	V <sub>DD</sub> = 5.0 V		2.1		mA	
						V <sub>DD</sub> = 3.0 V		2.1		mA	
					Normal operation	V <sub>DD</sub> = 5.0 V		4.6	7.0	mA	
						V <sub>DD</sub> = 3.0 V		4.6	7.0	mA	
				f <sub>IH</sub> = 24 MHz <sup>Note 3</sup>	Normal operation	V <sub>DD</sub> = 5.0 V		3.7	5.5	mA	
						V <sub>DD</sub> = 3.0 V		3.7	5.5	mA	
				f <sub>IH</sub> = 16 MHz <sup>Note 3</sup>	Normal operation	V <sub>DD</sub> = 5.0 V		2.7	4.0	mA	
						V <sub>DD</sub> = 3.0 V		2.7	4.0	mA	
				LS (low-speed main) mode <sup>Note 5</sup>	f <sub>IH</sub> = 8 MHz <sup>Note 3</sup>	Normal operation	V <sub>DD</sub> = 3.0 V		1.2	1.8	mA
							V <sub>DD</sub> = 2.0 V		1.2	1.8	mA
				LV (low-voltage main) mode <sup>Note 5</sup>	f <sub>IH</sub> = 4 MHz <sup>Note 3</sup>	Normal operation	V <sub>DD</sub> = 3.0 V		1.2	1.7	mA
							V <sub>DD</sub> = 2.0 V		1.2	1.7	mA
			HS (high-speed main) mode <sup>Note 5</sup>	f <sub>MX</sub> = 20 MHz <sup>Note 2</sup> , V <sub>DD</sub> = 5.0 V	Normal operation	Square wave input		3.0	4.6	mA	
						Resonator connection		3.2	4.8	mA	
					Normal operation	Square wave input		3.0	4.6	mA	
						Resonator connection		3.2	4.8	mA	
					f <sub>MX</sub> = 10 MHz <sup>Note 2</sup> , V <sub>DD</sub> = 5.0 V	Normal operation	Square wave input		1.9	2.7	mA
							Resonator connection		1.9	2.7	mA
					f <sub>MX</sub> = 10 MHz <sup>Note 2</sup> , V <sub>DD</sub> = 3.0 V	Normal operation	Square wave input		1.9	2.7	mA
							Resonator connection		1.9	2.7	mA
				LS (low-speed main) mode <sup>Note 5</sup>	f <sub>MX</sub> = 8 MHz <sup>Note 2</sup> , V <sub>DD</sub> = 3.0 V	Normal operation	Square wave input		1.1	1.7	mA
							Resonator connection		1.1	1.7	mA
					f <sub>MX</sub> = 8 MHz <sup>Note 2</sup> , V <sub>DD</sub> = 2.0 V	Normal operation	Square wave input		1.1	1.7	mA
							Resonator connection		1.1	1.7	mA
			Subsystem clock operation	f <sub>SUB</sub> = 32.768 kHz <sup>Note 4</sup> T <sub>A</sub> = −40°C	Normal operation	Square wave input		4.1	4.9	μA	
						Resonator connection		4.2	5.0	μA	
				f <sub>SUB</sub> = 32.768 kHz <sup>Note 4</sup> T <sub>A</sub> = +25°C	Normal operation	Square wave input		4.1	4.9	μA	
						Resonator connection		4.2	5.0	μA	
				f <sub>SUB</sub> = 32.768 kHz <sup>Note 4</sup> T <sub>A</sub> = +50°C	Normal operation	Square wave input		4.2	5.5	μA	
						Resonator connection		4.3	5.6	μA	
				f <sub>SUB</sub> = 32.768 kHz <sup>Note 4</sup> T <sub>A</sub> = +70°C	Normal operation	Square wave input		4.3	6.3	μA	
						Resonator connection		4.4	6.4	μA	
				f <sub>SUB</sub> = 32.768 kHz <sup>Note 4</sup> T <sub>A</sub> = +85°C	Normal operation	Square wave input		4.6	7.7	μA	
						Resonator connection		4.7	7.8	μA	

(Notes and Remarks are listed on the next page.)



**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)****(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

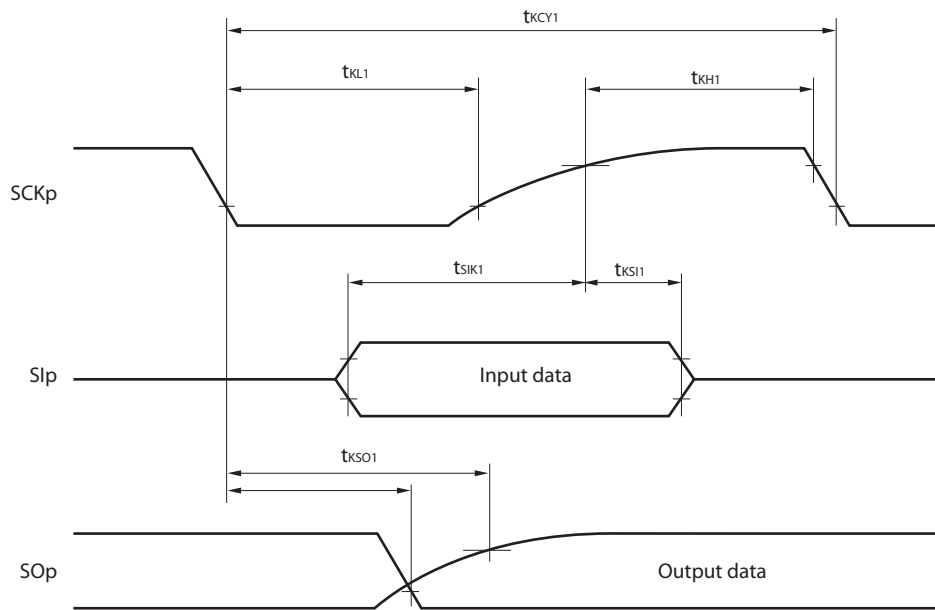
Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit	
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Transfer rate		Reception	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V			f <sub>MCK</sub> /6 Note 1		f <sub>MCK</sub> /6 Note 1		f <sub>MCK</sub> /6 Note 1	bps
						5.3		1.3		0.6	Mbps
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V			f <sub>MCK</sub> /6 Note 1		f <sub>MCK</sub> /6 Note 1		f <sub>MCK</sub> /6 Note 1	bps
						5.3		1.3		0.6	Mbps
			1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V			f <sub>MCK</sub> /6 Notes 1 to 3		f <sub>MCK</sub> /6 Notes 1, 2		f <sub>MCK</sub> /6 Notes 1, 2	bps
						5.3		1.3		0.6	Mbps

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.**2.** Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.**3.** The following conditions are required for low voltage interface when EV<sub>DD0</sub> < V<sub>DD</sub>.2.4 V ≤ EV<sub>DD0</sub> < 2.7 V : MAX. 2.6 Mbps1.8 V ≤ EV<sub>DD0</sub> < 2.4 V : MAX. 1.3 Mbps**4.** The maximum operating frequencies of the CPU/peripheral hardware clock (f<sub>CLK</sub>) are:HS (high-speed main) mode: 32 MHz (2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V)16 MHz (2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V)LS (low-speed main) mode: 8 MHz (1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V)LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V<sub>DD</sub> ≤ 5.5 V)

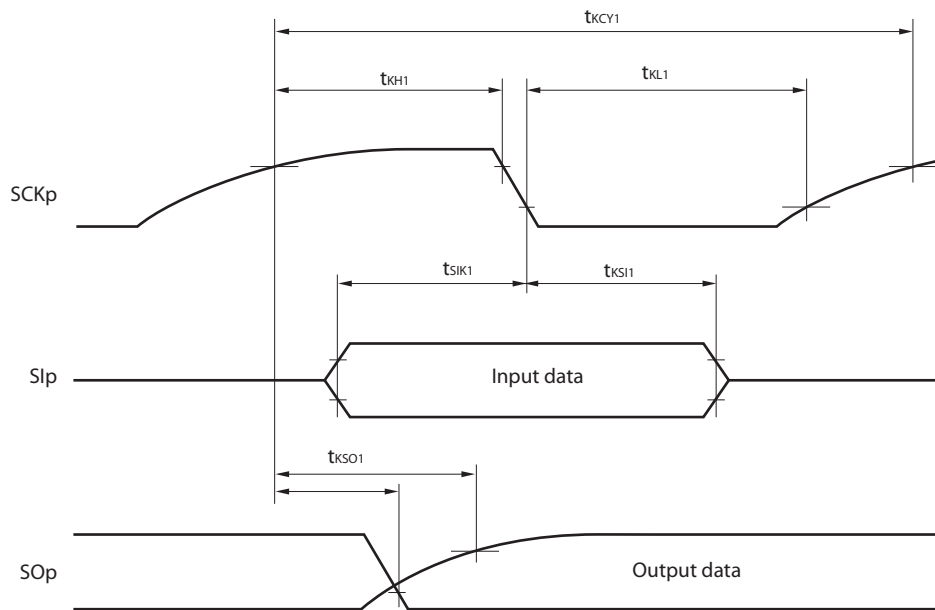
**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 20- to 52-pin products)/EV<sub>DD</sub> tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

**Remarks 1.** V<sub>b</sub>[V]: Communication line voltage**2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)**3.** f<sub>MCK</sub>: Serial array unit operation clock frequency(Operation clock to be set by the CKS<sub>mn</sub> bit of serial mode register mn (SMR<sub>mn</sub>). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))**4.** UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

**CSI mode serial transfer timing (master mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



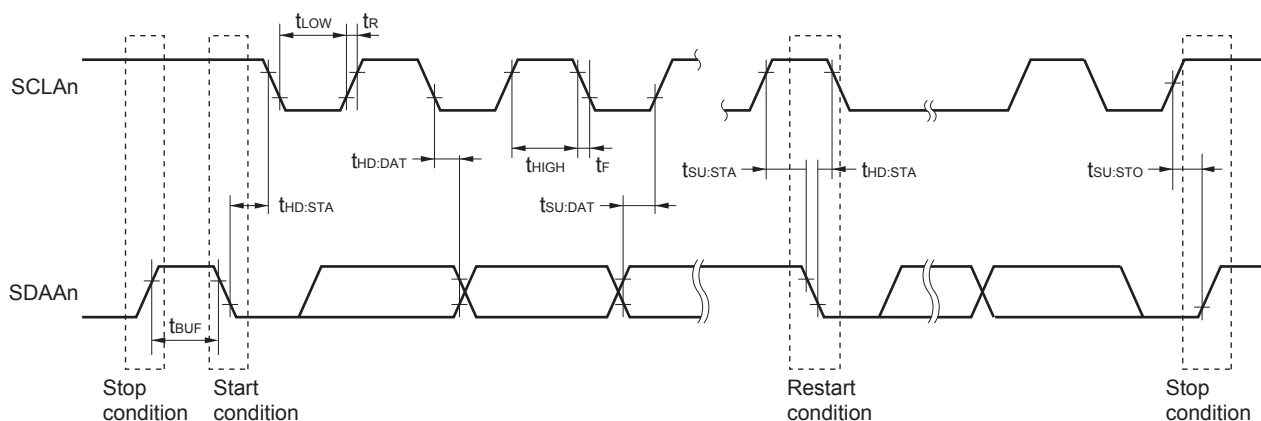
**CSI mode serial transfer timing (master mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



- Remarks**
1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
  2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**(3) I<sup>2</sup>C fast mode plus**(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f <sub>SCL</sub>	Fast mode plus: f <sub>CLK</sub> ≥ 10 MHz	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	0	1000	—	—	—	—	kHz
Setup time of restart condition	t <sub>SU:STA</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		0.26	—	—	—	—	—	μs
Hold time <sup>Note 1</sup>	t <sub>HD:STA</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		0.26	—	—	—	—	—	μs
Hold time when SCLA0 = "L"	t <sub>LOW</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		0.5	—	—	—	—	—	μs
Hold time when SCLA0 = "H"	t <sub>HIGH</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		0.26	—	—	—	—	—	μs
Data setup time (reception)	t <sub>SU:DAT</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		50	—	—	—	—	—	μs
Data hold time (transmission) <sup>Note 2</sup>	t <sub>HD:DAT</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		0	0.45	—	—	—	—	μs
Setup time of stop condition	t <sub>SU:STO</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		0.26	—	—	—	—	—	μs
Bus-free time	t <sub>BUF</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		0.5	—	—	—	—	—	μs

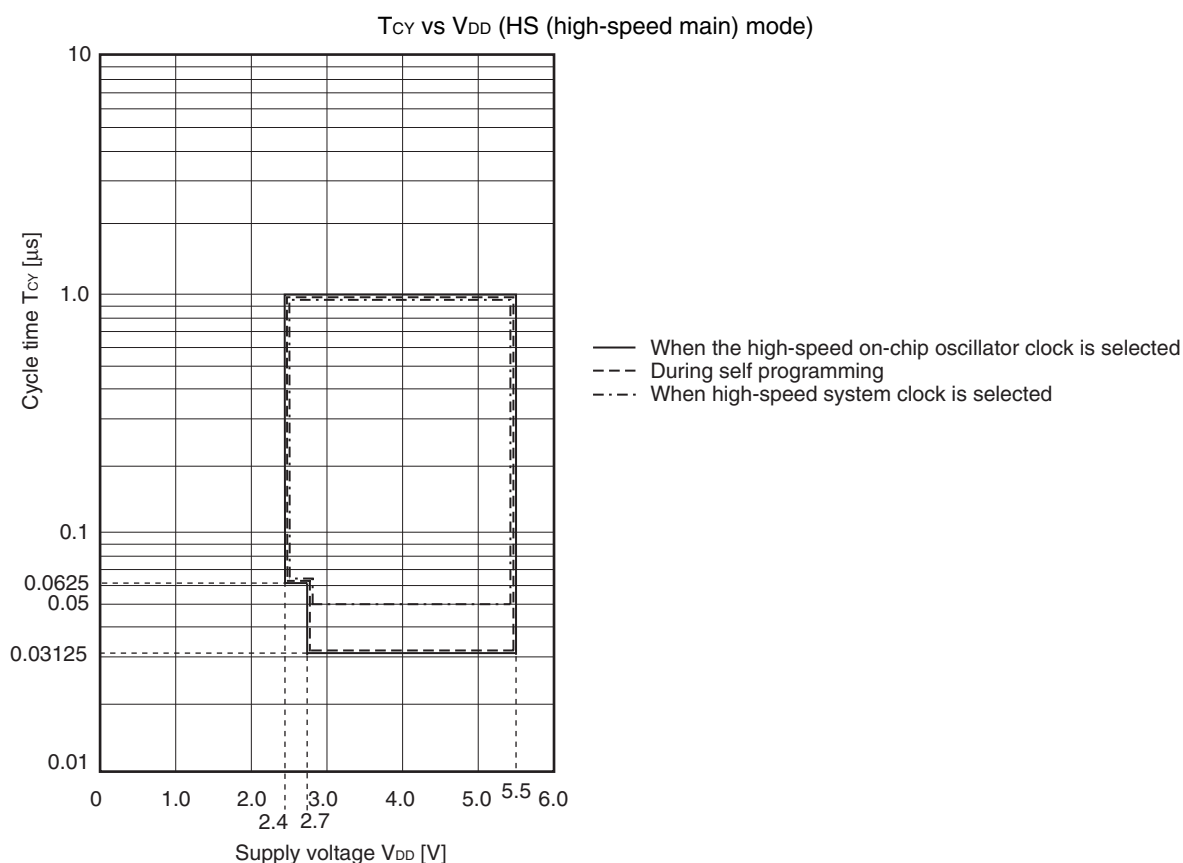
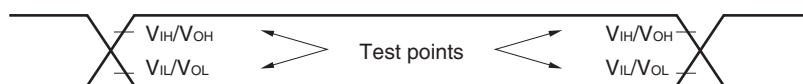
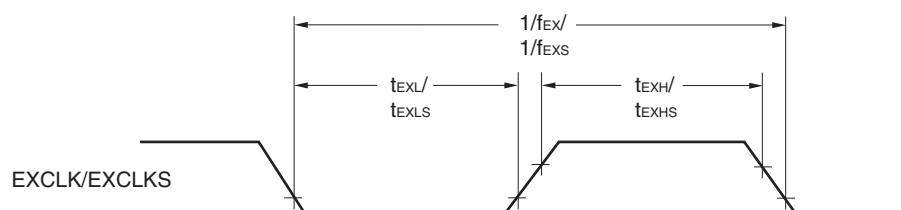
**Notes** 1. The first clock pulse is generated after this period when the start/restart condition is detected.<R> 2. The maximum value (MAX.) of t<sub>HD:DAT</sub> is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.**Caution** The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I<sub>OH1</sub>, I<sub>OL1</sub>, V<sub>OH1</sub>, V<sub>OL1</sub>) must satisfy the values in the redirect destination.**Remark** The maximum value of C<sub>b</sub> (communication line capacitance) and the value of R<sub>b</sub> (communication line pull-up resistor) at that time in each mode are as follows.Fast mode plus: C<sub>b</sub> = 120 pF, R<sub>b</sub> = 1.1 kΩ**I<sup>2</sup>C serial transfer timing****Remark** n = 0, 1

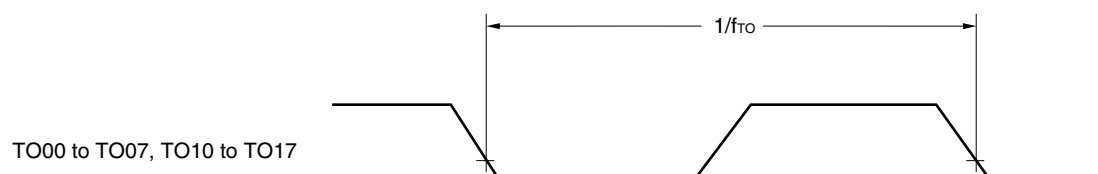
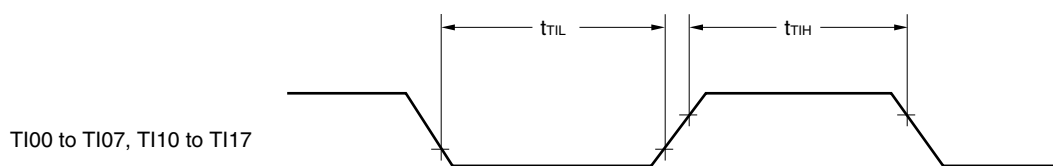
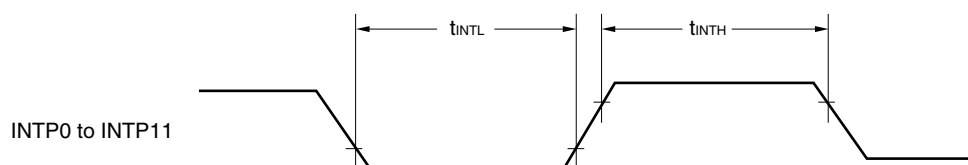
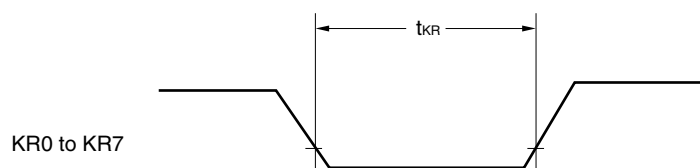
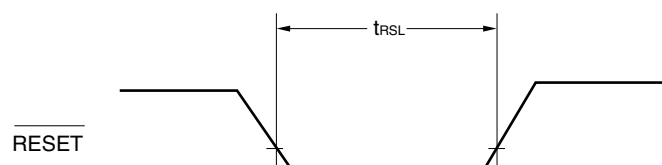
- Notes**
1. Total current flowing into  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , or  $V_{SS}$ ,  $EV_{SS0}$ , and  $EV_{SS1}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. When high-speed on-chip oscillator and subsystem clock are stopped.
  3. When high-speed system clock and subsystem clock are stopped.
  4. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $AMPHS1 = 1$  (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

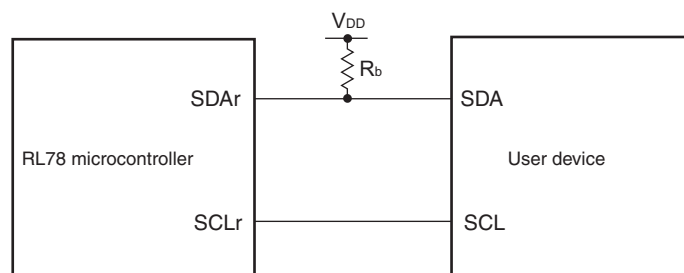
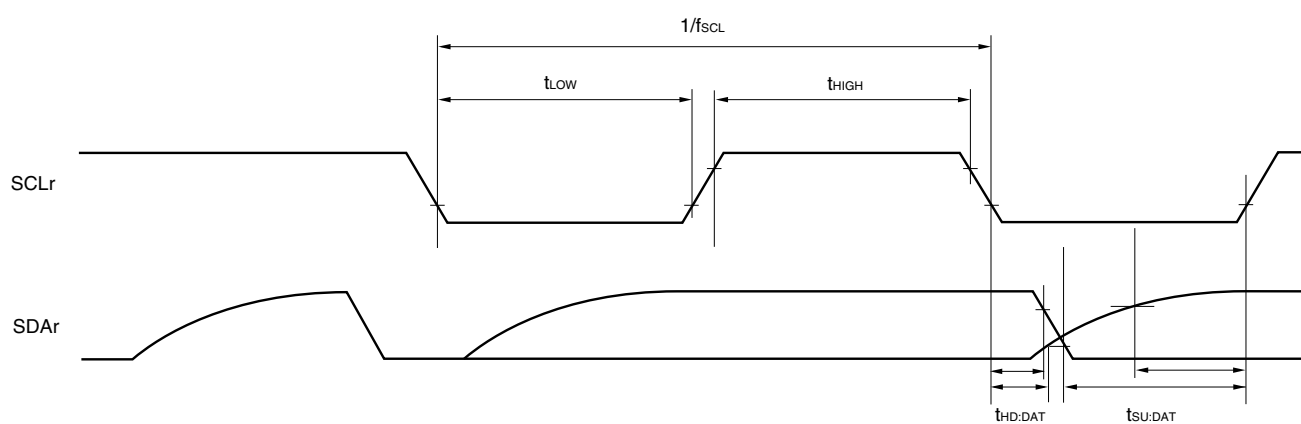
HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$

$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

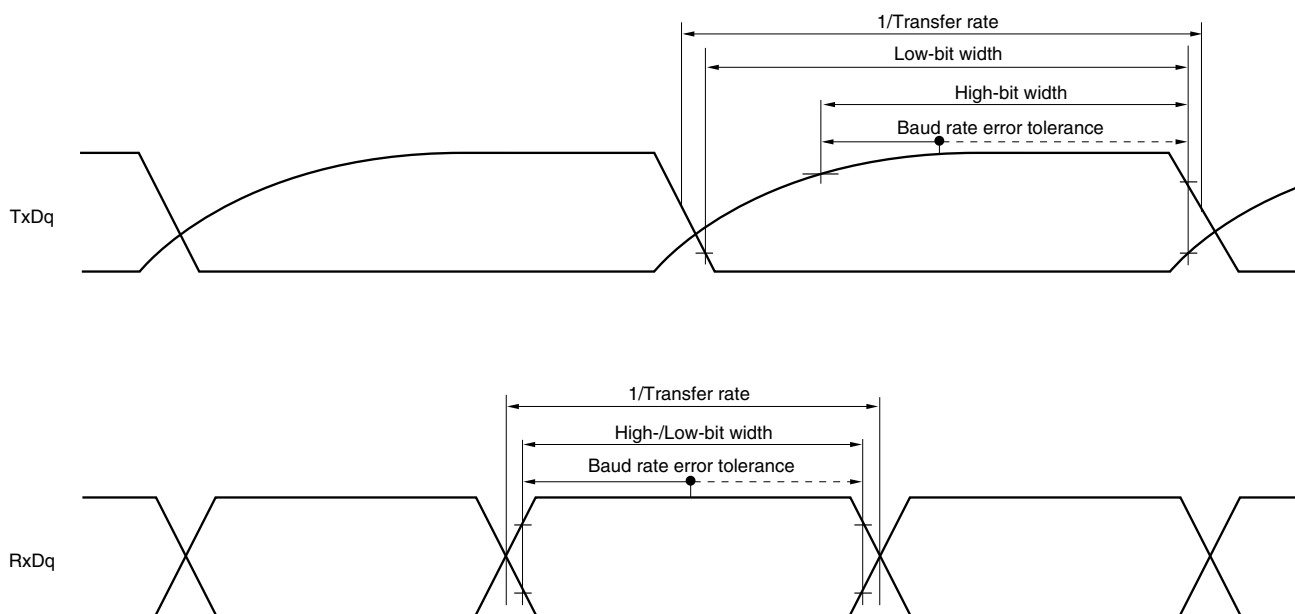
- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$

**Minimum Instruction Execution Time during Main System Clock Operation****AC Timing Test Points****External System Clock Timing**

**TI/TO Timing****Interrupt Request Input Timing****Key Interrupt Input Timing****RESET Input Timing**

**Simplified I<sup>2</sup>C mode connection diagram (during communication at same potential)****Simplified I<sup>2</sup>C mode serial transfer timing (during communication at same potential)**

- Remarks**
- $R_b[\Omega]$ : Communication line (SDAr) pull-up resistance,  $C_b[F]$ : Communication line (SDAr, SCLr) load capacitance
  - r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14),  
h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)
  - $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

**UART mode bit width (during communication at different potential) (reference)**

- Remarks**
1.  $R_b[\Omega]$ : Communication line (TxDq) pull-up resistance,  
 $C_b[F]$ : Communication line (TxDq) load capacitance,  $V_b[V]$ : Communication line voltage
  2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
  3.  $f_{MCK}$ : Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))
  4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.



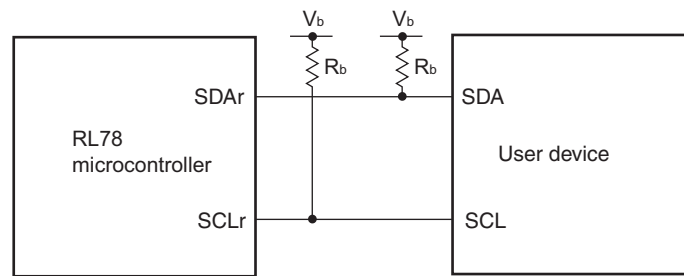
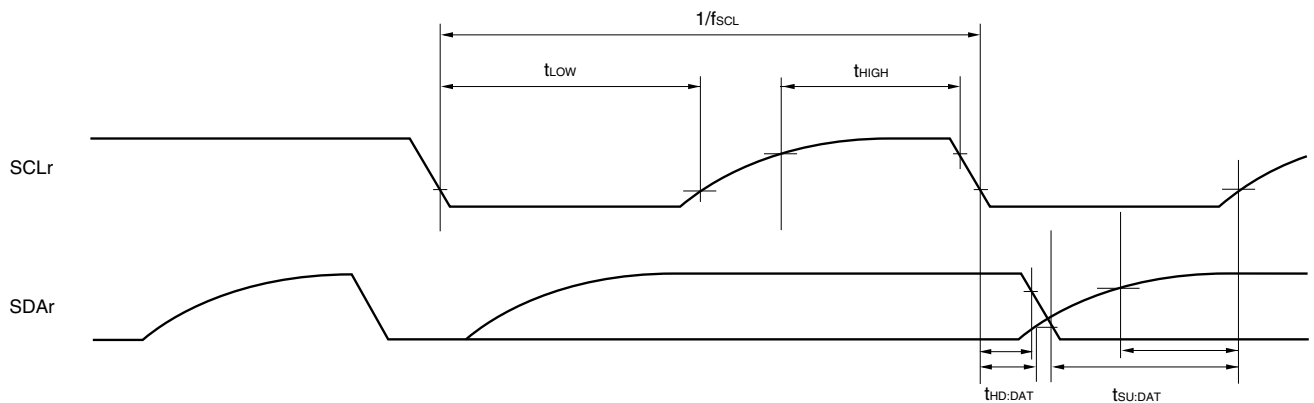
**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I<sup>2</sup>C mode) (2/2)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Data setup time (reception)	$t_{\text{SU:DAT}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 340$ Note 2		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 340$ Note 2		ns
		$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 2.8\text{ k}\Omega$	$1/f_{\text{MCK}} + 760$ Note 2		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 760$ Note 2		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$	$1/f_{\text{MCK}} + 570$ Note 2		ns
Data hold time (transmission)	$t_{\text{HD:DAT}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	0	770	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	0	770	ns
		$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 2.8\text{ k}\Omega$	0	1420	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	0	1420	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$	0	1215	ns

**Notes** 1. The value must also be equal to or less than  $f_{\text{MCK}}/4$ .2. Set the  $f_{\text{MCK}}$  value to keep the hold time of  $\text{SCLr} = \text{"L"}$  and  $\text{SCLr} = \text{"H"}$ .

**Caution** Select the TTL input buffer and the N-ch open drain output ( $\text{V}_{\text{DD}}$  tolerance (for the 20- to 52-pin products)/ $\text{EV}_{\text{DD}}$  tolerance (for the 64- to 100-pin products)) mode for the  $\text{SDAr}$  pin and the N-ch open drain output ( $\text{V}_{\text{DD}}$  tolerance (for the 20- to 52-pin products)/ $\text{EV}_{\text{DD}}$  tolerance (for the 64- to 100-pin products)) mode for the  $\text{SCLr}$  pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $\text{V}_{\text{IH}}$  and  $\text{V}_{\text{IL}}$ , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

**Simplified I<sup>2</sup>C mode connection diagram (during communication at different potential)****Simplified I<sup>2</sup>C mode serial transfer timing (during communication at different potential)**

**Caution** Select the TTL input buffer and the N-ch open drain output ( $V_{DD}$  tolerance (for the 20- to 52-pin products)/ $EV_{DD}$  tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output ( $V_{DD}$  tolerance (for the 20- to 52-pin products)/ $EV_{DD}$  tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.

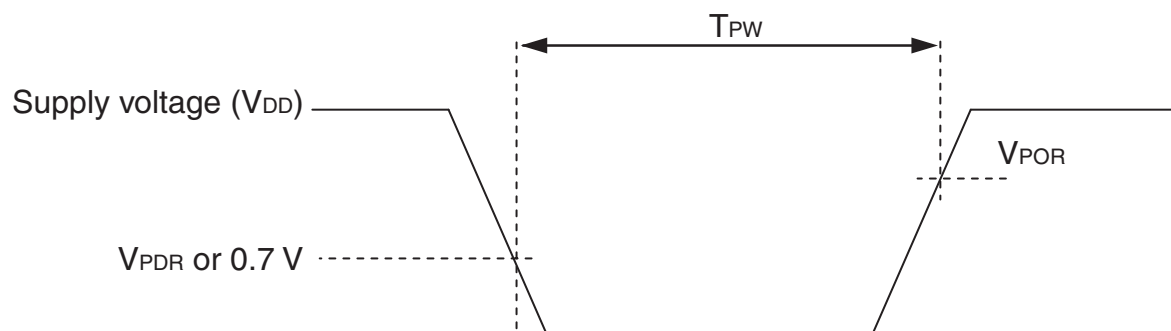
- Remarks**
1.  $R_b[\Omega]$ : Communication line (SDAr, SCLr) pull-up resistance,  $C_b[F]$ : Communication line (SDAr, SCLr) load capacitance,  $V_b[V]$ : Communication line voltage
  2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)
  3.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

## 3.6.3 POR circuit characteristics

 $(T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0$  V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	$V_{POR}$	Power supply rise time	1.45	1.51	1.57	V
	$V_{PDR}$	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width	$T_{PW}$		300			$\mu\text{s}$

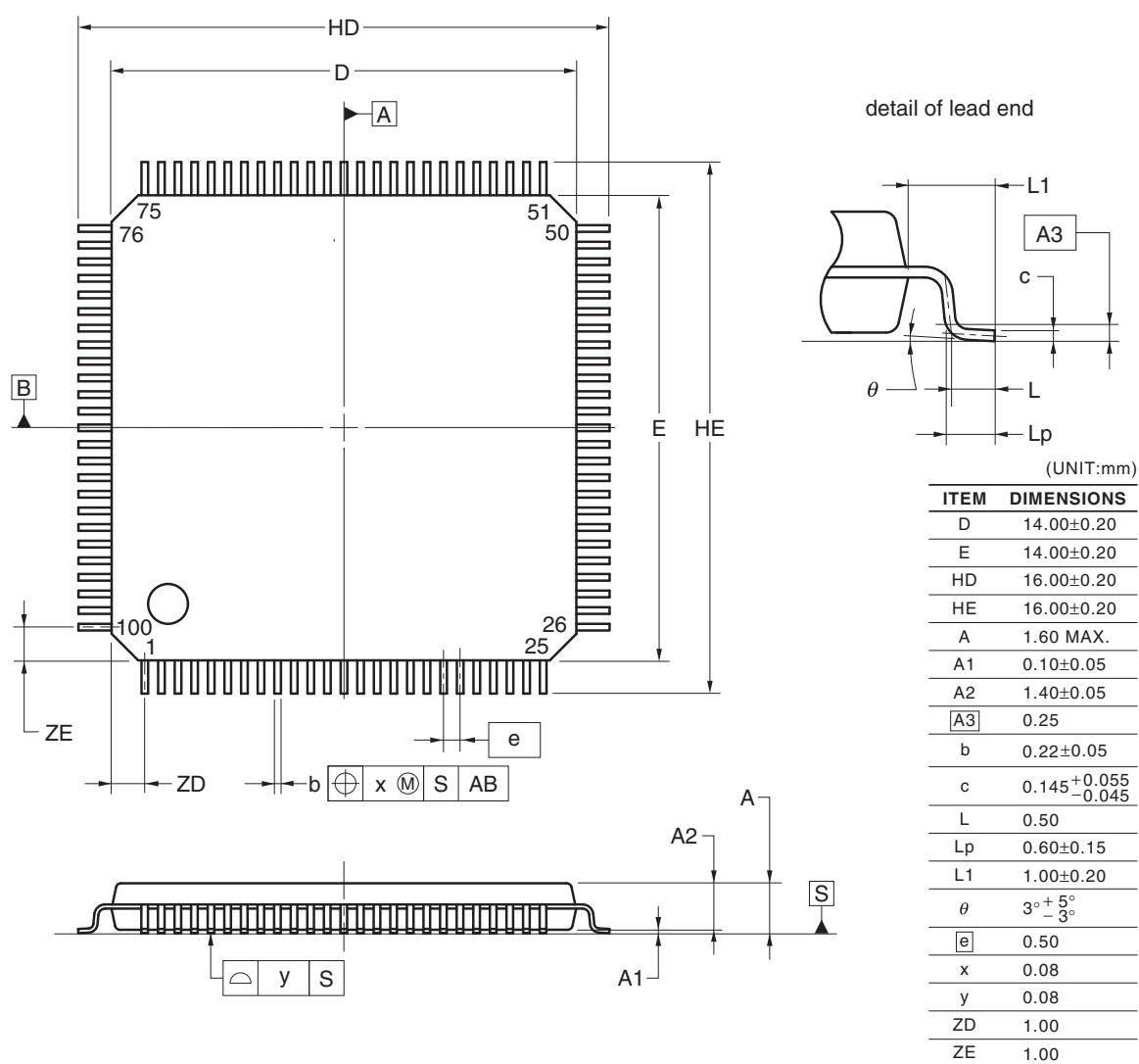
**Note** Minimum time required for a POR reset when  $V_{DD}$  exceeds below  $V_{PDR}$ . This is also the minimum time required for a POR reset from when  $V_{DD}$  exceeds below 0.7 V to when  $V_{DD}$  exceeds  $V_{POR}$  while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



## 4.13 100-pin Products

R5F100PFAFB, R5F100PGAFA, R5F100PHAFA, R5F100PJAFB, R5F100PKAFB, R5F100PLAFB  
 R5F101PFAFB, R5F101PGAFA, R5F101PHAFA, R5F101PJAFB, R5F101PKAFB, R5F101PLAFB  
 R5F100PFDFA, R5F100PGDFA, R5F100PHDFA, R5F100PJDFB, R5F100PKDFA, R5F100PLDFA  
 R5F101PFDFA, R5F101PGDFA, R5F101PHDFA, R5F101PJDFB, R5F101PKDFA, R5F101PLDFA  
 R5F100PFGFB, R5F100PGGFB, R5F100PHGFB, R5F100PJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69



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