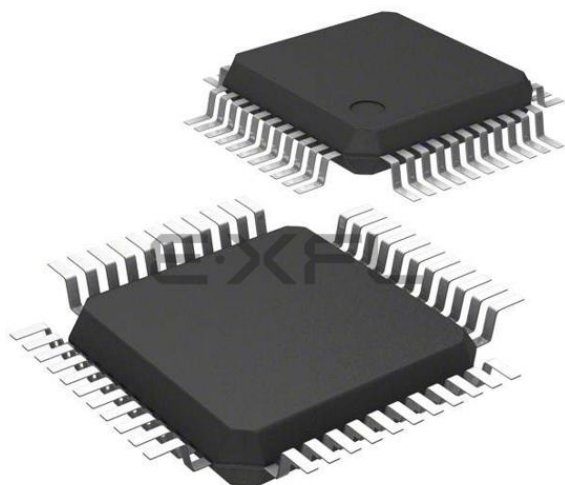




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100ffa-fp-v0

Table 1-1. List of Ordering Part Numbers

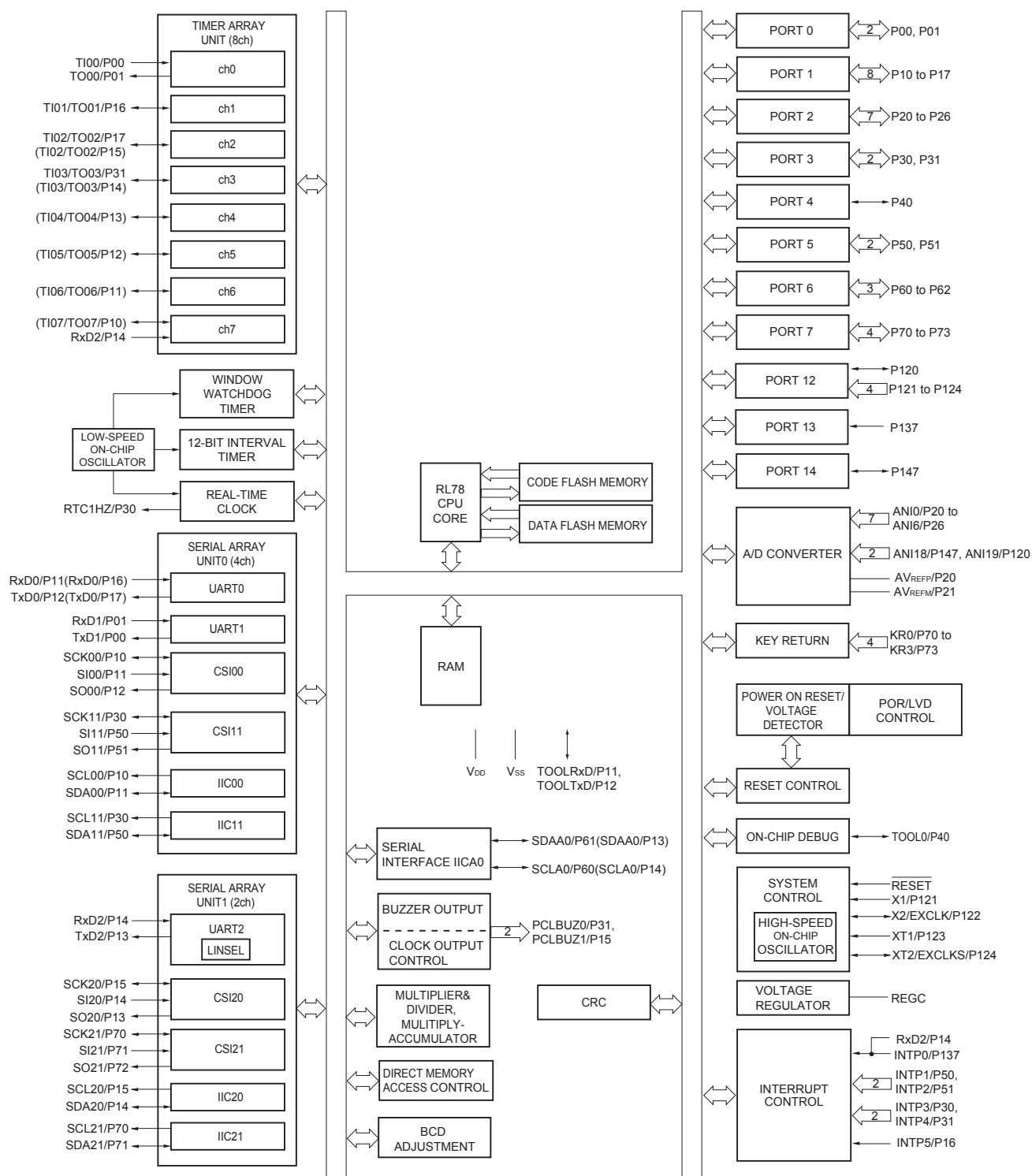
(9/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
64 pins	64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)	Mounted	A	R5F100LCAFB#V0, R5F100LDAFB#V0, R5F100LEAFB#V0, R5F100LFAFB#V0, R5F100LGAFB#V0, R5F100LHAFB#V0, R5F100LJAFB#V0, R5F100LKAFB#V0, R5F100LLAFB#V0 R5F100LCAFB#X0, R5F100LDAFB#X0, R5F100LEAFB#X0, R5F100LFAFB#X0, R5F100LGAFB#X0, R5F100LHAFB#X0, R5F100LJAFB#X0, R5F100LKAFB#X0, R5F100LLAFB#X0
			D	R5F100LCDFB#V0, R5F100LDDFB#V0, R5F100LEDFB#V0, R5F100LFDDB#V0, R5F100LGDFB#V0, R5F100LHDFB#V0, R5F100LJDFB#V0, R5F100LKDFB#V0, R5F100LLDFB#V0 R5F100LCDFB#X0, R5F100LDDFB#X0, R5F100LEDFB#X0, R5F100LFDDB#X0, R5F100LGDFB#X0, R5F100LHDFB#X0, R5F100LJDFB#X0, R5F100LKDFB#X0, R5F100LLDFB#X0
			G	R5F100LCGFB#V0, R5F100LDGFB#V0, R5F100LEGFB#V0, R5F100LFGFB#V0 R5F100LCGFB#X0, R5F100LDGFB#X0, R5F100LEGFB#X0, R5F100LFGFB#X0
				R5F100LGGFB#V0, R5F100LHGFB#V0, R5F100LJGFB#V0, R5F100LGGFB#X0, R5F100LHGFB#X0, R5F100LJGFB#X0
	64-pin plastic VFPGA (4 × 4 mm, 0.4 mm pitch)	Not mounted	A	R5F101LCAFB#V0, R5F101LDAFB#V0, R5F101LEAFB#V0, R5F101LFAFB#V0, R5F101LGAFB#V0, R5F101LHAFB#V0, R5F101LJAFB#V0, R5F101LKAFB#V0, R5F101LLAFB#V0 R5F101LCAFB#X0, R5F101LDAFB#X0, R5F101LEAFB#X0, R5F101LFAFB#X0, R5F101LGAFB#X0, R5F101LHAFB#X0, R5F101LJAFB#X0, R5F101LKAFB#X0, R5F101LLAFB#X0
			D	R5F101LCDFB#V0, R5F101LDDFB#V0, R5F101LEDFB#V0, R5F101LFDDB#V0, R5F101LGDFB#V0, R5F101LHDFB#V0, R5F101LJDFB#V0, R5F101LKDFB#V0, R5F101LLDFB#V0 R5F101LCDFB#X0, R5F101LDDFB#X0, R5F101LEDFB#X0, R5F101LFDDB#X0, R5F101LGDFB#X0, R5F101LHDFB#X0, R5F101LJDFB#X0, R5F101LKDFB#X0, R5F101LLDFB#X0
	64-pin plastic VFPGA (4 × 4 mm, 0.4 mm pitch)	Mounted	A	R5F100LCABG#U0, R5F100LDABG#U0, R5F100LEABG#U0, R5F100LFABG#U0, R5F100LGABG#U0, R5F100LHABG#U0, R5F100LJABG#U0 R5F100LCABG#W0, R5F100LDABG#W0, R5F100LEABG#W0, R5F100LFABG#W0, R5F100LGABG#W0, R5F100LHABG#W0, R5F100LJABG#W0
			G	R5F100LCGBG#U0, R5F100LDGBG#U0, R5F100LEGBG#U0, R5F100LFGBG#U0, R5F100LGGBG#U0, R5F100LHGBG#U0, R5F100LJGBG#U0 R5F100LCGBG#W0, R5F100LDGBG#W0, R5F100LEGBG#W0, R5F100LFGBG#W0, R5F100LGGBG#W0, R5F100LHGBG#W0, R5F100LJGBG#W0
	64-pin plastic VFPGA (4 × 4 mm, 0.4 mm pitch)	Not mounted	A	R5F101LCABG#U0, R5F101LDABG#U0, R5F101LEABG#U0, R5F101LFABG#U0, R5F101LGABG#U0, R5F101LHABG#U0, R5F101LJABG#U0 R5F101LCABG#W0, R5F101LDABG#W0, R5F101LEABG#W0, R5F101LFABG#W0, R5F101LGABG#W0, R5F101LHABG#W0, R5F101LJABG#W0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

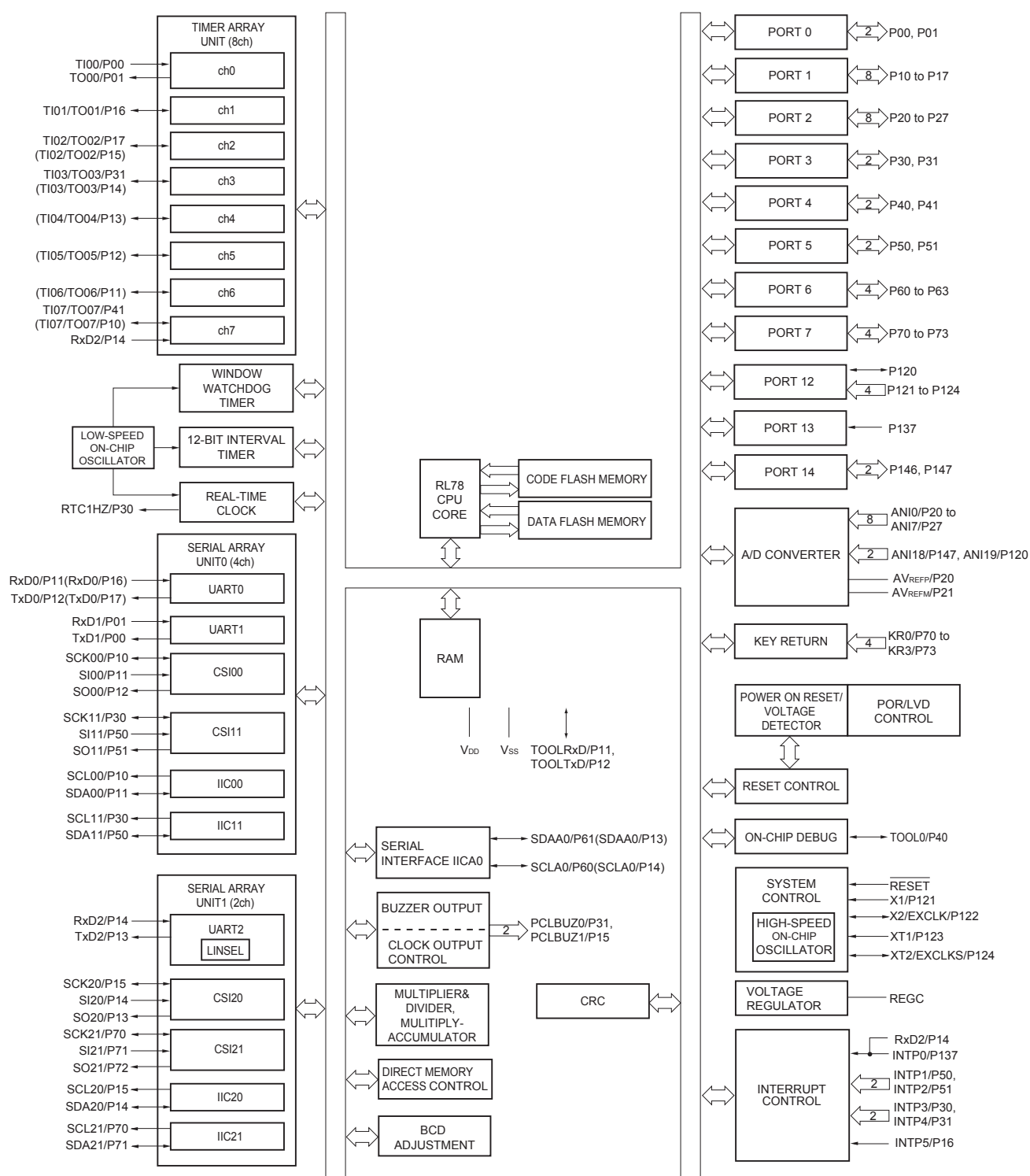
Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.5.7 40-pin products



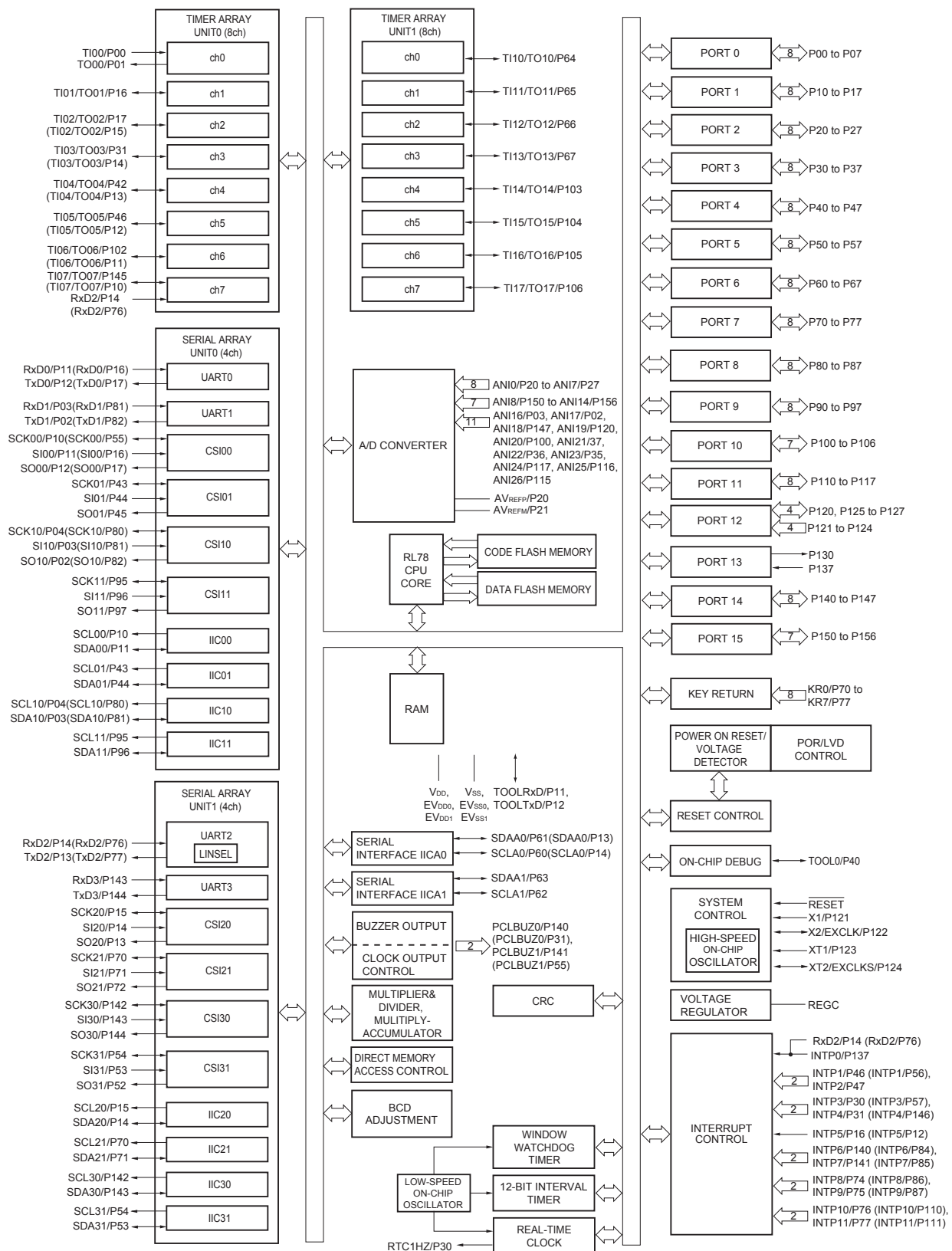
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.8 44-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

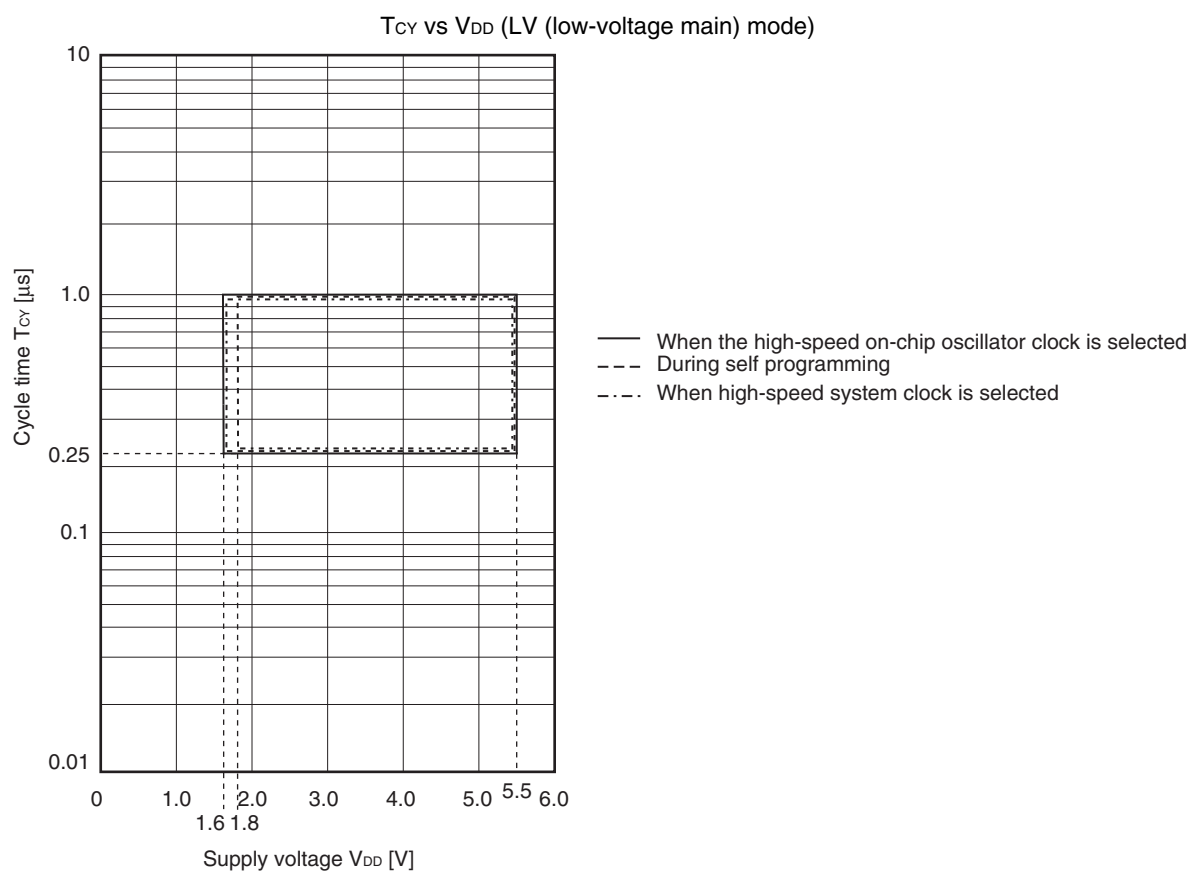
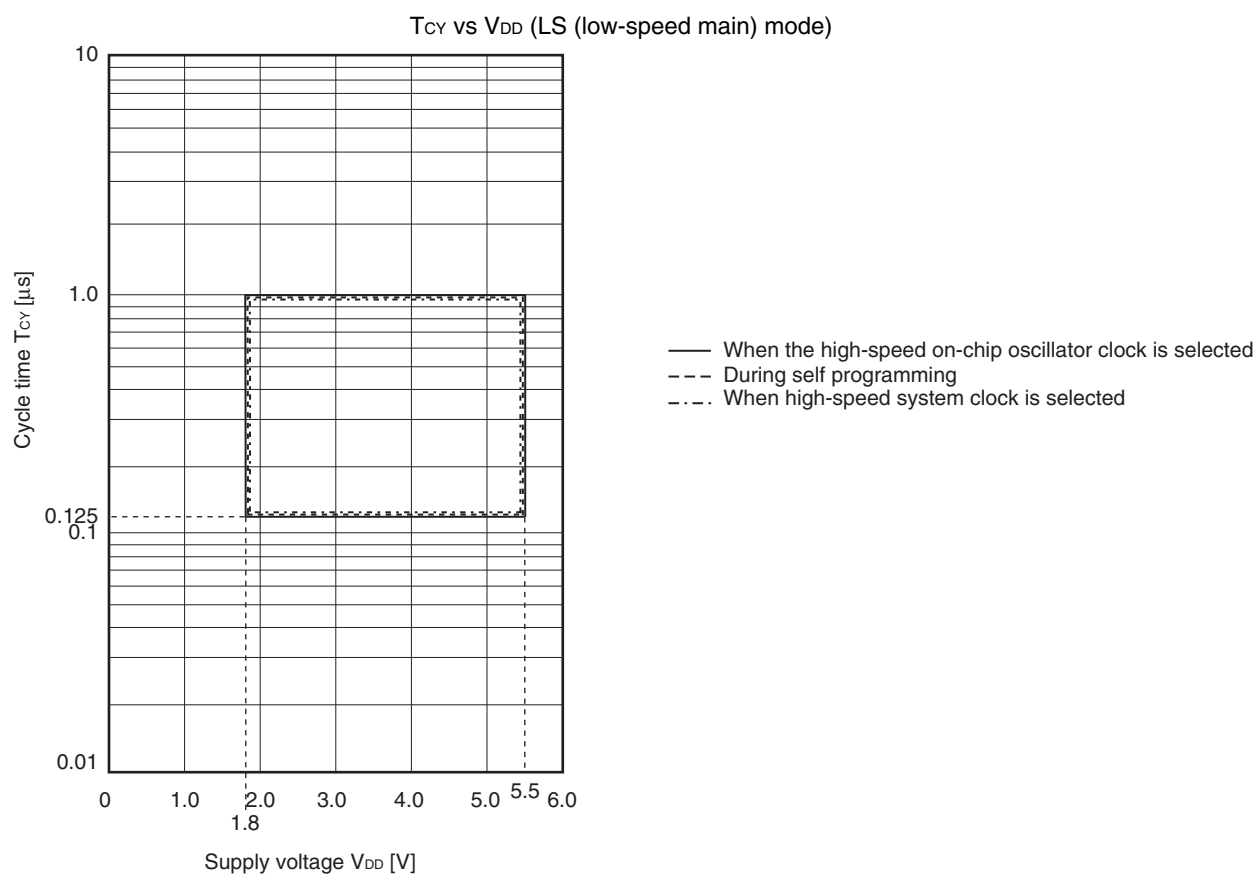
1.5.14 128-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

- Notes**
1. Total current flowing into V_{DD} , EV_{DD0} , and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} , and EV_{DD1} , or V_{SS} , EV_{SS0} , and EV_{SS1} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 32 MHz
 - $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 16 MHz
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 8 MHz
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 4 MHz
 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f_{IH}: High-speed on-chip oscillator clock frequency
3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C



(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2)

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK2}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} +20		1/f _{MCK} +30		1/f _{MCK} +30		ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} +30		1/f _{MCK} +30		1/f _{MCK} +30		ns
		1.7 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} +40		1/f _{MCK} +40		1/f _{MCK} +40		ns
		1.6 V ≤ EV _{DD0} ≤ 5.5 V		—		1/f _{MCK} +40		1/f _{MCK} +40		ns
Slp hold time (from SCKp↑) ^{Note 2}	t _{KSI2}	1.8 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} +31		1/f _{MCK} +31		1/f _{MCK} +31		ns
		1.7 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} +250		1/f _{MCK} +250		1/f _{MCK} +250		ns
		1.6 V ≤ EV _{DD0} ≤ 5.5 V		—		1/f _{MCK} +250		1/f _{MCK} +250		ns
Delay time from SCKp↓ to SOp output ^{Note 3}	t _{KSO2}	C = 30 pF ^{Note 4}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		2/f _{MCK} +44		2/f _{MCK} +110		2/f _{MCK} +110	ns
			2.4 V ≤ EV _{DD0} ≤ 5.5 V		2/f _{MCK} +75		2/f _{MCK} +110		2/f _{MCK} +110	ns
			1.8 V ≤ EV _{DD0} ≤ 5.5 V		2/f _{MCK} +110		2/f _{MCK} +110		2/f _{MCK} +110	ns
			1.7 V ≤ EV _{DD0} ≤ 5.5 V		2/f _{MCK} +220		2/f _{MCK} +220		2/f _{MCK} +220	ns
			1.6 V ≤ EV _{DD0} ≤ 5.5 V		—		2/f _{MCK} +220		2/f _{MCK} +220	ns

- Notes**
1. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp setup time becomes “to SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 2. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp hold time becomes “from SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 3. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The delay time to SOp output becomes “from SCKp↑” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 4. C is the load capacitance of the SOp output lines.
 5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)
 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

2.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode(T_A = -40 to +85°C, V_{PDR} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Detection voltage	Supply voltage level	V _{LVD0}	Power supply rise time	3.98	4.06	4.14	V		
			Power supply fall time	3.90	3.98	4.06	V		
		V _{LVD1}	Power supply rise time	3.68	3.75	3.82	V		
			Power supply fall time	3.60	3.67	3.74	V		
		V _{LVD2}	Power supply rise time	3.07	3.13	3.19	V		
			Power supply fall time	3.00	3.06	3.12	V		
		V _{LVD3}	Power supply rise time	2.96	3.02	3.08	V		
			Power supply fall time	2.90	2.96	3.02	V		
		V _{LVD4}	Power supply rise time	2.86	2.92	2.97	V		
			Power supply fall time	2.80	2.86	2.91	V		
		V _{LVD5}	Power supply rise time	2.76	2.81	2.87	V		
			Power supply fall time	2.70	2.75	2.81	V		
		V _{LVD6}	Power supply rise time	2.66	2.71	2.76	V		
			Power supply fall time	2.60	2.65	2.70	V		
		V _{LVD7}	Power supply rise time	2.56	2.61	2.66	V		
			Power supply fall time	2.50	2.55	2.60	V		
		V _{LVD8}	Power supply rise time	2.45	2.50	2.55	V		
			Power supply fall time	2.40	2.45	2.50	V		
		V _{LVD9}	Power supply rise time	2.05	2.09	2.13	V		
			Power supply fall time	2.00	2.04	2.08	V		
		V _{LVD10}	Power supply rise time	1.94	1.98	2.02	V		
			Power supply fall time	1.90	1.94	1.98	V		
		V _{LVD11}	Power supply rise time	1.84	1.88	1.91	V		
			Power supply fall time	1.80	1.84	1.87	V		
		V _{LVD12}	Power supply rise time	1.74	1.77	1.81	V		
			Power supply fall time	1.70	1.73	1.77	V		
		V _{LVD13}	Power supply rise time	1.64	1.67	1.70	V		
			Power supply fall time	1.60	1.63	1.66	V		
		Minimum pulse width		t _{LW}		300			μs
		Detection delay time						300	μs

2.8 Flash Memory Programming Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C_{erwr}	Retained for 20 years $T_A = 85^\circ\text{C}$	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 years $T_A = 25^\circ\text{C}$		1,000,000		
		Retained for 5 years $T_A = 85^\circ\text{C}$	100,000			
		Retained for 20 years $T_A = 85^\circ\text{C}$	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A = -40$ to $+105^\circ\text{C}$)

This chapter describes the following electrical specifications.

Target products G: Industrial applications $T_A = -40$ to $+105^\circ\text{C}$
R5F100xxGxx

- Cautions 1.** The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
- 2.** With products not provided with an EV_{DD0} , EV_{DD1} , EV_{SS0} , or EV_{SS1} pin, replace EV_{DD0} and EV_{DD1} with V_{DD} , or replace EV_{SS0} and EV_{SS1} with V_{SS} .
- 3.** The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions for each product.
- 4.** Please contact Renesas Electronics sales office for derating of operation under $T_A = +85^\circ\text{C}$ to $+105^\circ\text{C}$. Derating is the systematic reduction of load for the sake of improved reliability.

Remark When RL78/G13 is used in the range of $T_A = -40$ to $+85^\circ\text{C}$, see **CHAPTER 2 ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+85^\circ\text{C}$)**.

There are following differences between the products "G: Industrial applications ($T_A = -40$ to $+105^\circ\text{C}$)" and the products "A: Consumer applications, and D: Industrial applications".

Parameter	Application	
	A: Consumer applications, D: Industrial applications	G: Industrial applications
Operating ambient temperature	$T_A = -40$ to $+85^\circ\text{C}$	$T_A = -40$ to $+105^\circ\text{C}$
Operating mode Operating voltage range	HS (high-speed main) mode: $2.7\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$ $2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$ LS (low-speed main) mode: $1.8\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$ LV (low-voltage main) mode: $1.6\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$	HS (high-speed main) mode only: $2.7\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$ $2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
High-speed on-chip oscillator clock accuracy	$1.8\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ $\pm 1.0\% @ T_A = -20$ to $+85^\circ\text{C}$ $\pm 1.5\% @ T_A = -40$ to -20°C $1.6\text{ V} \leq \text{V}_{\text{DD}} < 1.8\text{ V}$ $\pm 5.0\% @ T_A = -20$ to $+85^\circ\text{C}$ $\pm 5.5\% @ T_A = -40$ to -20°C	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ $\pm 2.0\% @ T_A = +85$ to $+105^\circ\text{C}$ $\pm 1.0\% @ T_A = -20$ to $+85^\circ\text{C}$ $\pm 1.5\% @ T_A = -40$ to -20°C
Serial array unit	UART CSI: $f_{\text{CLK}}/2$ (supporting 16 Mbps), $f_{\text{CLK}}/4$ Simplified I ² C communication	UART CSI: $f_{\text{CLK}}/4$ Simplified I ² C communication
IICA	Normal mode Fast mode Fast mode plus	Normal mode Fast mode
Voltage detector	Rise detection voltage: 1.67 V to 4.06 V (14 levels) Fall detection voltage: 1.63 V to 3.98 V (14 levels)	Rise detection voltage: 2.61 V to 4.06 V (8 levels) Fall detection voltage: 2.55 V to 3.98 V (8 levels)

(Remark is listed on the next page.)

Absolute Maximum Ratings ($T_A = 25^{\circ}\text{C}$) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I _{OH1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	−70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	−100	mA
	I _{OH2}	Per pin	P20 to P27, P150 to P156	−0.5	mA
		Total of all pins		−2	mA
	Output current, low	I _{OL1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40
Total of all pins 170 mA			P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
I _{OL2}		Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature		T _A	In normal operation mode		−40 to +105
	In flash memory programming mode				
Storage temperature	T _{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD0} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I _{DD1}	Operating mode	HS (high-speed main) mode Note 5	$f_{IH} = 32\text{ MHz}$ Note 3	Basic operation	$V_{DD} = 5.0\text{ V}$		2.1		mA
						$V_{DD} = 3.0\text{ V}$		2.1		mA
					Normal operation	$V_{DD} = 5.0\text{ V}$		4.6	7.5	mA
						$V_{DD} = 3.0\text{ V}$		4.6	7.5	mA
				$f_{IH} = 24\text{ MHz}$ Note 3	Normal operation	$V_{DD} = 5.0\text{ V}$		3.7	5.8	mA
						$V_{DD} = 3.0\text{ V}$		3.7	5.8	mA
				$f_{IH} = 16\text{ MHz}$ Note 3	Normal operation	$V_{DD} = 5.0\text{ V}$		2.7	4.2	mA
						$V_{DD} = 3.0\text{ V}$		2.7	4.2	mA
			HS (high-speed main) mode Note 5	$f_{MX} = 20\text{ MHz}$ Note 2, $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	mA
				$f_{MX} = 20\text{ MHz}$ Note 2, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	mA
				$f_{MX} = 10\text{ MHz}$ Note 2, $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	mA
				$f_{MX} = 10\text{ MHz}$ Note 2, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	mA
		Subsystem clock operation		$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = -40^\circ\text{C}$	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +25^\circ\text{C}$	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +50^\circ\text{C}$	Normal operation	Square wave input		4.2	5.5	μA
						Resonator connection		4.3	5.6	μA
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +70^\circ\text{C}$	Normal operation	Square wave input		4.3	6.3	μA
						Resonator connection		4.4	6.4	μA
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +85^\circ\text{C}$	Normal operation	Square wave input		4.6	7.7	μA
						Resonator connection		4.7	7.8	μA
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +105^\circ\text{C}$	Normal operation	Square wave input		6.9	19.7	μA
						Resonator connection		7.0	19.8	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} and EV_{DD0} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

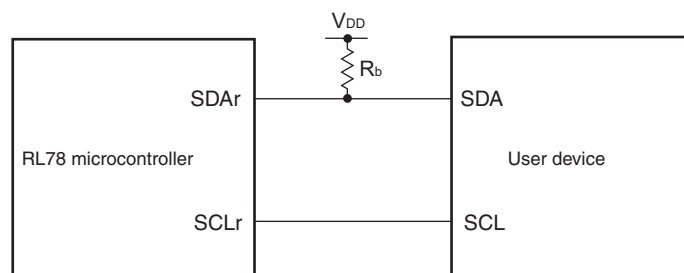
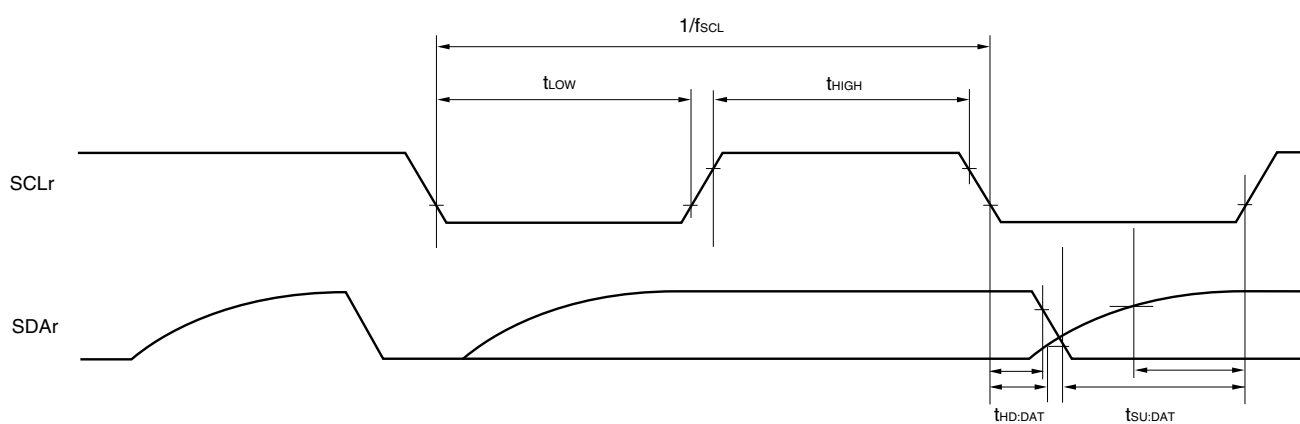
- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

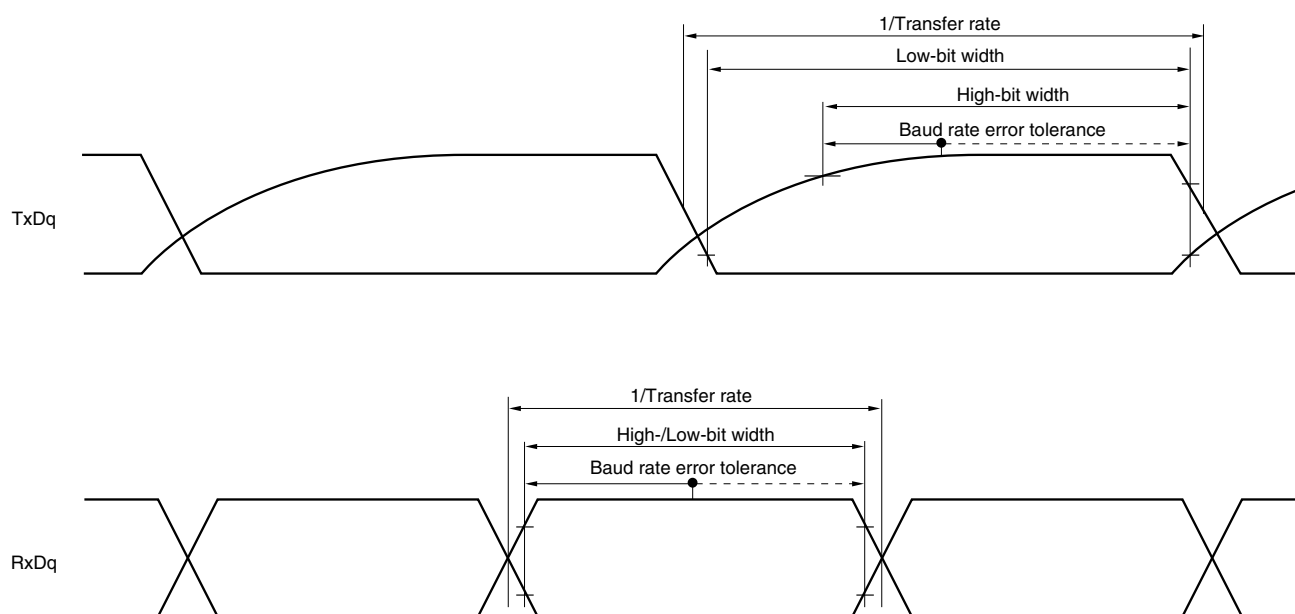
(TA = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I _{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f _{IH} = 32 MHz ^{Note 4}	V _{DD} = 5.0 V		0.62	3.40	mA	
					V _{DD} = 3.0 V		0.62	3.40	mA	
				f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 5.0 V		0.50	2.70	mA	
					V _{DD} = 3.0 V		0.50	2.70	mA	
				f _{IH} = 16 MHz ^{Note 4}	V _{DD} = 5.0 V		0.44	1.90	mA	
					V _{DD} = 3.0 V		0.44	1.90	mA	
			HS (high-speed main) mode Note 7	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.31	2.10	mA	
					Resonator connection		0.48	2.20	mA	
				f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.31	2.10	mA	
					Resonator connection		0.48	2.20	mA	
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.21	1.10	mA	
					Resonator connection		0.28	1.20	mA	
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.21	1.10	mA	
					Resonator connection		0.28	1.20	mA	
		Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 5} T _A = −40°C	Square wave input		0.28	0.61	μA		
				Resonator connection		0.47	0.80	μA		
			f _{SUB} = 32.768 kHz ^{Note 5} T _A = +25°C	Square wave input		0.34	0.61	μA		
				Resonator connection		0.53	0.80	μA		
			f _{SUB} = 32.768 kHz ^{Note 5} T _A = +50°C	Square wave input		0.41	2.30	μA		
				Resonator connection		0.60	2.49	μA		
			f _{SUB} = 32.768 kHz ^{Note 5} T _A = +70°C	Square wave input		0.64	4.03	μA		
				Resonator connection		0.83	4.22	μA		
			f _{SUB} = 32.768 kHz ^{Note 5} T _A = +85°C	Square wave input		1.09	8.04	μA		
				Resonator connection		1.28	8.23	μA		
		f _{SUB} = 32.768 kHz ^{Note 5} T _A = +105°C	Square wave input		5.50	41.00	μA			
			Resonator connection		5.50	41.00	μA			
	I _{DD3} ^{Note 6}	STOP mode ^{Note 8}	T _A = −40°C					0.19	0.52	μA
			T _A = +25°C					0.25	0.52	μA
			T _A = +50°C					0.32	2.21	μA
			T _A = +70°C					0.55	3.94	μA
			T _A = +85°C					1.00	7.95	μA
			T _A = +105°C					5.00	40.00	μA

(Notes and Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at same potential)**Simplified I²C mode serial transfer timing (during communication at same potential)**

- Remarks**
- $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance
 - r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14),
h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)
 - f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

UART mode bit width (during communication at different potential) (reference)

- Remarks**
1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance,
 $C_b[\text{F}]$: Communication line (TxDq) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))
 4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp↓) ^{Note}	t_{SIK1}	$4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	88		ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	88		ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	220		ns
Slp hold time (from SCKp↓) ^{Note}	t_{KSI1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	38		ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	38		ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	38		ns
Delay time from SCKp↑ to SOp output ^{Note}	t_{KSO1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		50	ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		50	ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		50	ns

Note When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)

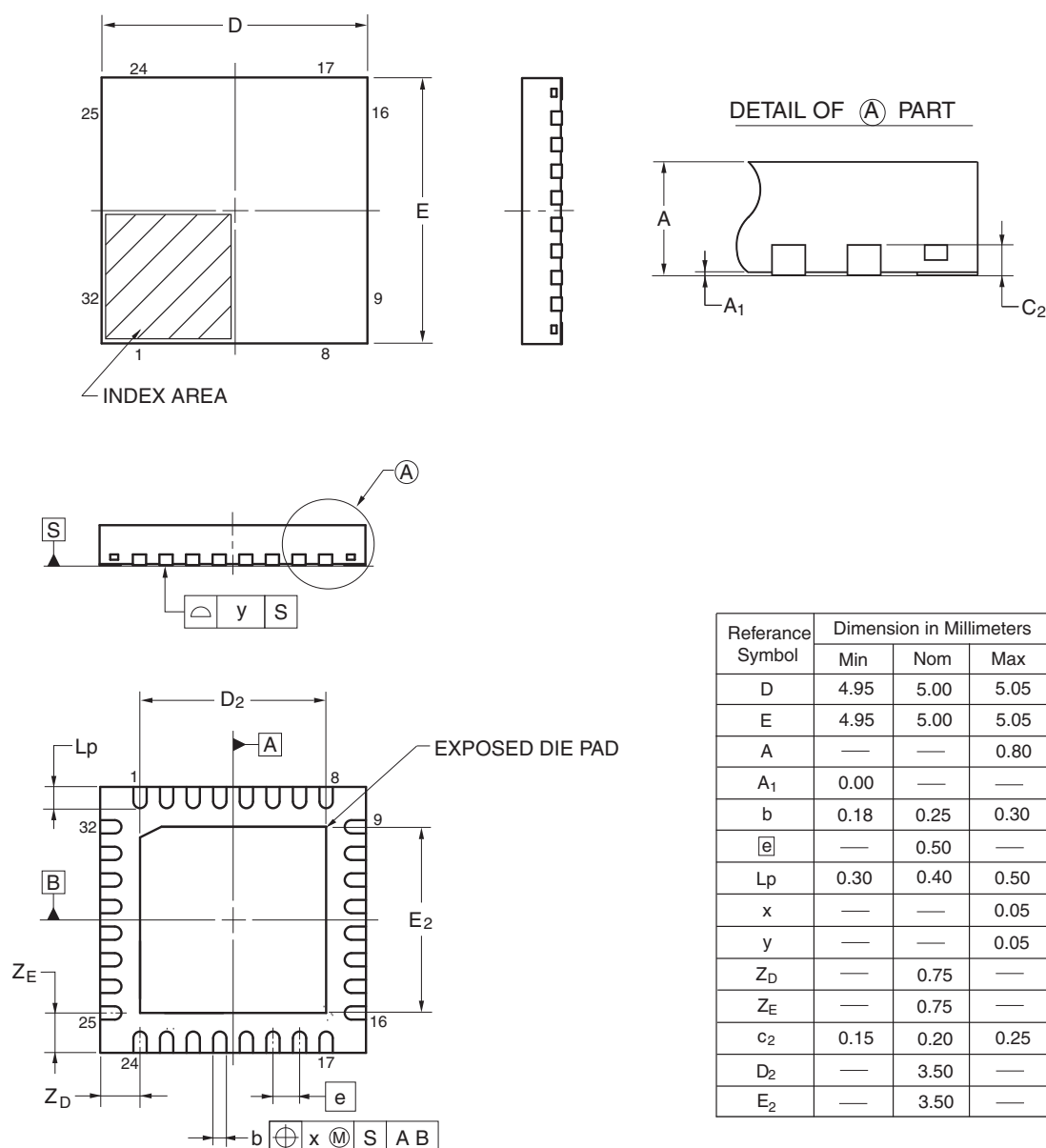
Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time ^{Note 1}	t _{KCY2}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$	$24\text{ MHz} < f_{\text{MCK}}$	$28/f_{\text{MCK}}$		ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	$24/f_{\text{MCK}}$		ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$20/f_{\text{MCK}}$		ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	$16/f_{\text{MCK}}$		ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	$12/f_{\text{MCK}}$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$	$24\text{ MHz} < f_{\text{MCK}}$	$40/f_{\text{MCK}}$		ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	$32/f_{\text{MCK}}$		ns
			$16\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$28/f_{\text{MCK}}$		ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 16\text{ MHz}$	$24/f_{\text{MCK}}$		ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	$16/f_{\text{MCK}}$		ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	$12/f_{\text{MCK}}$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$	$24\text{ MHz} < f_{\text{MCK}}$	$96/f_{\text{MCK}}$		ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	$72/f_{\text{MCK}}$		ns
			$16\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$64/f_{\text{MCK}}$		ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 16\text{ MHz}$	$52/f_{\text{MCK}}$		ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	$32/f_{\text{MCK}}$		ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	$20/f_{\text{MCK}}$		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$		t _{KCY2} /2 – 24		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$		t _{KCY2} /2 – 36		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2}		t _{KCY2} /2 – 100		ns
Slp setup time (to SCKp↑) ^{Note 2}	t _{SIK2}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$		$1/f_{\text{MCK}} + 40$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$		$1/f_{\text{MCK}} + 40$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$		$1/f_{\text{MCK}} + 60$		ns
Slp hold time (from SCKp↑) ^{Note 3}	t _{KSI2}			$1/f_{\text{MCK}} + 62$		ns
Delay time from SCKp↓ to SOp output ^{Note 4}	t _{KSO2}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$			$2/f_{\text{MCK}} + 240$	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$			$2/f_{\text{MCK}} + 428$	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$			$2/f_{\text{MCK}} + 1146$	ns

(Notes, Caution and Remarks are listed on the next page.)

4.5 32-pin Products

R5F100BAANA, R5F100BCANA, R5F100BDANA, R5F100BEANA, R5F100BFANA, R5F100BGANA
 R5F101BAANA, R5F101BCANA, R5F101BDANA, R5F101BEANA, R5F101BFANA, R5F101BGANA
 R5F100BADNA, R5F100BCDNA, R5F100BDDNA, R5F100BEDNA, R5F100BFDNA, R5F100BGDNA
 R5F101BADNA, R5F101BCDNA, R5F101BDDNA, R5F101BEDNA, R5F101BFDNA, R5F101BGDNA
 R5F100BAGNA, R5F100BCGNA, R5F100BDGNA, R5F100BEGNA, R5F100BFGNA, R5F100BGGNA

JEITA Package code	RENESAS code	Previous code	MASS (TYP.)[g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-5	0.06



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4.11 64-pin Products

R5F100LCAFA, R5F100LDAFA, R5F100LEAFA, R5F100LFAFA, R5F100LGAFA, R5F100LHAFA, R5F100LJAFA,
 R5F100LKAFA, R5F100LLAFA
 R5F101LCAFA, R5F101LDAFA, R5F101LEAFA, R5F101LFAFA, R5F101LGAFA, R5F101LHAFA, R5F101LJAFA,
 R5F101LKAFA, R5F101LLAFA
 R5F100LCDFA, R5F100LDDFA, R5F100LEDFA, R5F100LFDFA, R5F100LG DFA, R5F100LHDFA, R5F100LJDFA,
 R5F100LK DFA, R5F100LLDFA
 R5F101LCDFA, R5F101LDDFA, R5F101LEDFA, R5F101LFDFA, R5F101LG DFA, R5F101LHDFA, R5F101LJDFA,
 R5F101LK DFA, R5F101LLDFA
 R5F100LCGFA, R5F100LDGFA, R5F100LEGFA, R5F100LFGFA, R5F100LGGFA, R5F100LHGFA,
 R5F100LJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51

